DiePlus™ Advantage iCE65L08F-TCS110I

SiliconBlue®

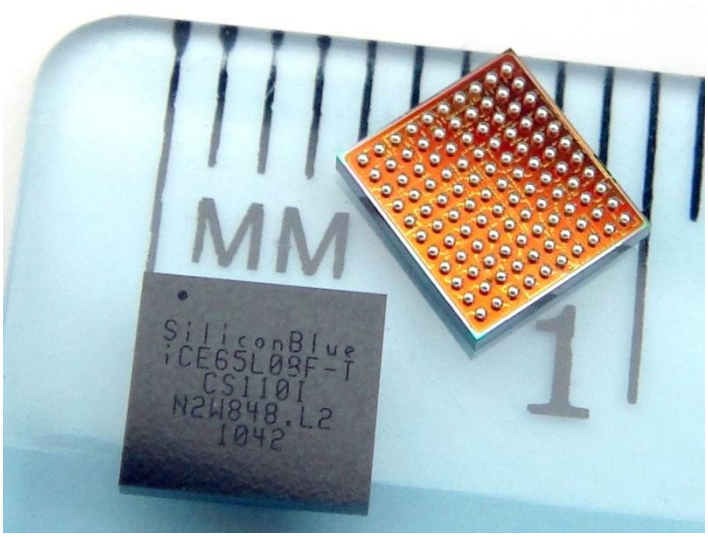
November 24, 2010 (1.0) **Preliminary Data Sheet Supplement**

New package Supplement for CS110
4.35mm x 4.77 mm WLCSP
(see iCE65 L-Series Data Sheet for Electrical and Architecture Characteristics)

DiePlus™ Advantage is SiliconBlue's focused program to provide designers with an optimal device mounting solution for mobile handheld applications. This data sheet provides detailed information regarding the DiePlus Advantage iCE65L08 CS110 device.

- **Smallest possible board footprint**
  - Mechanical package structures such as lead frames and heat slugs are eliminated, as well plastic encapsulation
- **Lowest cost solution, eliminating costs associated with encapsulated packages**
- **Up to 90% less weight than equivalent pin-count packaged devices**
- **WLCSP redistribution layer technology exhibits excellent electrical characteristics**
  - No signal integrity issues often associated with mounting substrates
  - Robust electrical connections minimize resistance and inductance
- **WLCSP technology eliminates need for KGD manufacturing flow**
  - Devices use standard PCB reflow mounting methods
  - Eliminates need for wire bonding and lead frames
  - Available in 0.4mm pitch (CS)

Figure 1: **iCE65L08 WLCSP**



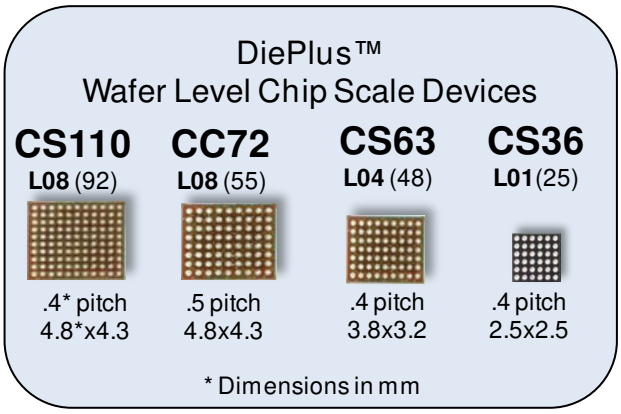
- **Laser etched custom marking available for WLCSP devices**
- **Full wafer custom programming of Non-Volatile Configuration Memory (NVCM) available**

Table 1: **iCE65 Ultra Low-Power Programmable Logic DiePlus Family Summary**

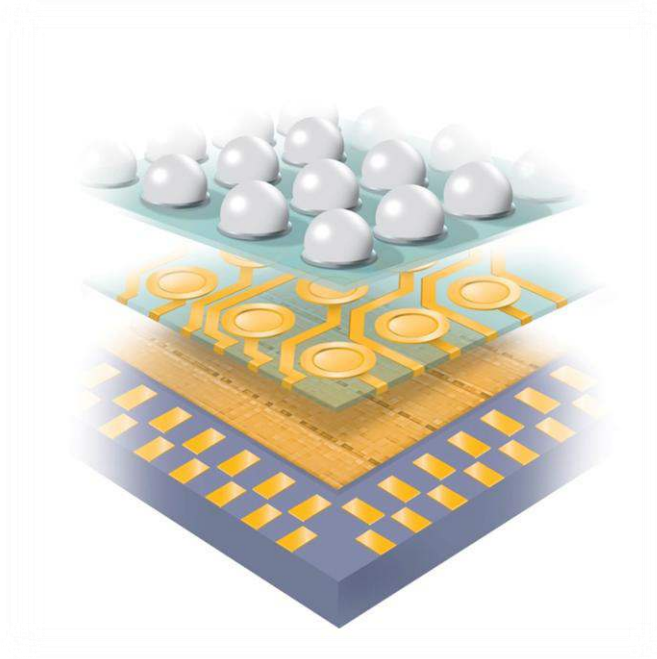
		iCE65L08
Logic Cells (LUT + Flip-Flop)		7,680
RAM4K Memory Blocks		32
RAM4K Memory bits		128K
Configuration bits		1.057 Kb
Size		4.77mm x 4.35mm
Weight		34 mg
Wafer Level Chip Scale Package, WLCSP	**Package**	CS110
	I/O Pins	92(12)

Industry's most advanced packages

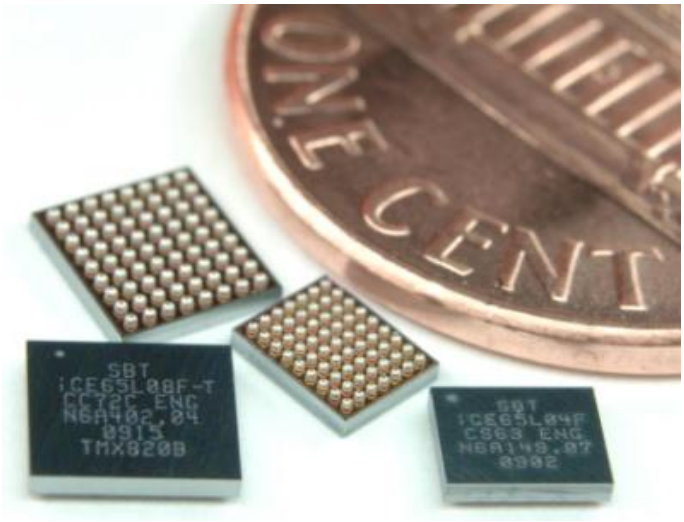
The iCE65 mobileFPGA family uses the most advanced packaging technology available,



including Wafer Level Chip Scale Packaging (WLCSP). WLCSP technology adds a redistribution layer to a bare die, allowing standard mounting balls to be added.



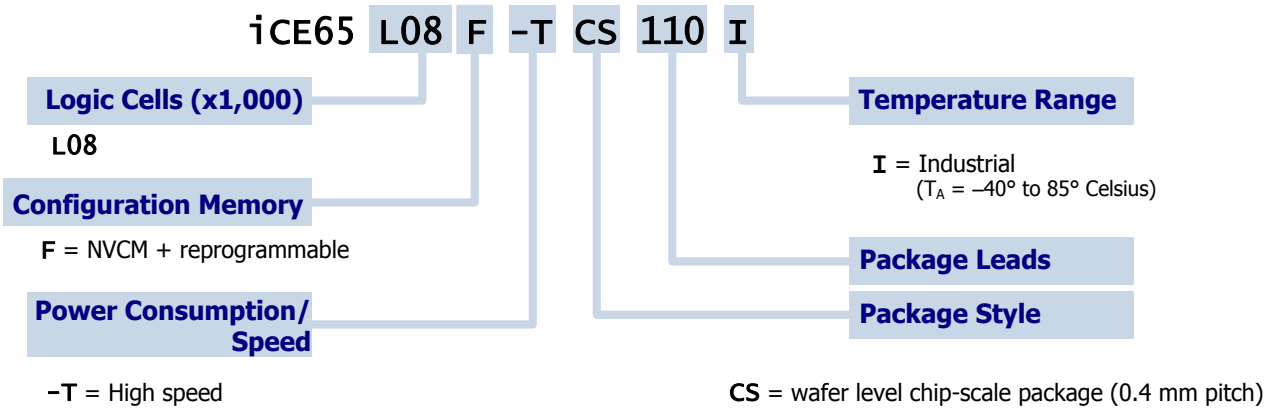
These devices can then be mounted to printed circuit boards just like standard ball grid array devices. By using WLCSP, iCE65 mobileFPGAs offer very small footprints and eliminate standard plastic package costs.



Ordering Information: WLCSP

Figure 2 describes the iCE65 ordering codes for all packaged components. See the separate iCE DiCE data sheets when ordering die-based products.

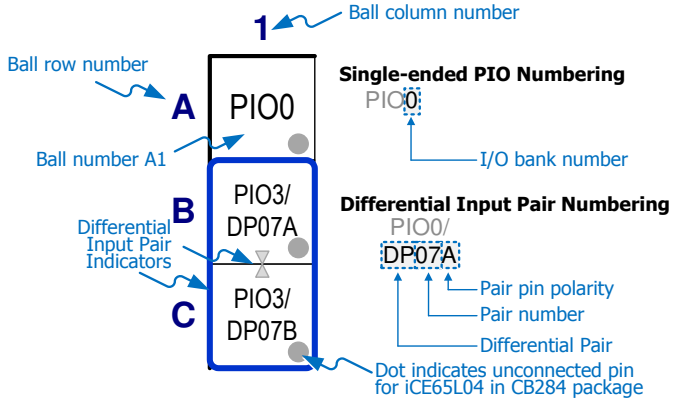
Figure 2: **iCE65 Ordering Codes (WLCSP)**



iCE65 Footprint Diagram Conventions

Figure 3 illustrates the naming conventions used in the following footprint diagrams. Each PIO pin is associated with an I/O Bank. PIO pins in I/O Bank 3 that support differential inputs are also numbered by differential input pair.

Figure 3: **CS and CC Package Footprint Diagram Conventions**



CS110 Wafer-Level Chip-Scale Ball Grid Array

The CS110 package is wafer-level chip-scale ball grid array with 0.4 mm ball pitch. The iCE65L08 is the only device available in this package.

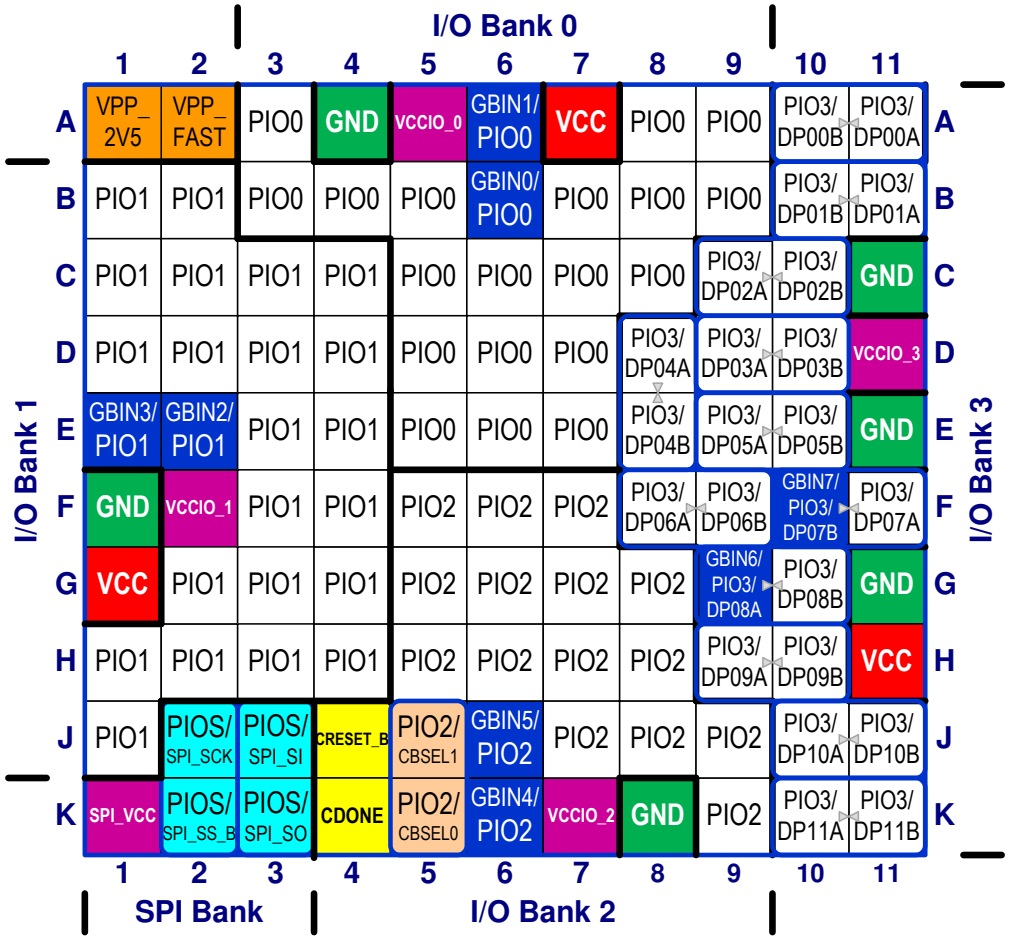
Footprint Diagram

Figure 4 shows the footprint diagram for the 110-ball wafer-level chip-scale package (CS110). Figure 3 shows the conventions used in the diagram. Compared to other packages, the footprint may appear left-right flipped because the balls on the CS110 package are mounted on the same side as the active circuitry. In other packages, the balls are mounted on the opposite side from the active circuitry.

See Table 2 for a complete, detailed pinout for the 110-ball wafer-level chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 4: **iCE65L08 CS110 Wafer-Level Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 2 provides a detailed pinout table for the CS110 package. The iCE65L08 is the only device available in the CS110 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential input pairs in I/O Bank 3. The CS110 package has no JTAG pins.

Table 2: **iCE65L08 CS110 Wafer-level Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Type	Bank
GBIN0/PIO0	B6	GBIN	0
GBIN1/PIO0	A6	GBIN	0
PIO0	A3	PIO	0
PIO0	A8	PIO	0
PIO0	A9	PIO	0
PIO0	B3	PIO	0

Ball Function	Ball Number	Type	Bank
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B7	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	E5	PIO	0
PIO0	E6	PIO	0
PIO0	E7	PIO	0
VCCIO_0	A5	VCCIO	0
GBIN2/PIO1	E2	GBIN	1
GBIN3/PIO1	E1	GBIN	1
PIO1	B1	PIO	1
PIO1	B2	PIO	1
PIO1	C1	PIO	1
PIO1	C2	PIO	1
PIO1	C3	PIO	1
PIO1	C4	PIO	1
PIO1	D1	PIO	1
PIO1	D2	PIO	1
PIO1	D3	PIO	1
PIO1	D4	PIO	1
PIO1	E3	PIO	1
PIO1	E4	PIO	1
PIO1	F3	PIO	1
PIO1	F4	PIO	1
PIO1	G2	PIO	1
PIO1	G3	PIO	1
PIO1	G4	PIO	1
PIO1	H1	PIO	1
PIO1	H2	PIO	1
PIO1	H3	PIO	1
PIO1	H4	PIO	1
PIO1	J1	PIO	1
VCCIO_1	F2	VCCIO	1
CDONE	K4	CONFIG	2
CRESET_B	J4	CONFIG	2
GBIN4/PIO2	K6	GBIN	2
GBIN5/PIO2	J6	GBIN	2
PIO2	F5	PIO	2
PIO2	F6	PIO	2
PIO2	F7	PIO	2
PIO2	G5	PIO	2
PIO2	G6	PIO	2
PIO2	G7	PIO	2

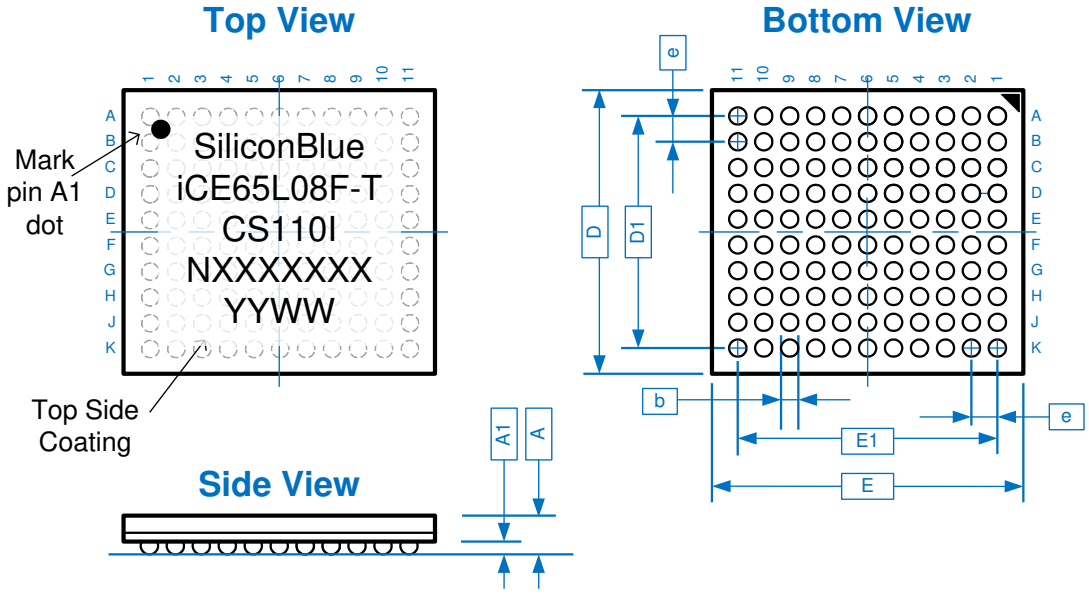
Ball Function	Ball Number	Type	Bank
PIO2	G8	PIO	2
PIO2	H5	PIO	2
PIO2	H6	PIO	2
PIO2	H7	PIO	2
PIO2	H8	PIO	2
PIO2	J7	PIO	2
PIO2	J8	PIO	2
PIO2	J9	PIO	2
PIO2	K9	PIO	2
PIO2/CBSEL0	K5	PIO	2
PIO2/CBSEL1	J5	PIO	2
VCCIO_2	K7	VCCIO	2
PIO3/DP00A	A11	DPIO	3
PIO3/DP00B	A10	DPIO	3
PIO3/DP01A	B11	DPIO	3
PIO3/DP01B	B10	DPIO	3
PIO3/DP02A	C9	DPIO	3
PIO3/DP02B	C10	DPIO	3
PIO3/DP03A	D9	DPIO	3
PIO3/DP03B	D10	DPIO	3
PIO3/DP04A	D8	DPIO	3
PIO3/DP04B	E8	DPIO	3
PIO3/DP05A	E9	DPIO	3
PIO3/DP05B	E10	DPIO	3
PIO3/DP06A	F8	DPIO	3
PIO3/DP06B	F9	DPIO	3
PIO3/DP07A	F11	DPIO	3
GBIN7/PIO3/DP07B	F10	DPIO/GBIN	3
GBIN6/PIO3/DP08A	G9	DPIO/GBIN	3
PIO3/DP08B	G10	DPIO	3
PIO3/DP09A	H9	DPIO	3
PIO3/DP09B	H10	DPIO	3
PIO3/DP10A	J10	DPIO	3
PIO3/DP10B	J11	DPIO	3
PIO3/DP11A	K10	DPIO	3
PIO3/DP11B	K11	DPIO	3
VCCIO_3	D11	VCCIO	3
PIOS/SPI_SO	K3	SPI	SPI
PIOS/SPI_SI	J3	SPI	SPI
PIOS/SPI_SCK	J2	SPI	SPI
PIOS/SPI_SS_B	K2	SPI	SPI
SPI_VCC	K1	SPI_VCC	SPI
GND	A4	GND	GND
GND	C11	GND	GND
GND	E11	GND	GND
GND	F1	GND	GND
GND	G11	GND	GND
GND	K8	GND	GND
VCC	A7	VCC	VCC

Ball Function	Ball Number	Type	Bank
VCC	G1	VCC	VCC
VCC	H11	VCC	VCC
VPP_2V5	A1	VPP	VPP
VPP_FAST	A2	VPP	VPP

Package Mechanical Drawing

Figure 5: **CS110 Package Mechanical Drawing**

CS110: 4.354 x 4.770 mm, 110-ball, 0.4 mm ball-pitch, wafer-level chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			10		Rows
Number of Signal Balls		n		110		Balls
Body Size	X	E	—	4.770	4.790	mm
	Y	D	—	4.354	4.374	
Ball Pitch		e	—	0.40	—	
Ball Diameter		b	—	0.25	—	
Edge Ball Center to Center	X	E1	—	4.00	—	
	Y	D1	—	3.60	—	
Package Height		A	0.761	0.800	0.839	
Stand Off		A1	0.17	0.20	0.23	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L08F	Part number
	-T	Power/Speed
3	CS110	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
37	30

Revision History

Version	Date	Description
1.0	24-NOV-2010	Initial Preliminary Data Sheet Supplement Release

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