

4-Mbit (256K x 16) Pseudo Static RAM

Features

- Wide voltage range: 2.70V–3.30V
- Access time: 55 ns, 60 ns and 70 ns
- Ultra-low active power
 - Typical active current: 1 mA @ f = 1 MHz
- Typical active current: 8 mA @ f = f_{max} (70-ns speed)
- Ultra low standby power
- · Automatic power-down when deselected
- CMOS for optimum speed/power
- Offered in a 48-ball BGA package

Functional Description^[1]

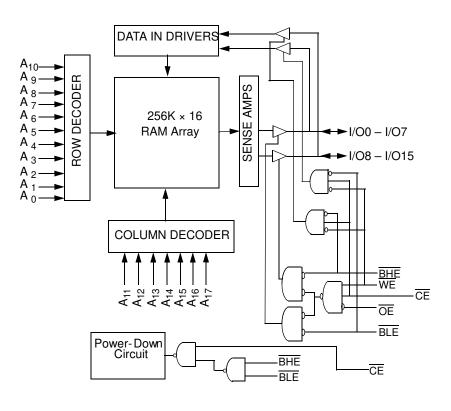
The CYK256K16MCCB is a high-performance CMOS Pseudo static RAM organized as 256K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life[™] (MoBL[®]) in portable applications such as cellular telephones. The device

can be put into standby mode when deselected (\overline{CE} HIGH or both BHE and BLE are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , BLE HIGH), or during a write operation (\overline{CE} LOW and WE LOW).

<u>Writing</u> to the device is accomplished by taking Chip Enable $(\overline{CE} \text{ LOW})$ and Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins $(I/O_0 \text{ through } I/O_7)$ is written into the location specified on the address pins $(A_0 \text{ through } A_{17})$. If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins $(I/O_8 \text{ through } I/O_{15})$ is written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enable (CE LOW) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . Refer to the truth table for a complete description of read and write modes.

Logic Block Diagram

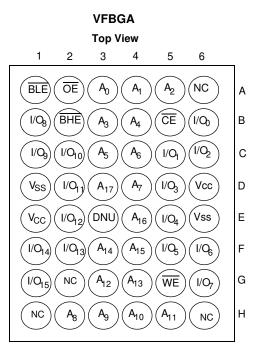


Note:

1. For best practice recommendations, please refer to the CY application note System Design Guidelines on http://www.cypress.com.



Pin Configuration^[2, 3, 4]



Product Portfolio

					Power Dissipatio				n	
					(Operating	g I _{CC} (mA))		
	V _{CC} Range (V)		V _{CC} Range (V)		f = 1	MHz	f = 1	max	Standby	I _{SB2} (μ A)
Product	Min.	Typ. ^[5]	Max.	Speed (ns)	Typ. ^[5]	Max.	Typ. ^[5]	Max.	Typ. ^[5]	Max.
CYK256K16MCCB	2.70	3.0	3.30	55	1	5	14	22	17	40
				60						
				70			8	15		

Notes:

2. Ball H1, G2 and ball H6 for the VFBGA package can be used to upgrade to an 8-Mbit, 16-Mbit and 32-Mbit density, respectively.

3. NC "no connect" - not connected internally to the die.

4. DNU (Do Not Use) pins have to be left floating or tied to Vss to ensure proper application. 5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25^{\circ}C$.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	65°C to + 150°C
Ambient Temperature with Power Applied	–55°C to + 125°C
Supply Voltage to Ground Potential	0.4V to 4.6V
DC Voltage Applied to Outputs in High-Z State ^[6, 7, 8]	–0.4V to 3.7V

Electrical Characteristics Over the Operating Range

DC Input Voltage ^[6, 7, 8]	–0.4V to 3.7V
Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001 V
Latch-up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	–25°C to +85°C	2.70V to 3.30V

				CYK256K16MCCB -55, 60, 70				
Parameter	Description	Test Conditi	Min.	Typ. ^[5]	Max.	Unit		
V _{CC}	Supply Voltage		2.7	3.0	3.3	V		
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	$V_{CC} = 2.70V$	$V_{CC} - 0.4$			V	
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = 2.70V			0.4	V	
V _{IH}	Input HIGH Voltage		•	0.8 * Vcc		V _{CC} + 0.4V	V	
V _{IL}	Input LOW Voltage			-0.4		0.6	V	
I _{IX}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$	–1		+1	μA		
I _{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}, Outp$	–1		+1	μA		
I _{CC}	V _{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	V _{CC} = V _{CCmax} I _{OUT} = 0 mA		14 for –55 14 for –60 8 for –70	22 for55 22 for60 15 for70	mA	
		f = 1 MHz	CMOS levels		1 for all speeds	5 for all speeds	mA	
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\begin{array}{l} \hline CE \geq V_{CC}-0.2V \\ V_{IN} \geq V_{CC}-0.2V, \ V_{IN} \leq \\ 0.2V) \ f = f_{MAX} \ (Address \\ and \ \underline{Data} \ \underline{Only}), \ f = 0 \\ (\underline{OE}, \ WE, \ BHE \ and \\ BLE), \ V_{CC} = 3.30V \end{array} V_{CC} = 3.3V$			150	250	μΑ	
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\label{eq:constraint} \begin{split} \overline{CE} \geq V_{CC} & - 0.2V \\ V_{IN} \geq V_{CC} & - 0.2V \text{ or} \\ V_{IN} \leq 0.2V, \\ f = 0, \ V_{CC} = 3.30V \end{split}$	V _{CC} = 3.3V		17	40	μA	

Thermal Resistance^[9]

Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods	55	°C/W
Θ^{JC}		and procedures for measuring thermal impedence, per EIA/JESD51.	17	°C/W

Capacitance^[9]

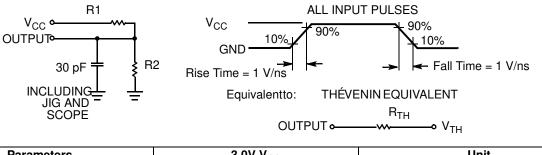
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz},$	8	pF
C _{OUT}	Output Capacitance	$V_{CC} = V_{CC(typ)}$	8	pF

Notes:

V_{IL(MIN)} = -0.5V for pulse durations less than 20 ns.
V_{IL(MIX)} = V_{CC} + 0.5V for pulse durations less than 20 ns.
Overshoot and undershoot specifications are characterized and are not 100% tested.
Tested initially and after any design or process changes that may affect these parameters.



AC Test Loads and Waveforms



Parameters	3.0V V _{CC}	Unit
R1	22000	Ω
R2	22000	Ω
R _{TH}	11000	Ω
V _{TH}	1.50	V

Switching Characteristics Over the Operating Range^[10]

	55 ns ^[14]		60 ns		70 ns		
Description	Min.	Max.	Min.	Max.	Min.	Max.	Unit
							•
Read Cycle Time	55		60		70		ns
Address to Data Valid		55		60		70	ns
Data Hold from Address Change	5		8		10		ns
CE LOW to Data Valid		55		60		70	ns
OE LOW to Data Valid		25		25		35	ns
OE LOW to LOW Z ^[11, 13]	5		5		5		ns
OE HIGH to High Z ^[11, 13]		25		25		25	ns
CE LOW to Low Z ^[11, 13]	2		2		5		ns
CE HIGH to High Z ^[11, 13]		25		25		25	ns
BLE/BHE LOW to Data Valid		55		60		70	ns
BLE/BHE LOW to Low Z ^[11, 13]	5		5		5		ns
BLE/BHE HIGH to HIGH Z ^[11, 13]		10		10		25	ns
Address Skew		0		5		10	ns
	-	1		1	1	•	
Write Cycle Time	55		60		70		ns
CE LOW to Write End	45		45		60		ns
Address Set-Up to Write End	45		45		55		ns
Address Hold from Write End	0		0		0		ns
Address Set-Up to Write Start	0		0		0		ns
WE Pulse Width	40		40		45		ns
	Read Cycle Time Address to Data Valid Data Hold from Address Change CE CE LOW to Data Valid OE LOW to Data Valid OE LOW to LOW Z ^[11, 13] OE DE HIGH to High Z ^[11, 13] CE DOE HIGH to High Z ^[11, 13] CE BLE/BHE LOW to Low Z ^[11, 13] BLE/BHE BLE/BHE LOW to Low Z ^[11, 13] BLE/BHE Address Skew Write CE Write Cycle Time CE CE Write Cycle Time CE Address Set-Up to Write End Address Hold from Write End Address Set-Up to Write End Address Set-Up to Write Start	DescriptionMin.Read Cycle Time55Address to Data ValidData Hold from Address Change5CE LOW to Data ValidOE LOW to Data ValidOE LOW to LOW Z ^[11, 13] 5OE HIGH to High Z ^[11, 13] 2CE LOW to Low Z ^[11, 13] 2CE HIGH to High Z ^[11, 13] 5BLE/BHE LOW to Low Z ^[11, 13] 5BLE/BHE LOW to Low Z ^[11, 13] 5BLE/BHE HIGH to HIGH Z ^[11, 13] 5BLE/BHE HIGH to HIGH Z ^[11, 13] 5Address SkewWrite Cycle Time55CE LOW to Write End45Address Set-Up to Write End0Address Set-Up to Write Start0	DescriptionMin.Max.Read Cycle Time55Address to Data Valid55Data Hold from Address Change5CE LOW to Data Valid55OE LOW to Data Valid25OE LOW to LOW Z ^[11, 13] 5OE HIGH to High Z ^[11, 13] 25CE LOW to Low Z ^[11, 13] 25CE LOW to Low Z ^[11, 13] 25DE HIGH to High Z ^[11, 13] 25BLE/BHE LOW to Data Valid55BLE/BHE LOW to Low Z ^[11, 13] 5BLE/BHE HIGH to HIGH Z ^[11, 13] 10Address Skew0Write Cycle Time55CE LOW to Write End45Address Set-Up to Write End45Address Set-Up to Write Start0	Description Min. Max. Min. Read Cycle Time 55 60 Address to Data Valid 55 60 Data Hold from Address Change 5 8 CE LOW to Data Valid 55 8 OE LOW to Data Valid 25 5 OE LOW to Low Z ^[11, 13] 5 5 OE HIGH to High Z ^[11, 13] 25 2 CE LOW to Low Z ^[11, 13] 25 2 CE HIGH to High Z ^[11, 13] 25 2 CE HIGH to High Z ^[11, 13] 25 5 BLE/BHE LOW to Data Valid 55 5 BLE/BHE HIGH to HIGH Z ^[11, 13] 10 2 Address Skew 0 10 10 Mrite Cycle Time 55 60 CE LOW to Write End 45 45 Address Set-Up to Write End 45 45 Address Hold from Write End 0 0	Description Min. Max. Min. Max. Read Cycle Time 55 60 60 Address to Data Valid 55 60 Data Hold from Address Change 5 8 60 OE LOW to Data Valid 55 60 60 OE LOW to Data Valid 25 25 25 OE LOW to Data Valid 25 25 25 OE LOW to LOW Z ^[11, 13] 5 5 60 OE HIGH to High Z ^[11, 13] 2 2 25 CE LOW to Low Z ^[11, 13] 2 2 25 DE HIGH to High Z ^[11, 13] 2 2 25 CE HIGH to High Z ^[11, 13] 2 5 60 BLE/BHE LOW to Low Z ^[11, 13] 5 5 60 BLE/BHE HIGH to HIGH Z ^[11, 13] 10 10 10 Address Skew 0 5 5 Write Cycle Time 55 60 5 CE LOW to Write End 45 45 45 Address	Description Min. Max. Min. Max. Min. Read Cycle Time 55 60 70 Address to Data Valid 55 60 70 Data Hold from Address Change 5 8 10 CE LOW to Data Valid 55 60 10 OE LOW to Data Valid 25 25 10 OE LOW to LOW z ^[11, 13] 5 5 5 OE LOW to LOW z ^[11, 13] 2 2 5 OE LOW to Low z ^[11, 13] 2 25 10 OE LOW to Low z ^[11, 13] 2 2 5 CE LOW to Low z ^[11, 13] 2 2 5 CE HIGH to High z ^[11, 13] 2 25 10 BLE/BHE LOW to Data Valid 55 60 5 BLE/BHE HIGH to HIGH Z ^[11, 13] 10 10 10 Address Skew 0 5 5 5 Write Cycle Time 55 60 70 6 CE LOW to Write End 45	Description Min. Max. Min. Max. Min. Max. Read Cycle Time 55 60 70 Address to Data Valid 55 60 70 Data Hold from Address Change 5 8 10 CE LOW to Data Valid 55 60 70 DE LOW to Data Valid 25 25 35 OE LOW to LOW Z ^[11, 13] 5 5 5 5 OE LOW to LOW Z ^[11, 13] 2 2 5 25 OE LOW to Low Z ^[11, 13] 2 2 5 25 OE HIGH to High Z ^[11, 13] 2 2 5 25 CE HIGH to High Z ^[11, 13] 2 2 5 25 BLE/BHE LOW to Low Z ^[11, 13] 5 5 5 5 BLE/BHE LOW to Low Z ^[11, 13] 10 10 25 4dress Skew 0 5 10 Write Cycle Time 55 60 70 5 10 CE LOW to Write End 45

Notes:

10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0V to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section. 11. t_{HZOE} , t_{HZEE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state. 12. The internal Write time of the memory is defined by the overlap of WE, $\overline{CE} = V_{IL}$, BHE and/or BLE = V_{IL} . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write the write.

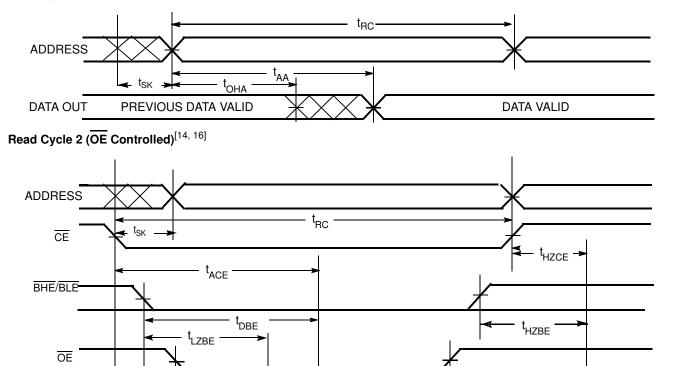
13. High Z and Low-Z parameters are characterized and are not 100% tested.
14. To achieve 55-ns performance, the read access should be CE controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.



Switching Characteristics Over the Operating Range^[10] (continued)

		55 ns ^[14]		60 ns		70 ns		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t _{BW}	BLE/BHE LOW to Write End	50		50		55		ns
t _{SD}	Data Set-Up to Write End	25		25		25		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	WE LOW to High-Z ^[11, 13]		25		25		25	ns
t _{LZWE}	WE HIGH to Low-Z ^[11, 13]	5		5		5		ns

Switching Waveforms



t_{DOE}

50%

- t_{LZOE} HIGH IMPEDANCE

t_{LZCE}

Read Cycle 1 (Address Transition Controlled)^[14, 15, 16]

Notes:

DATA OUT-

SUPPL **CURRENT**

15. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$. 16. WE is HIGH for Read Cycle.

HIGH IMPEDANCE

 I_{CC}

I_{SB}

^IHZOE

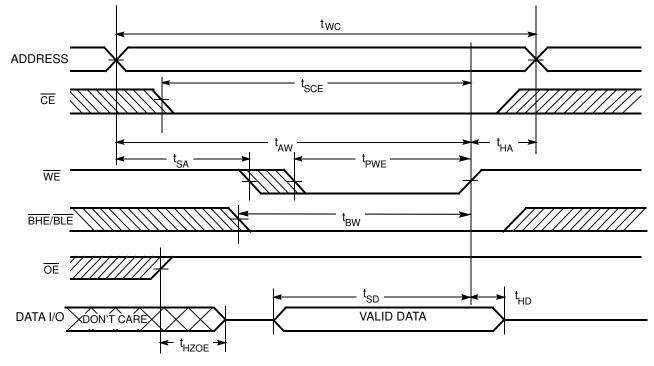
50%

DATA VALID

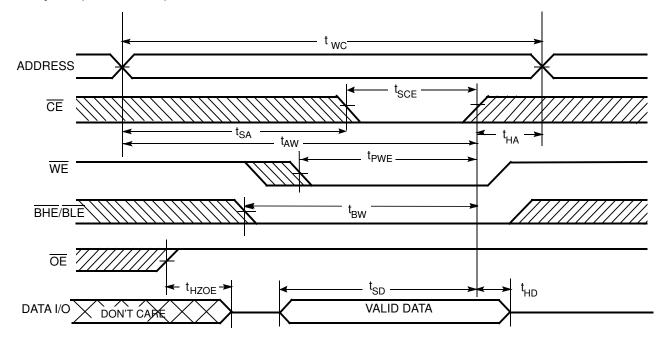


Switching Waveforms (continued)

Write Cycle 1 (WE Controlled)^[12, 13, 17, 18, 19]







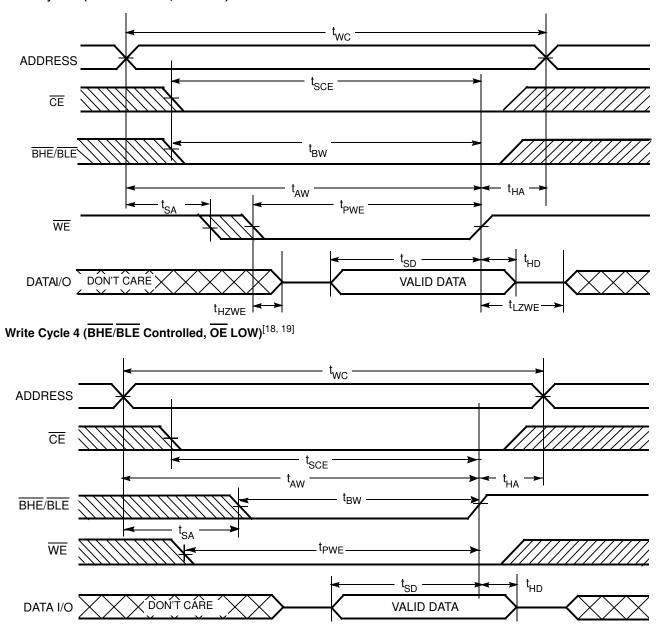
Notes:

17. Data I/O is high-impedance if $\overline{OE} \ge \underline{V_{IH.}}$ 18. If Chip Enable goes INACTIVE with WE = V_{IH} , the output remains in a high-impedance state. 19. During this period in the DATA I/O waveform, the I/Os could be in the output state and input signals should not be applied.



Switching Waveforms (continued)

Write Cycle 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[18, 19]





Truth Table [20]

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	Х	Х	Х	Х	High Z	Deselect/Power-Down	Standby (I _{SB})
Х	Х	Х	Н	Н	High Z	Deselect/Power-Down	Standby (I _{SB})
L	Н	L	L	L	Data Out (I/O0 – I/O15)	Read	Active (I _{CC})
L	Н	L	Н	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read	Active (I _{CC})
L	Н	L	L	Н	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read	Active (I _{CC})
L	Н	Н	L	Н	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	Н	L	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	L	L	High Z	Output Disabled	Active (I _{CC})
L	L	Х	L	L	Data In (I/O0 – I/O15)	Write	Active (I _{CC})
L	L	Х	Н	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write	Active (I _{CC})
L	L	Х	L	Н	High Z (I/O0 – I/O7); Data In (I/O8 – I/O15)	Write	Active (I _{CC})

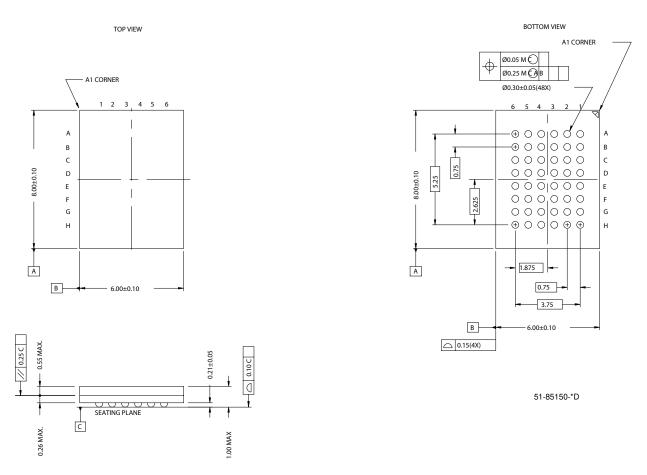
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CYK256K16MCCBU-55BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
	CYK256K16MCBU-55BVXI		48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm) (Pb-Free)	
60	CYK256K16MCCBU-60BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
70	CYK256K16MCCBU-70BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
	CYK256K16MCBU-70BVXI	1	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm) (Pb-Free)	

Note: 20. H = Logic HIGH, L = Logic LOW, X = Don't Care.



Package Diagram



48-ball VFBGA (6 x 8 x 1 mm) (51-85150)

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Document History Page

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	223482	See ECN	REF	New data sheet
*A	234474	See ECN	SYT	Changed ball E3 on package pinout from NC to DNU
*В	260330	See ECN	PCI	Changed from preliminary to final
*C	298651	See ECN	PCI	Added 60-ns speed bin
*D	314013	See ECN	RKF	Added Pb-Free parts to the Ordering information
*E	397852	See ECN	SYT	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Changed typo in ordering code from CYK256K16MCCB to CYK256K16MCCBU in the "Ordering Information" on Page#8 Updated the revision of package diagram of Spec 51-85150 from *B to *D
*F	522566	See ECN	NXR	Changed V _{IL} Max spec from 0.4 V to 0.6 V in DC Electrical Characteristics tabl