CYK256K16MCCB
MoBL3™

4-Mbit (256K x 16) Pseudo Static RAM

Features

- **Wide voltage range: 2.70V–3.30V**
- **Access time: 55 ns, 60 ns and 70 ns**
- **Ultra-low active power**
  - **Typical active current: 1 mA @ f = 1 MHz**
  - **Typical active current: 8 mA @ f = f_{max} (70-ns speed)**
- **Ultra low standby power**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in a 48-ball BGA package**

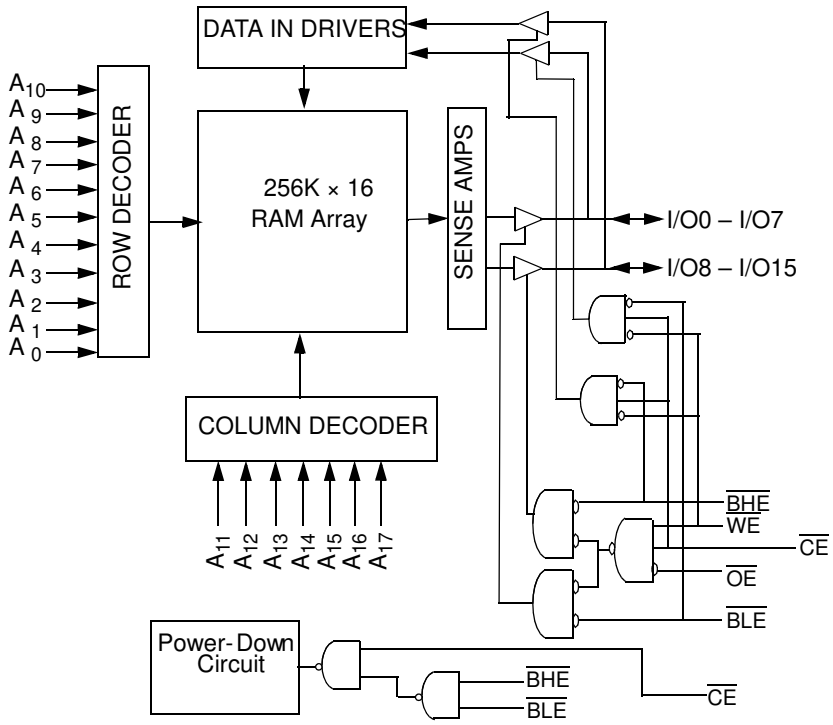
Functional Description[1]

The CYK256K16MCCB is a high-performance CMOS Pseudo static RAM organized as 256K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device can be put into standby mode when deselected ($\overline{CE}$ HIGH or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$ LOW) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$ LOW) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. Refer to the truth table for a complete description of read and write modes.

Logic Block Diagram

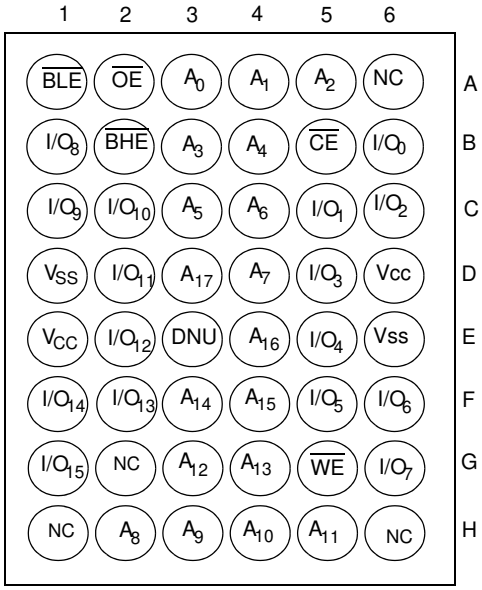


Note:
1. For best practice recommendations, please refer to the CY application note *System Design Guidelines* on http://www.cypress.com.

Pin Configuration[2, 3, 4]

VFBGA

Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC}(mA)				Standby I_{SB2}(µA)	
					f = 1MHz		f = f_{max}			
	Min.	Typ.[5]	Max.		Typ.[5]	Max.	Typ.[5]	Max.	Typ.[5]	Max.
CYK256K16MCCB	2.70	3.0	3.30	55	1	5	14	22	17	40
				60						
				70			8	15		

Notes:
2. Ball H1, G2 and ball H6 for the VFBGA package can be used to upgrade to an 8-Mbit, 16-Mbit and 32-Mbit density, respectively.
3. NC "no connect" – not connected internally to the die.
4. DNU (Do Not Use) pins have to be left floating or tied to Vss to ensure proper application.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied .....–55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.4V to 4.6V

DC Voltage Applied to Outputs in High-Z State[6, 7, 8] ..... –0.4V to 3.7V

DC Input Voltage[6, 7, 8] .....–0.4V to 3.7V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current .....> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–25°C to +85°C	2.70V to 3.30V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CYK256K16MCCB -55, 60, 70			Unit
				Min.	Typ.[5]	Max.	
V_{CC}	Supply Voltage			2.7	3.0	3.3	V
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.70V	V_{CC} – 0.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.70V			0.4	V
V_{IH}	Input HIGH Voltage			0.8 * Vcc		V_{CC} + 0.4V	V
V_{IL}	Input LOW Voltage			–0.4		0.6	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels		14 for –55 14 for –60 8 for –70	22 for –55 22 for –60 15 for –70	mA
		f = 1 MHz			1 for all speeds	5 for all speeds	mA
I_{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC}–0.2V V_{IN} ≥ V_{CC}–0.2V, V_{IN} ≤ 0.2V) f = f_{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V_{CC} = 3.30V	V_{CC} = 3.3V		150	250	µA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.30V	V_{CC} = 3.3V		17	40	µA

Thermal Resistance[9]

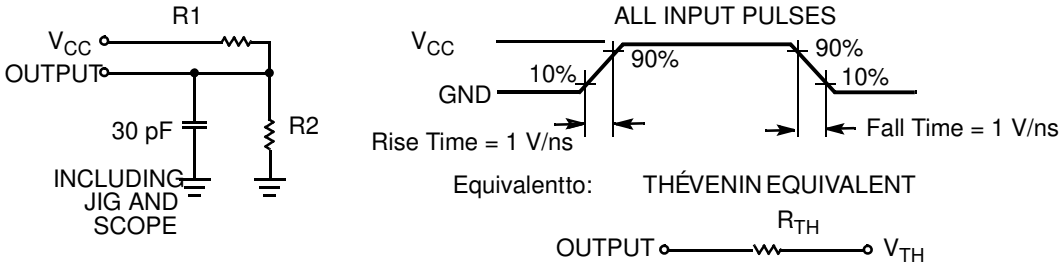
Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedence, per EIA/JESD51.	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		17	°C/W

Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:
6. $V_{IL(MIN)}$ = –0.5V for pulse durations less than 20 ns.
7. $V_{IH(Max)}$ = V_{CC} + 0.5V for pulse durations less than 20 ns.
8. Overshoot and undershoot specifications are characterized and are not 100% tested.
9. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Parameters	3.0V V_{CC}	Unit
R1	22000	Ω
R2	22000	Ω
R_{TH}	11000	Ω
V_{TH}	1.50	V

Switching Characteristics Over the Operating Range[10]

Parameter	Description	55 ns[14]		60 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	55		60		70		ns
t_{AA}	Address to Data Valid		55		60		70	ns
t_{OHA}	Data Hold from Address Change	5		8		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		60		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[11, 13]	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 13]		25		25		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[11, 13]	2		2		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[11, 13]		25		25		25	ns
t_{DBE}	BLE/BHE LOW to Data Valid		55		60		70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[11, 13]	5		5		5		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[11, 13]		10		10		25	ns
t_{SK}[14]	Address Skew		0		5		10	ns
Write Cycle[12]								
t_{WC}	Write Cycle Time	55		60		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		45		60		ns
t_{AW}	Address Set-Up to Write End	45		45		55		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		40		45		ns

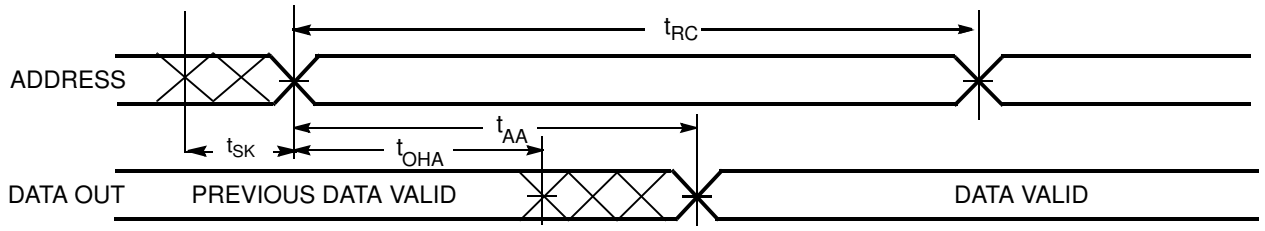
Notes:
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0V to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
12. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
13. High-Z and Low-Z parameters are characterized and are not 100% tested.
14. To achieve 55-ns performance, the read access should be $\overline{CE}$ controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Characteristics Over the Operating Range[10] (continued)

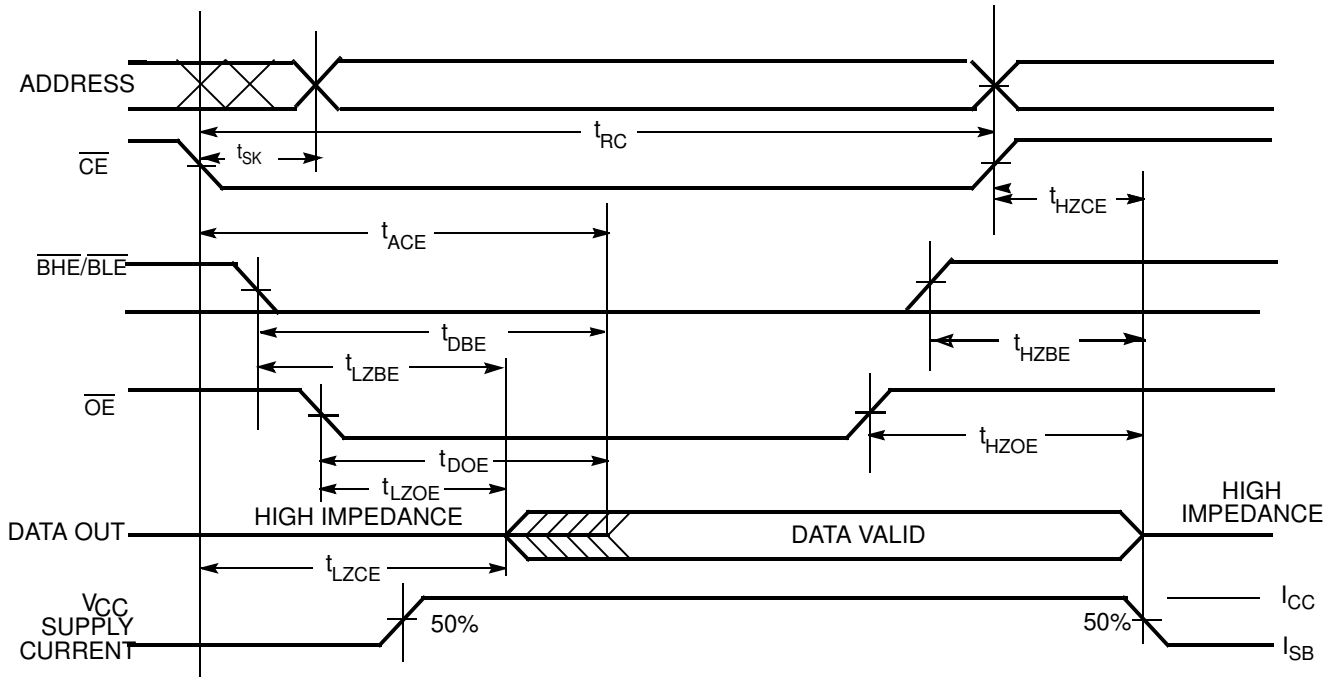
Parameter	Description	55 ns[14]		60 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	50		50		55		ns
t_{SD}	Data Set-Up to Write End	25		25		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 13]		25		25		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11, 13]	5		5		5		ns

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[14, 15, 16]



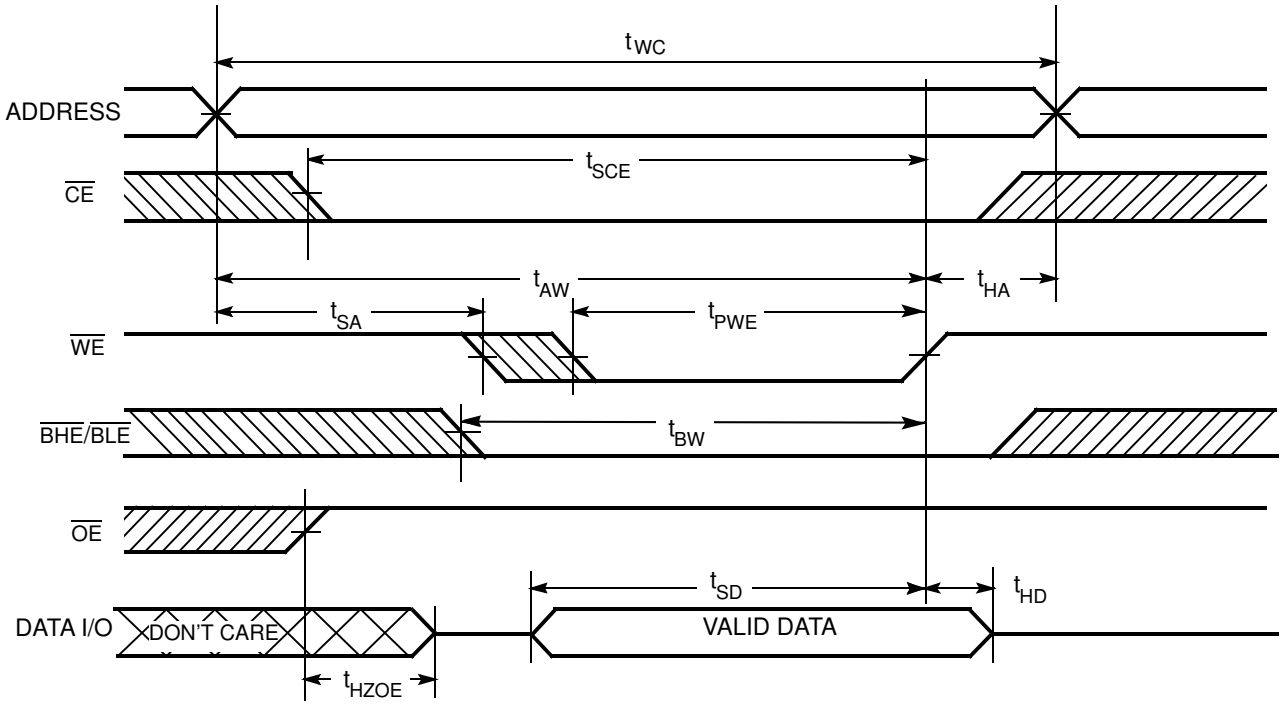
Read Cycle 2 ($\overline{OE}$ Controlled)[14, 16]



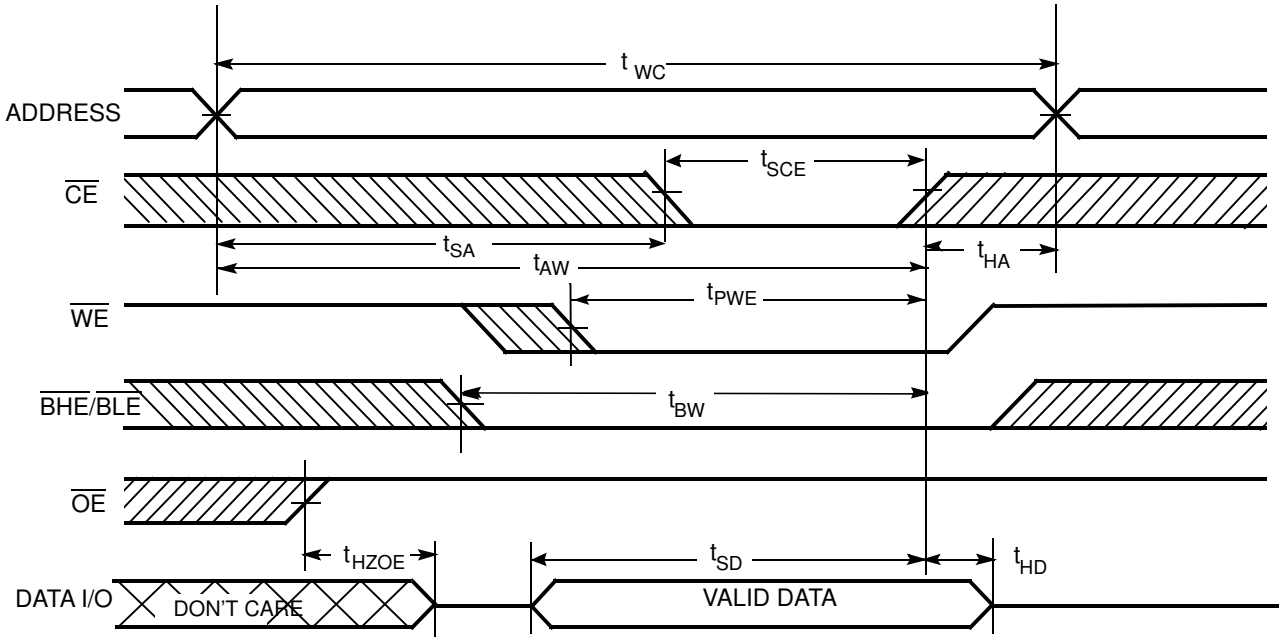
Notes:
15. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
16. $\overline{WE}$ is HIGH for Read Cycle.

Switching Waveforms (continued)

Write Cycle 1 ($\overline{WE}$ Controlled)[12, 13, 17, 18, 19]



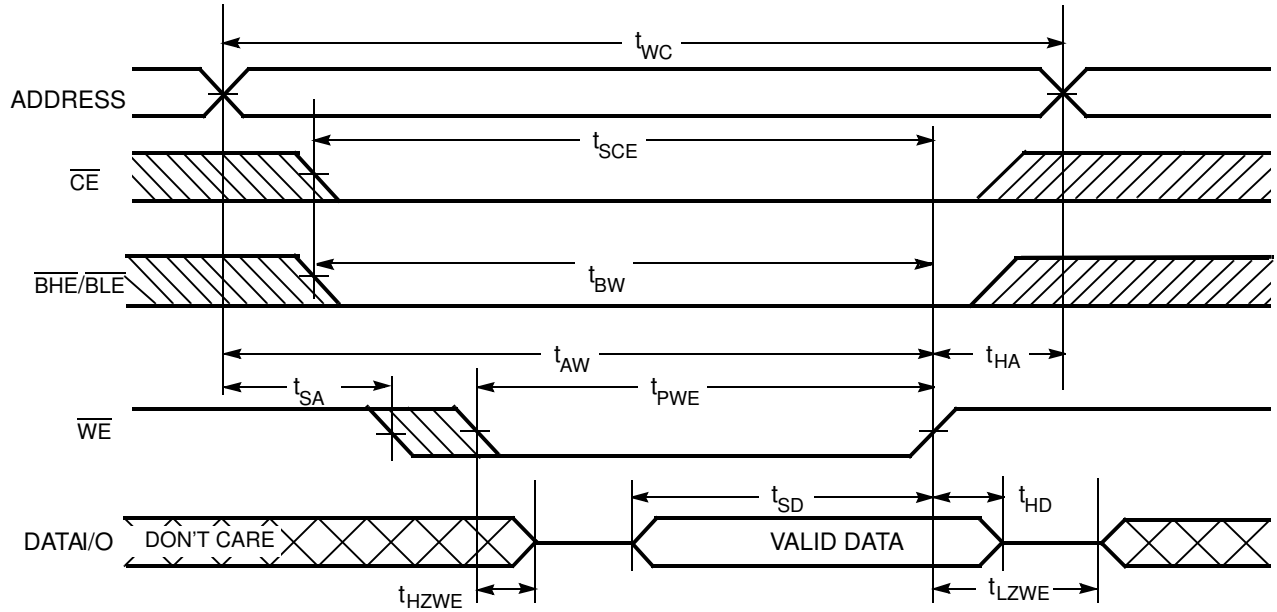
Write Cycle 2 ($\overline{CE}$ Controlled)[12, 13, 17, 18, 19]



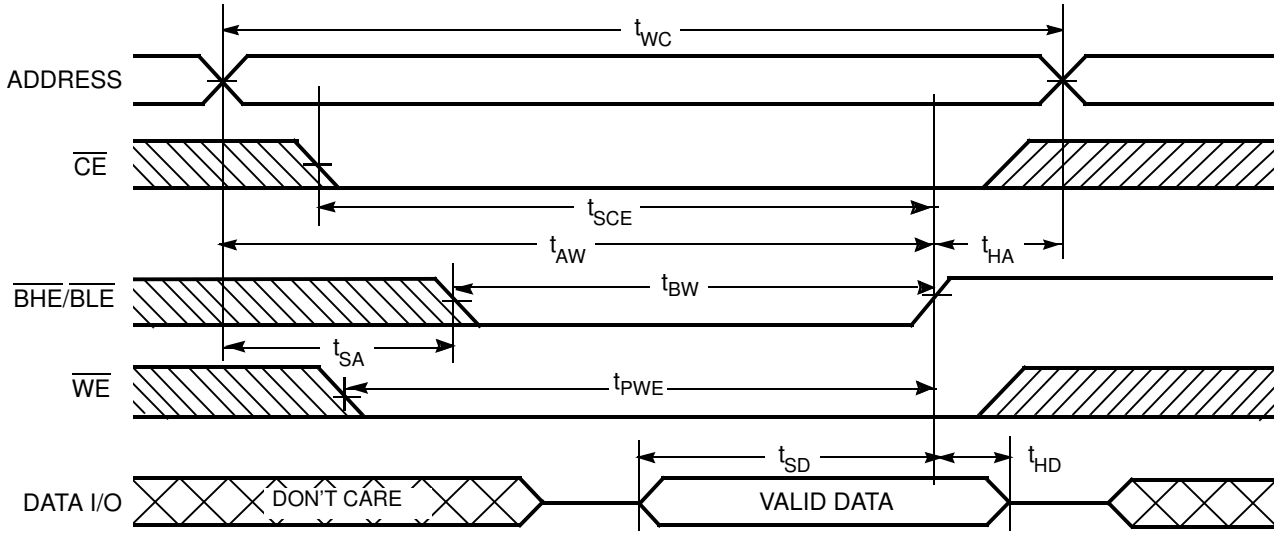
Notes:
17. Data I/O is high-impedance if $\overline{OE} \geq V_{IH}$.
18. If Chip Enable goes INACTIVE with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
19. During this period in the DATA I/O waveform, the I/Os could be in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[18, 19]



Write Cycle 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[18, 19]



Truth Table [20]

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O0 – I/O15)	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read	Active (I_{CC})
L	H	L	L	H	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O0 – I/O15)	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write	Active (I_{CC})
L	L	X	L	H	High Z (I/O0 – I/O7); Data In (I/O8 – I/O15)	Write	Active (I_{CC})

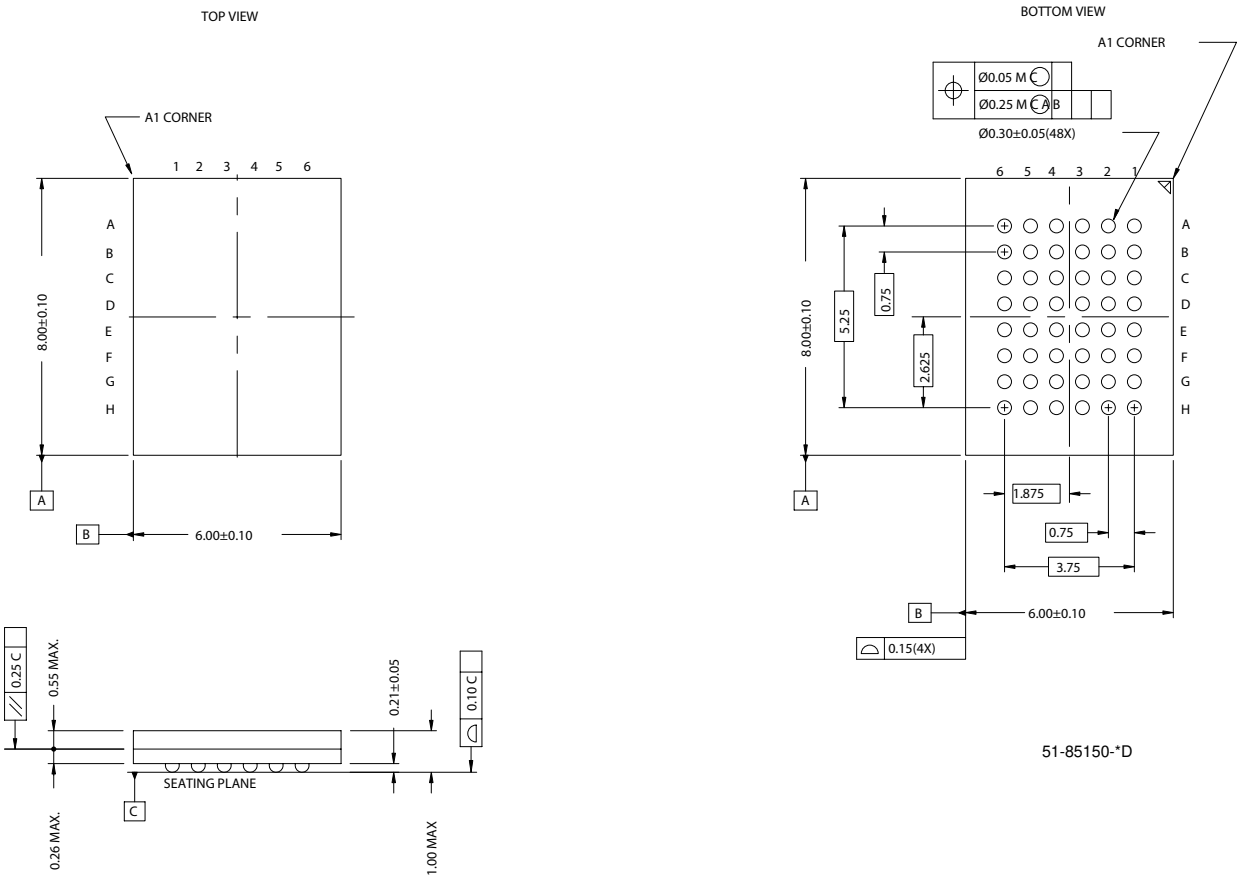
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CYK256K16MCCBU-55BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
	CYK256K16MCBU-55BVXI		48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm) (Pb-Free)	
60	CYK256K16MCCBU-60BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
70	CYK256K16MCCBU-70BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
	CYK256K16MCBU-70BVXI		48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm) (Pb-Free)	

Note:
20. H = Logic HIGH, L = Logic LOW, X = Don't Care.

Package Diagram

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



Document History Page

Document Title: CYK256K16MCCB MoBL3™4-Mbit (256K x 16) Pseudo Static RAM Document Number: 38-05585				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	223482	See ECN	REF	New data sheet
*A	234474	See ECN	SYT	Changed ball E3 on package pinout from NC to DNU
*B	260330	See ECN	PCI	Changed from preliminary to final
*C	298651	See ECN	PCI	Added 60-ns speed bin
*D	314013	See ECN	RKF	Added Pb-Free parts to the Ordering information
*E	397852	See ECN	SYT	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Changed typo in ordering code from CYK256K16MCCB to CYK256K16MCCBU in the “Ordering Information” on Page#8 Updated the revision of package diagram of Spec 51-85150 from *B to *D
*F	522566	See ECN	NXR	Changed V_{IL} Max spec from 0.4 V to 0.6 V in DC Electrical Characteristics table