

N-Channel Enhancement Mode Field Effect Transistor

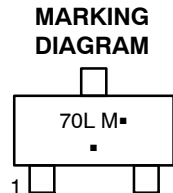
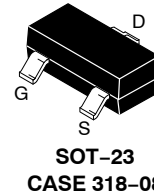
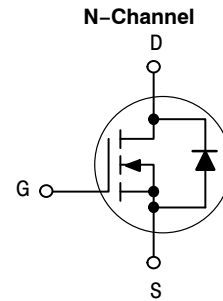
2N7002L

Description

This N-channel enhancement mode field effect transistor is produced using high cell density, trench MOSFET technology. This product minimizes on-state resistance while providing rugged, reliable and fast switching performance. This product is particularly suited for low-voltage, low-current applications such as small servo motor control, power MOSFET gate drivers, logic level translator, high speed line drivers, power management/power supply, and switching applications.

Features

- High Density Cell Design for Low $R_{DS(ON)}$
- Voltage Controlled Small Signal Switch
- Rugged and Reliable
- High Saturation Current Capability
- Very Low Capacitance
- Fast Switching Speed
- This Device is Pb-Free and Halogen Free



70L = Device Code
M = Date Code*
▪ = Pb-Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
2N7002L	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2N7002L

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain–Source Voltage	60	V
V _{DGR}	Drain–Gate Voltage (R _{GS} ≤ 1.0 MΩ)	60	V
V _{GSS}	Gate–Source Voltage – Continuous – Non Repetitive (t _p < 50 μs)	±20 ±40	V
I _D	Maximum Drain Current – Continuous – Pulsed	115 800	mA
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Note 1)

Symbol	Parameter	Value	Unit
P _D	Maximum Power Dissipation	200	mW
	Derate Above 25°C	1.6	mW/°C
R _{θJA}	Thermal Resistance, Junction–to–Ambient	380	°C/W

ESD RATING (Note 2)

Symbol	Parameter	Value	Unit
HBM	Human Body Model per ANSI/ESDA/JEDEC JS-001–2012	50	V
CDM	Charged Device Model per JEDEC C101C	>2000	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 10 μA	60.0	65.2	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 60 V, V _{GS} = 0 V	–	0.024	1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 125°C	–	0.080	500	
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	0.107	100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –20 V, V _{DS} = 0 V	–	–0.037	–100	nA

ON CHARACTERISTICS (Note 3)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.80	1.81	2.50	V
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 500 mA	–	3.35	7.50	Ω
		V _{GS} = 10 V, I _D = 500 mA, T _J = 100°C	–	5.62	13.50	
		V _{GS} = 5 V, I _D = 50 mA	–	2.68	7.50	
		V _{GS} = 5 V, I _D = 50 mA, T _J = 100°C	–	3.97	13.50	
V _{DS(ON)}	Drain–Source On–Voltage	V _{GS} = 10 V, I _D = 500 mA	–	1.68	3.75	V
		V _{GS} = 5 V, I _D = 50 mA	–	0.13	1.50	
I _{D(ON)}	On–State Drain Current	V _{GS} = 10 V, V _{DS} ≥ 2 V _{DS(ON)}	500	557	–	mA
		V _{GS} = 4.5 V, V _{DS} = 10 V	75	571	–	

2N7002L

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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ON CHARACTERISTICS (Note 3)

g_{FS}	Forward Trans-conductance	$V_{DS} \geq 2 V_{DS(ON)}$, $I_D = 200 \text{ mA}$	80	214	–	mS
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DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	–	12.8	50	pF
C_{oss}	Output Capacitance		–	3.25	25	
C_{rss}	Reverse Transfer Capacitance		–	1.52	5	
R_G	Gate Resistance	$V_{GS} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	–	22.2	–	Ω

SWITCHING CHARACTERISTICS (Note 3)

t_{on}	Turn-On Time	$V_{DD} = 30 \text{ V}$, $R_L = 150 \Omega$, $I_D = 200 \text{ mA}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = 25 \Omega$	–	4.35	20	ns
t_{off}	Turn-Off Time		–	15.6	20	ns

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current		–	–	115	mA
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		–	–	0.8	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = 115 \text{ mA}$ (Note 3)	–	0.818	1.5	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- 380°C/W when mounted on a minimum pad.

- ESD values are in typical, no over-voltage rating is implied, ESD CDM zap voltage is 2000 V maximum.
- Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2.0\%$.

TYPICAL CHARACTERISTICS

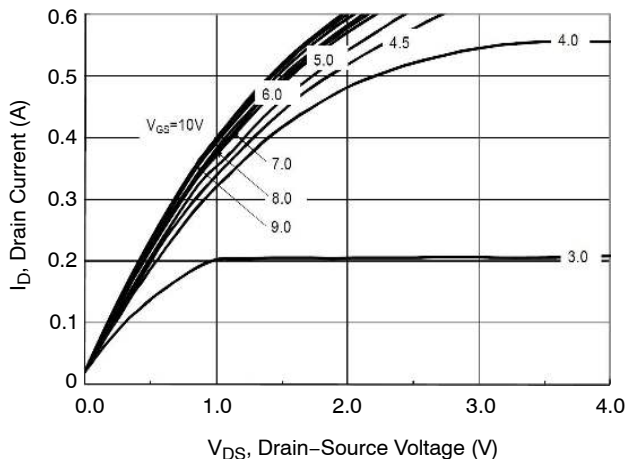


Figure 1. On-Region Characteristics

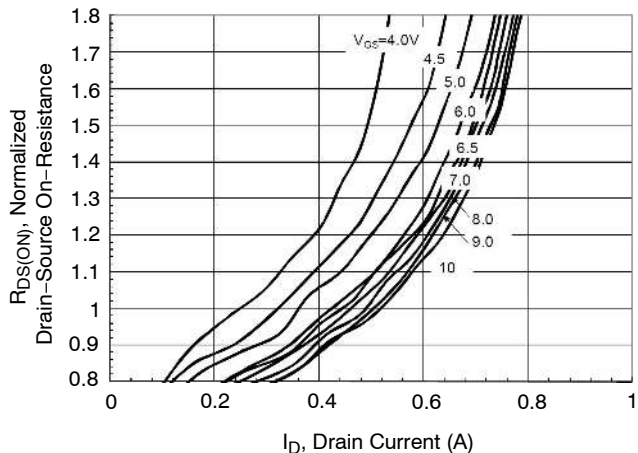


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

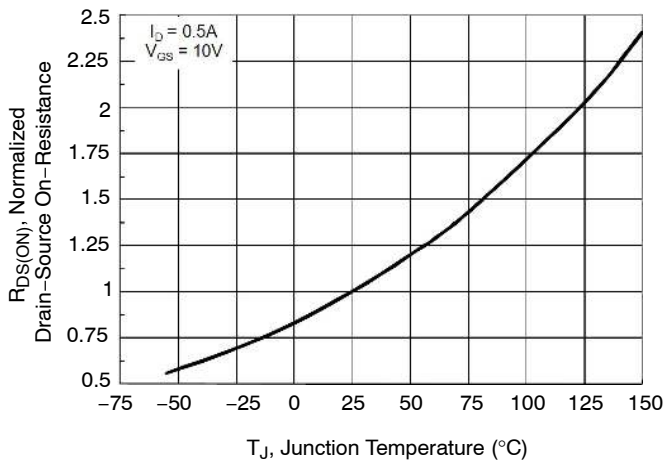


Figure 3. On-Resistance Variation with Temperature

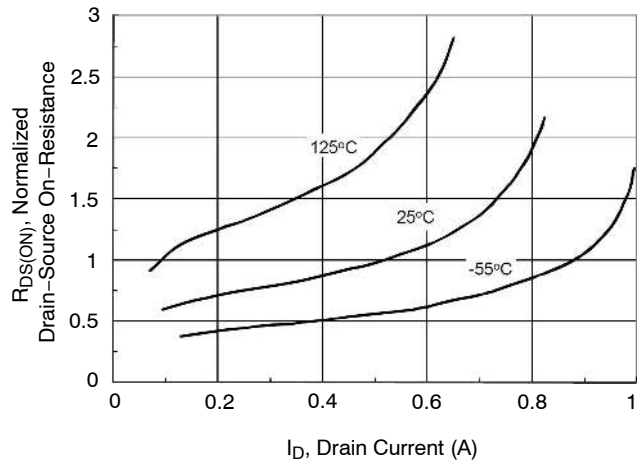


Figure 4. On-Resistance Variation with Drain Current and Temperature

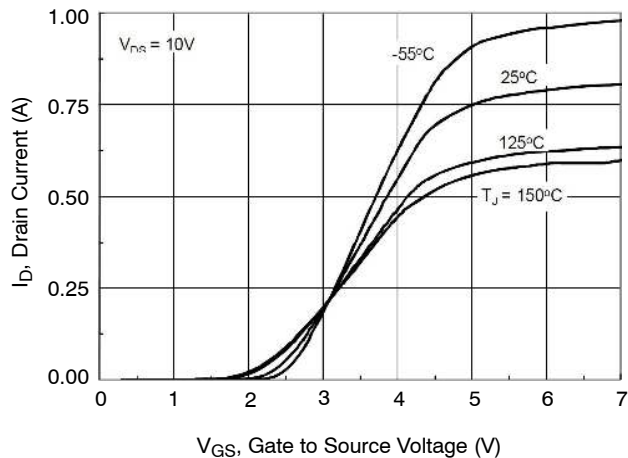


Figure 5. Transfer Characteristics

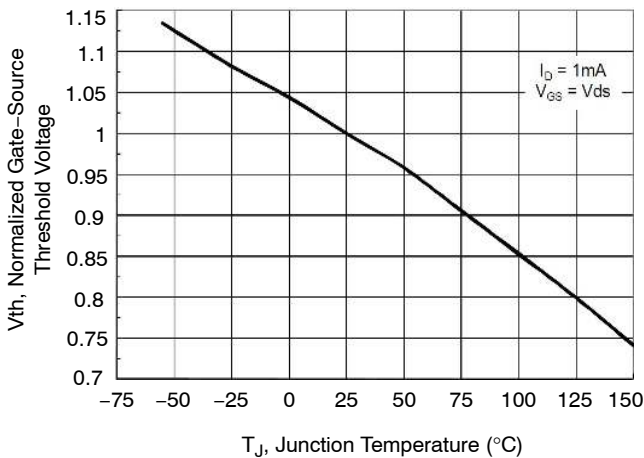


Figure 6. Gate Threshold Variation with Temperature

TYPICAL CHARACTERISTICS (continued)

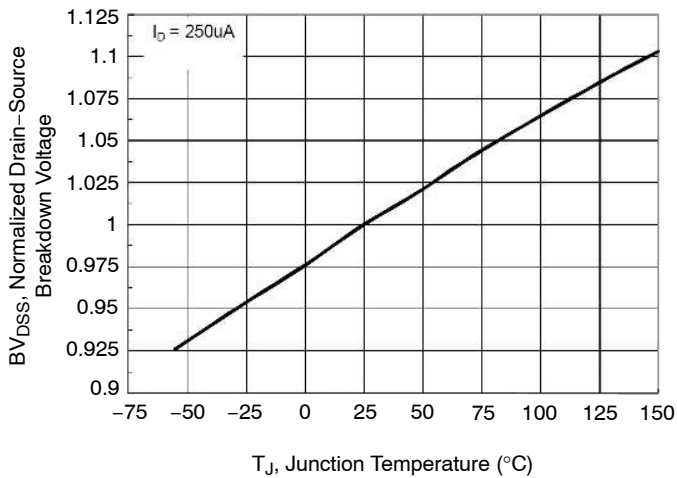


Figure 7. Breakdown Voltage Variation with Temperature

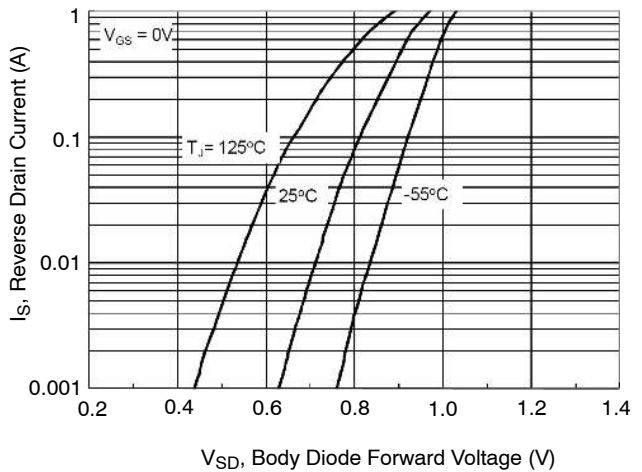


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

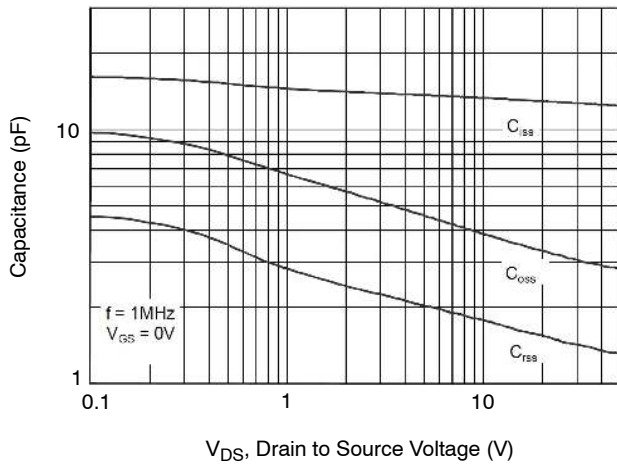


Figure 9. Capacitance Characteristics

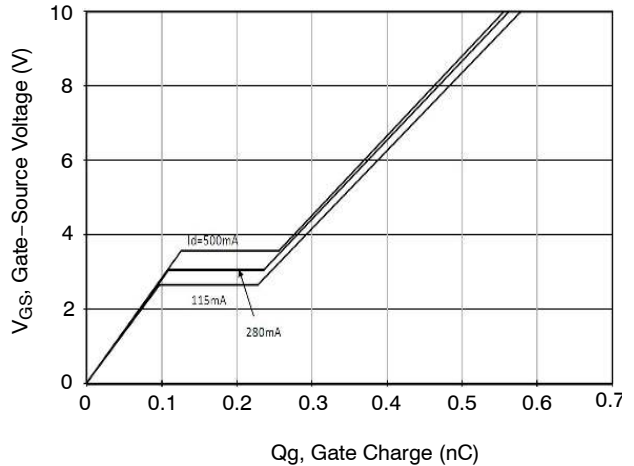


Figure 10. Gate Charge Characteristics

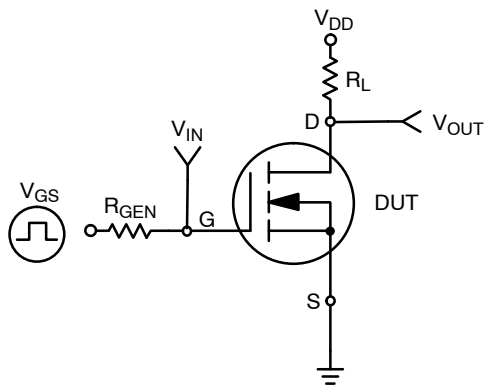


Figure 11.

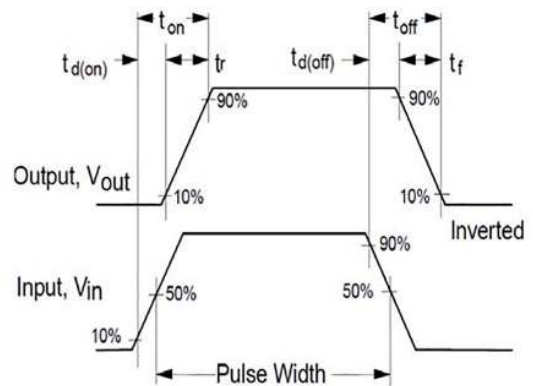


Figure 12. Switching Waveforms

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TYPICAL CHARACTERISTICS (continued)

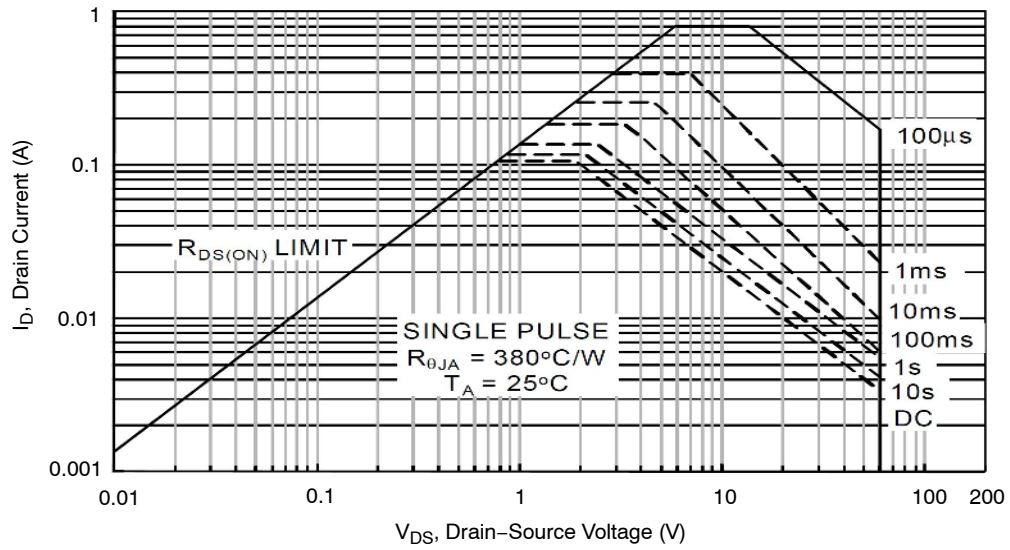


Figure 13. Maximum Safe Operating Area

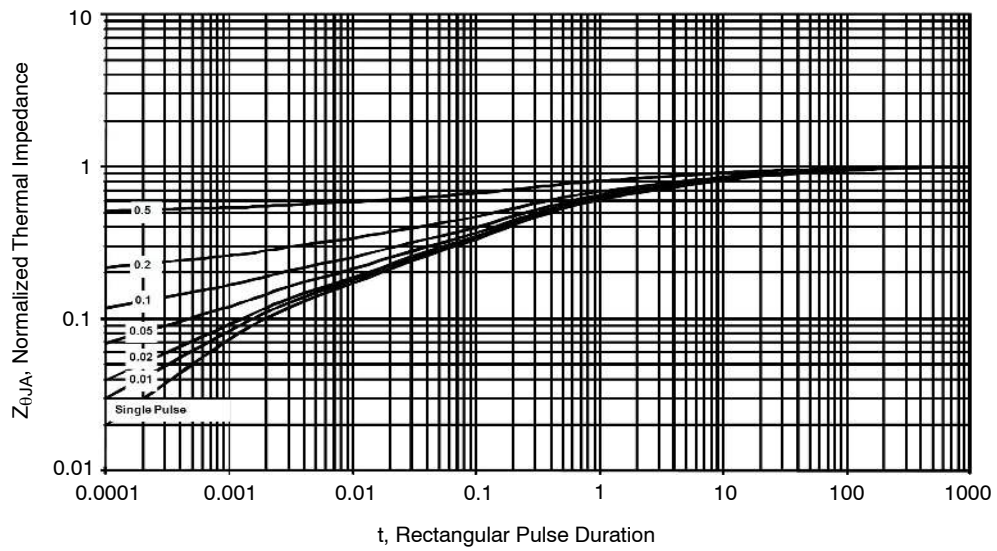
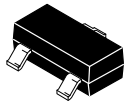


Figure 14. Transient Thermal Response Curve

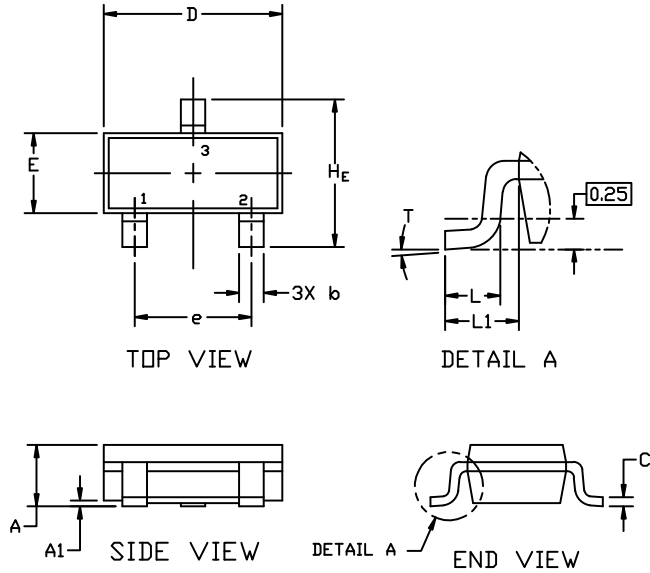
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23 (TO-236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

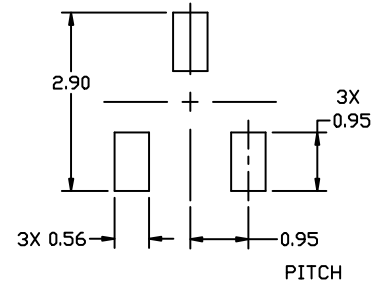
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H _E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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