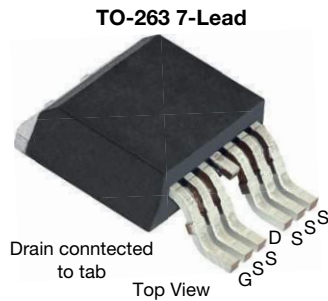


N-Channel 100 V (D-S) MOSFET



FEATURES

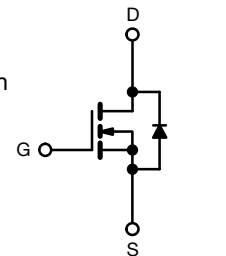
- TrenchFET® power MOSFET
- Maximum 175 °C junction temperature
- Very low Q_{gd} reduces power loss from passing through $V_{plateau}$
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power supply
- Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management
- OR-ing / e-fuse



N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0035
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.0037
Q_g typ. (nC)	142.4
I_D (A) ^d	150
Configuration	Single

ORDERING INFORMATION

Package	D ² PAK (TO-263-7L)
Lead (Pb)-free and halogen-free	SUM70030M-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	100	V	
Gate-source voltage	V_{GS}	± 20		
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	150 ^d	
		$T_C = 70$ °C	150 ^d	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	500	A	
Avalanche current	I_{AS}	60		
Single avalanche energy ^a	E_{AS}	L = 0.1 mH	180	mJ
Maximum power dissipation ^a		$T_C = 25$ °C	375 ^b	
		$T_C = 125$ °C	125 ^b	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient (PCB mount) ^c	R_{thJA}	40	°C/W
Junction-to-case (drain)	R_{thJC}	0.4	

Notes

- Duty cycle ≤ 1 %
- See SOA curve for voltage derating
- When mounted on 1" square PCB (FR4 material)
- Package limited



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 250	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	150	μA
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	5	mA
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}$, $V_{GS} = 10\text{ V}$	120	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$	-	0.0029	0.0035	Ω
		$V_{GS} = 7.5\text{ V}$, $I_D = 20\text{ A}$	-	0.0031	0.0037	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 30\text{ A}$	-	110	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$	-	10 870	-	μF
Output capacitance	C_{oss}		-	820	-	
Reverse transfer capacitance	C_{rss}		-	40	-	
Total gate charge ^c	Q_g	$V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	-	142.4	214	nC
Gate-source charge ^c	Q_{gs}		-	46.8	-	
Gate-drain charge ^c	Q_{gd}		-	18.5	-	
Output charge	Q_{oss}	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$	-	138	207	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.34	1.7	3.4	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}$, $R_L = 3\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	-	30	60	ns
Rise time ^c	t_r		-	13	26	
Turn-off delay time ^c	$t_{d(off)}$		-	50	100	
Fall time ^c	t_f		-	15	30	
Drain-Source Body Diode Ratings and Characteristics ^b ($T_C = 25\text{ }^\circ\text{C}$)						
Pulsed current ($t = 100\text{ }\mu\text{s}$)	I_{SM}		-	-	250	A
Forward voltage ^a	V_{SD}	$I_F = 10\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.8	1.5	V
Reverse recovery time	t_{rr}	$I_F = 34\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	76	150	ns
Peak reverse recovery charge	$I_{RM(REC)}$		-	4.6	5.6	A
Reverse recovery charge	Q_{rr}		-	0.205	0.24	μC
Reverse recovery fall time	t_a		-	52	-	ns
Reverse recovery rise time	t_b		-	24	-	

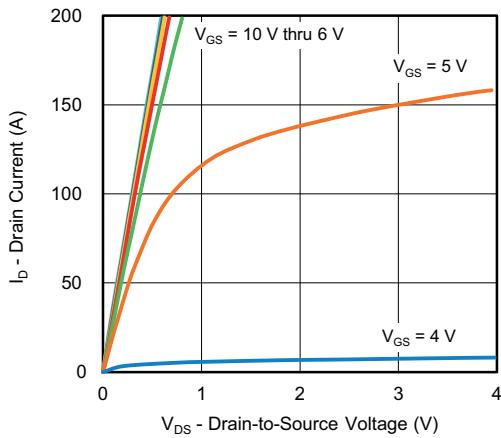
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

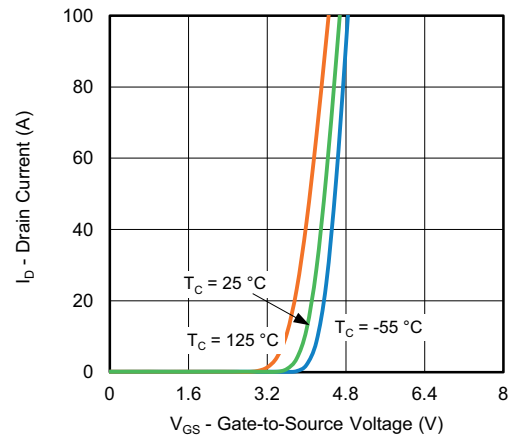
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



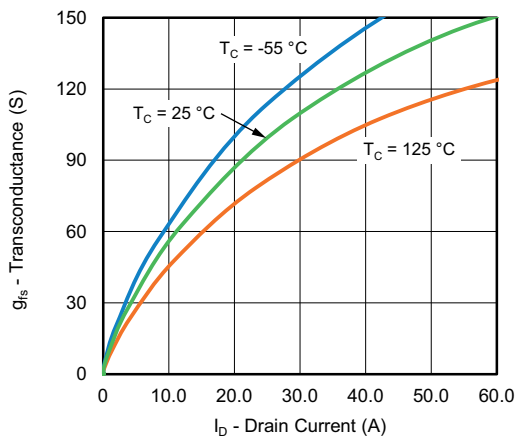
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



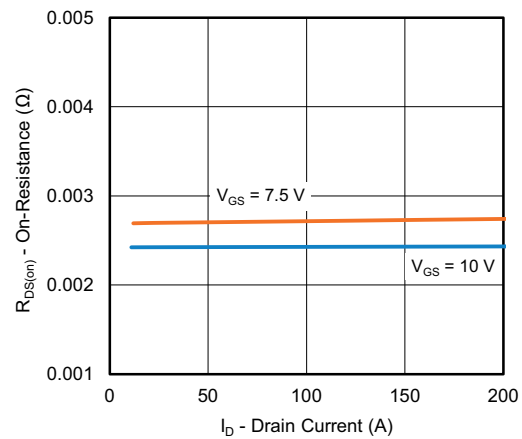
Output Characteristics



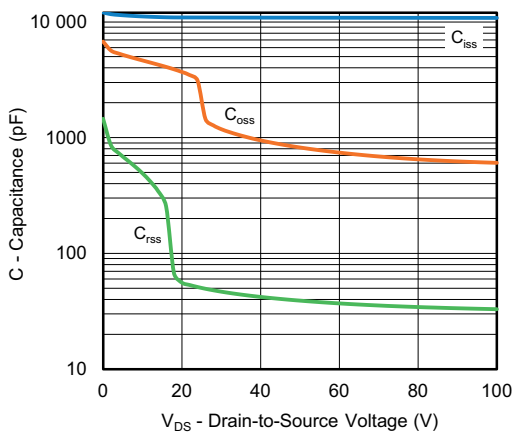
Transfer Characteristics



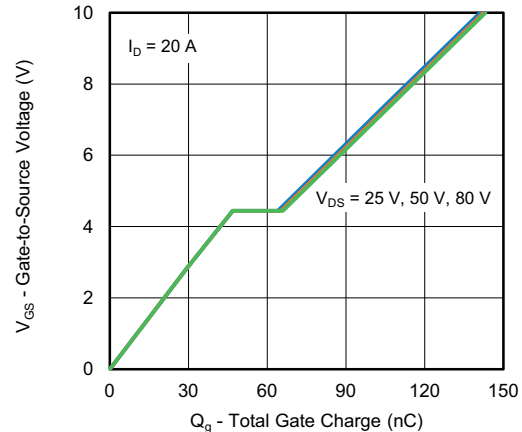
Transconductance



On-Resistance vs. Drain Current



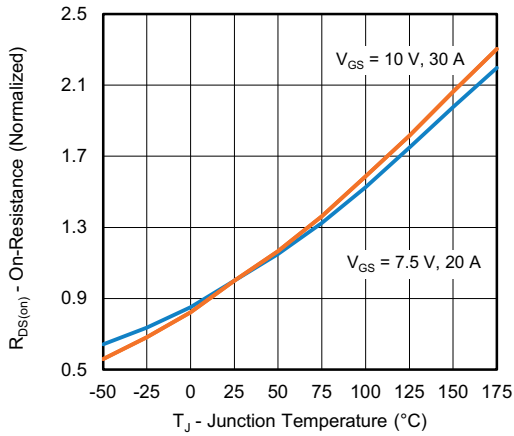
Capacitance



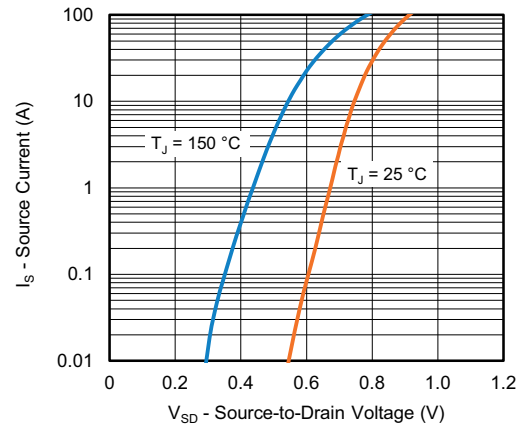
Gate Charge



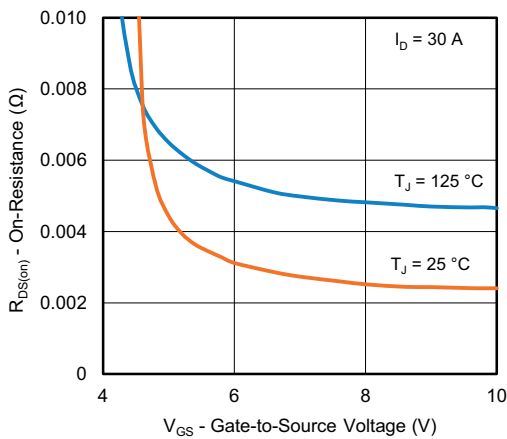
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



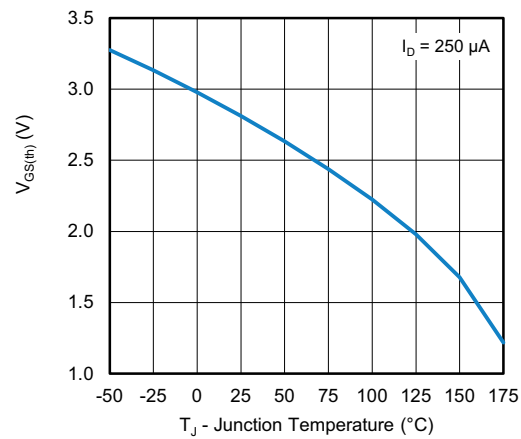
On-Resistance vs. Junction Temperature



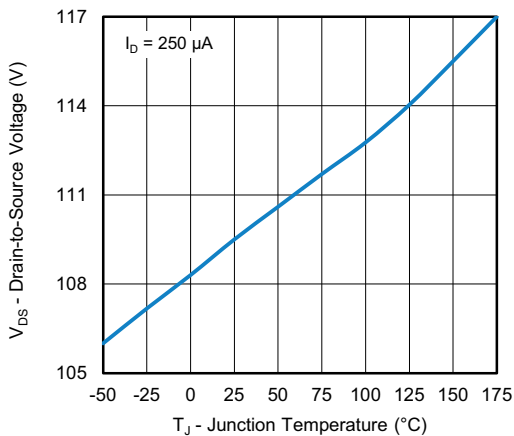
Source Drain Diode Forward Voltage



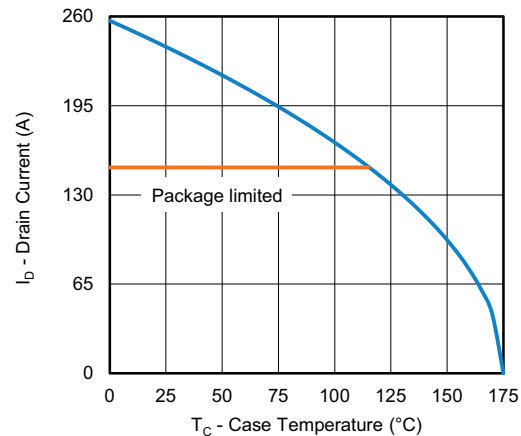
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



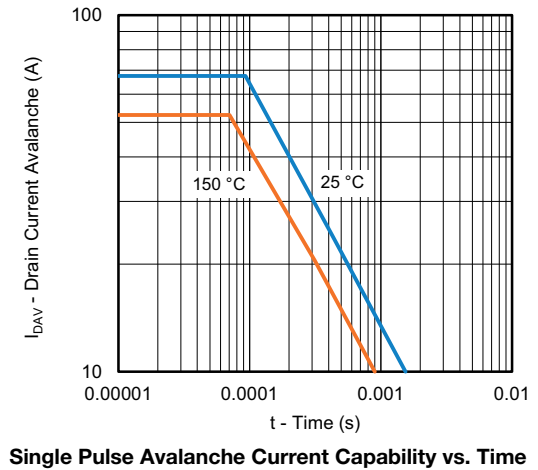
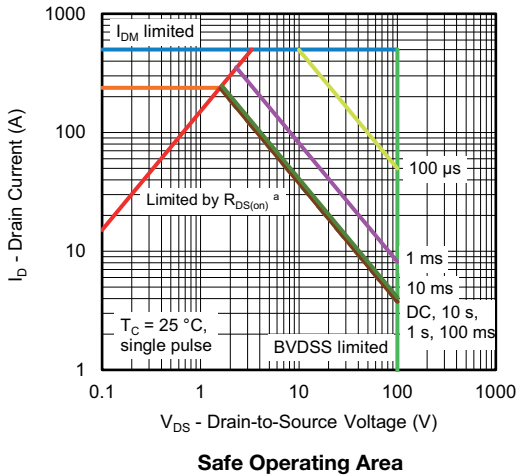
Drain Source Breakdown vs. Junction Temperature



Current Derating

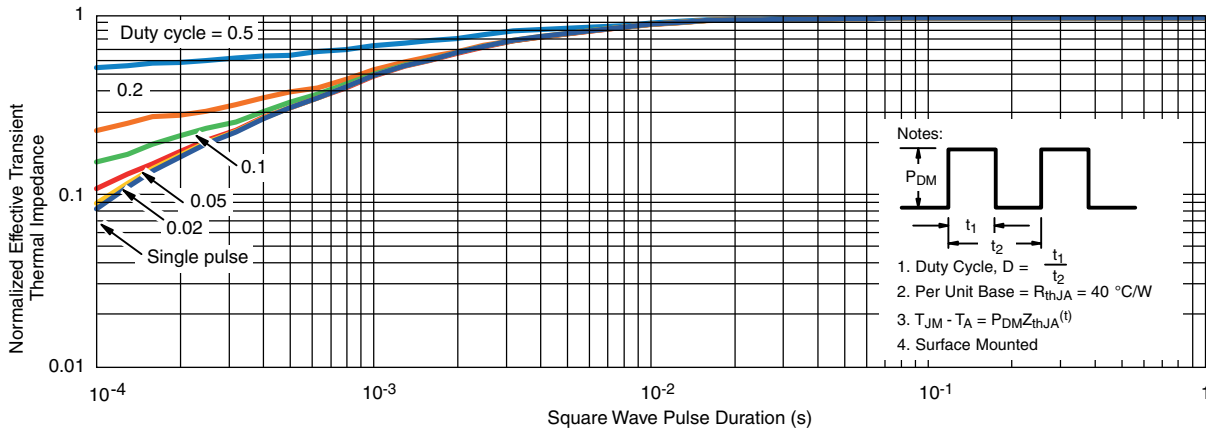


THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$

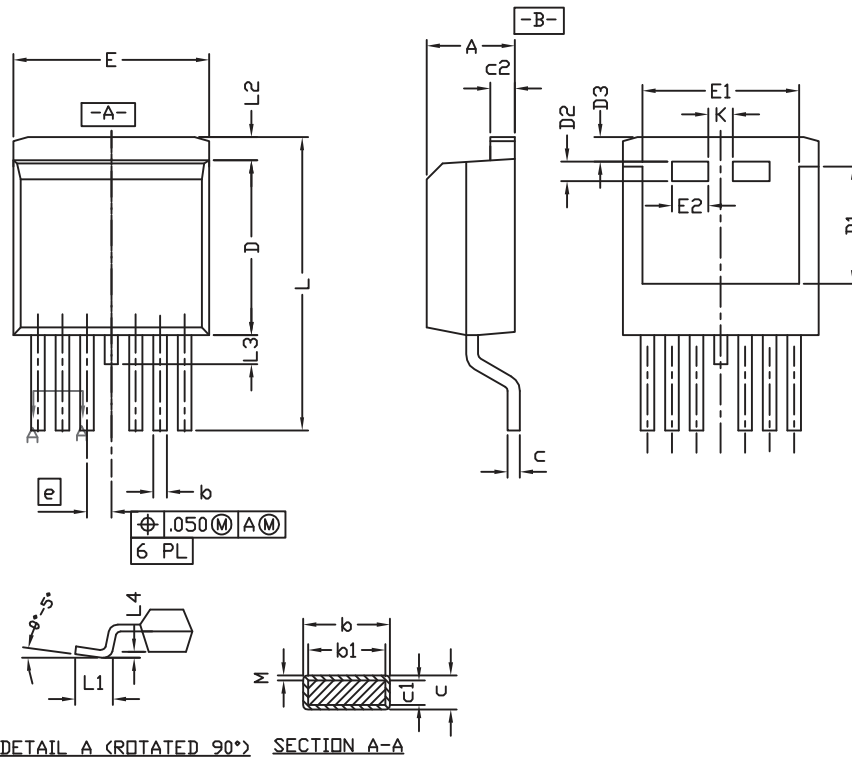


Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction to Case ($25\text{ }^\circ\text{C}$)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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D²PAK (TO-263-7L) Case Outline

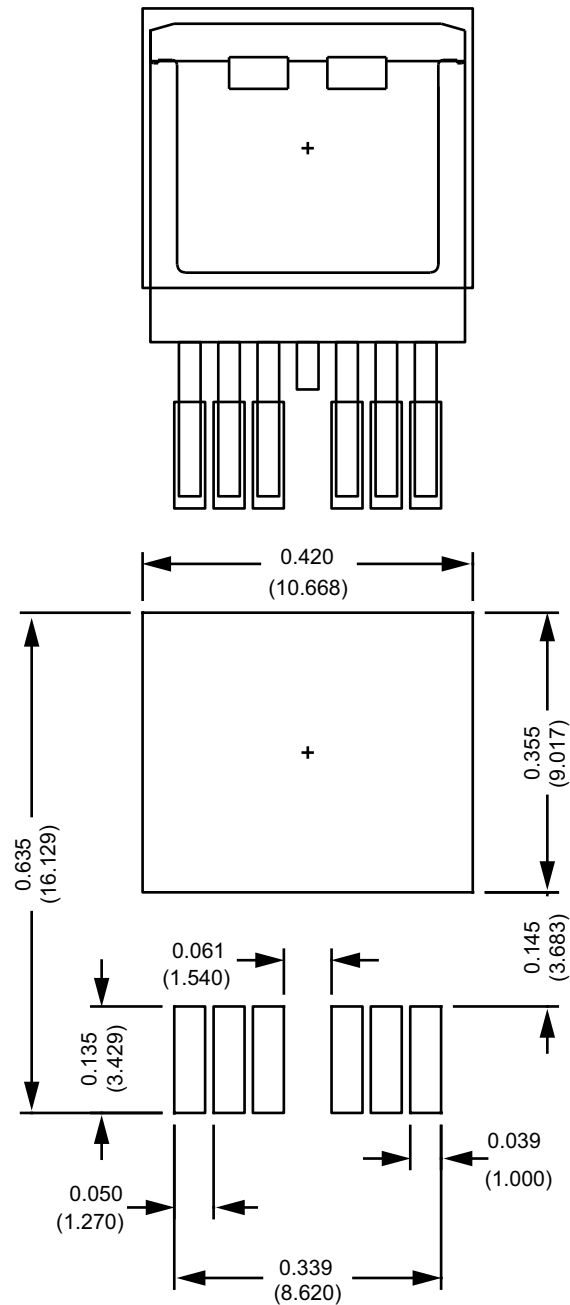

Notes

1. Plane B includes maximum features of heat sink tab and plastic
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils
3. Pin to pin coplanarity max. 4 mils
4. Lead thickness 25 mils
5. For SUM part numbers lead thickness is 24 mils to 29 mils
6. For reference only
7. Use inches as the primary measurement
8. This feature is only for SUM

DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.064	4.826
b	0.020	0.039	0.508	0.990
b1	0.020	0.035	0.508	0.889
c* SUB	0.012	0.018	0.305	0.457
c* SUM	0.022	0.028	0.559	0.711
c1	0.018	0.025	0.457	0.635
c2	0.045	0.055	1.143	1.397
D	0.340	0.380	8.636	9.652
D1	0.260	0.280	6.604	7.112
D2	0.046	0.050	1.168	1.270
D3	0.045	0.055	1.143	1.397
E	0.380	0.410	9.652	10.414
E1	0.245	-	6.223	-
E2	0.072	0.078	1.829	1.981
e	0.050 BSC		1.27 BSC	
K	0.045	0.055	1.143	1.397
L	0.575	0.625	14.605	15.875
L1	0.090	0.110	2.286	2.794
L2	0.040	0.055	1.016	1.397
L3	0.050	0.070	1.270	1.778
L4	0.010 BSC		0.254 BSC	
M	-	0.002	-	0.050
ECN: T22-0410-Rev. D, 19-Sep-2022				
DWG: 6006				



Recommended Land Pattern D²PAK (TO-263-7L)





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