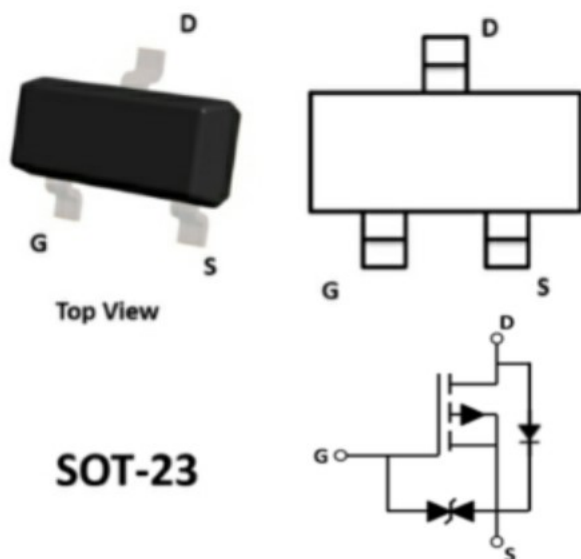


## P-Channel Enhancement Mode Field Effect Transistor



SOT-23

### Product Summary

- $V_{DS}$  -20V
- $I_D$  -5.6A
- $R_{DS(ON)}$ ( at  $V_{GS}=-4.5V$ ) <42 mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-2.5V$ ) <55 mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-1.8V$ ) <100 mohm
- ESD Protected Up to 4.0KV (HBM)

### General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Load switch
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	$V_{DS}$	-20	V
Gate-source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current	$I_D$	$T_A=25^\circ\text{C}$ Steady State	-5.6
		$T_A=70^\circ\text{C}$ Steady State	-4.5
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-23	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$ Steady State	$P_D$	1.3	W
Thermal Resistance Junction-to-Ambient @ Steady State <sup>B</sup>	$R_{\theta JA}$	96	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3415A	F2	3415.	3000	30000	120000	7" reel

# YJL3415A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V		±2.5	±10	μA
		V <sub>GS</sub> = ±8V, V <sub>DS</sub> =0V		±900	±2000	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.40	-0.62	-1.0	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-5.6A		29	42	mΩ
		V <sub>GS</sub> = -2.5V, I <sub>D</sub> =-4.3A		36	55	
		V <sub>GS</sub> = -1.8V, I <sub>D</sub> =-2.0A		55	100	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-5.6A, V <sub>GS</sub> =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				-5.6	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHZ		1010		pF
Output Capacitance	C <sub>oss</sub>			130		
Reverse Transfer Capacitance	C <sub>rss</sub>			109		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-4.5V, V <sub>DD</sub> =-10V, I <sub>D</sub> =-4A		10.98		nC
Gate Source Charge	Q <sub>gs</sub>			2.17		
Gate Drain Charge	Q <sub>gd</sub>			2.54		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-4A, di/dt=100A/us		4.38		
Reverse Recovery Time	t <sub>rr</sub>			24.8		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-4.5V, V <sub>DD</sub> =-10V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		8.4		ns
Turn-on Rise Time	t <sub>r</sub>			36.2		
Turn-off Delay Time	t <sub>D(off)</sub>			76.8		
Turn-off Fall Time	t <sub>f</sub>			56.2		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

## ■ Typical Performance Characteristics

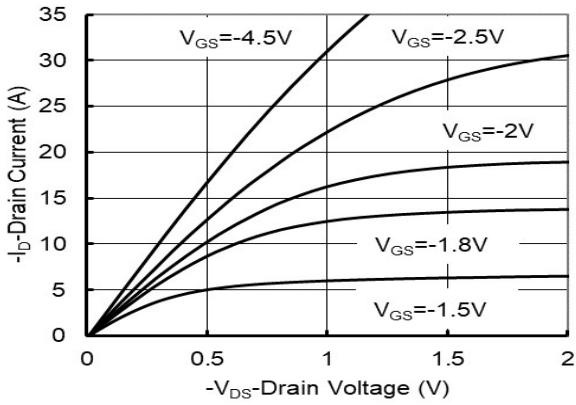


Figure1. Output Characteristics

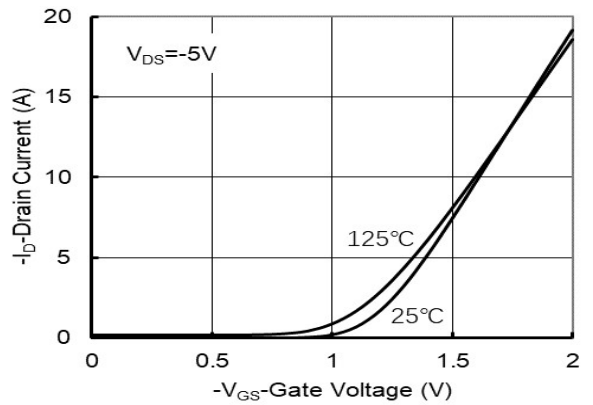


Figure2. Transfer Characteristics

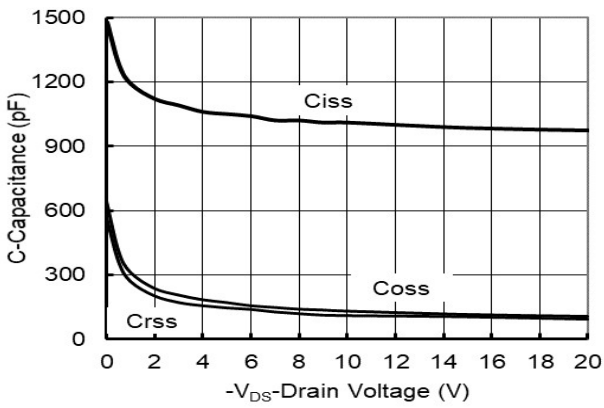


Figure3. Capacitance Characteristics

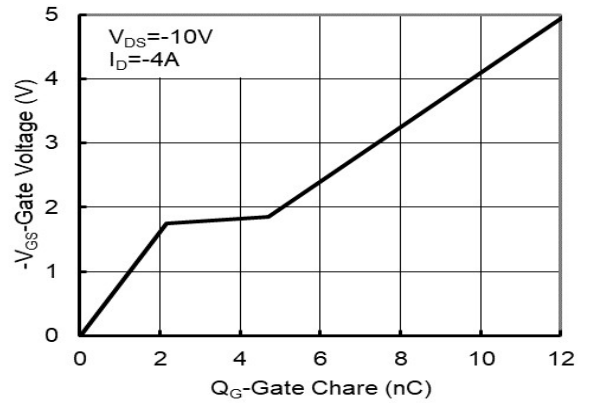


Figure4. Gate Charge

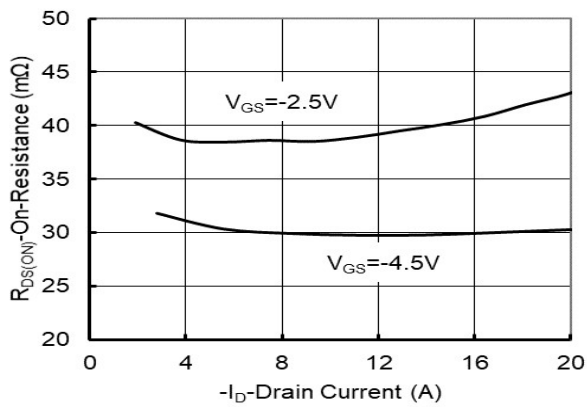


Figure5. Drain-Source on Resistance

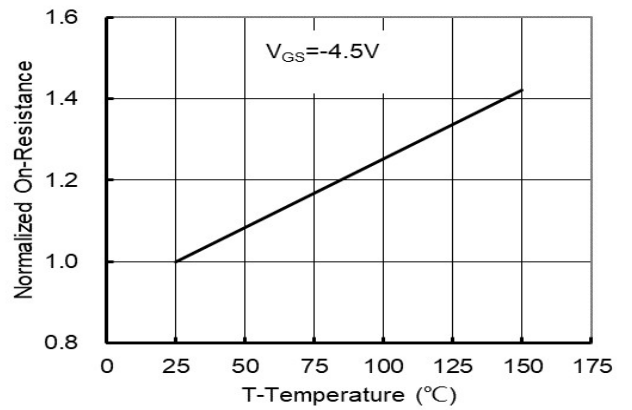


Figure6. Drain-Source on Resistance

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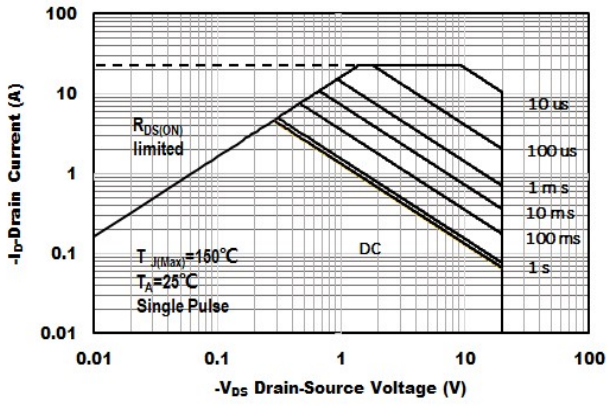


Figure7. Safe Operation Area

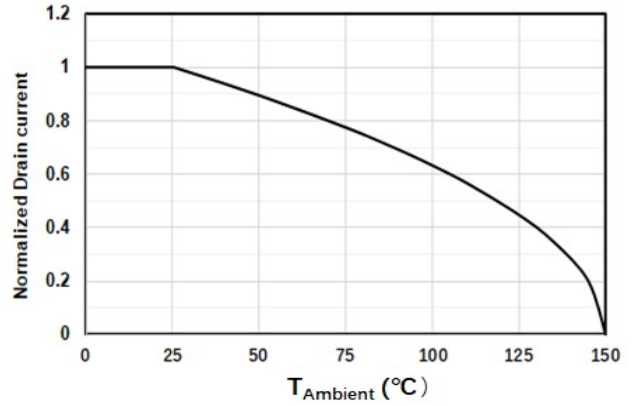


Figure8. Drain Current vs Ambient temperature

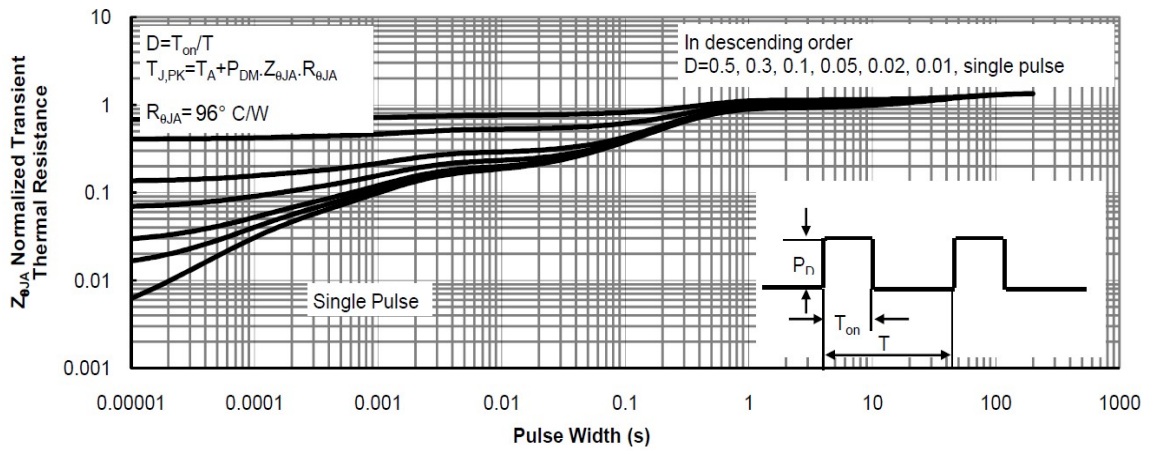
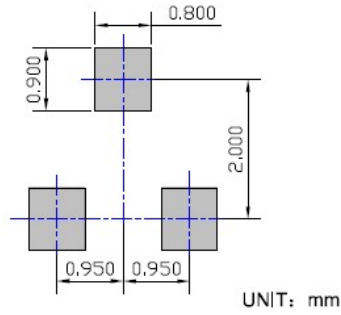
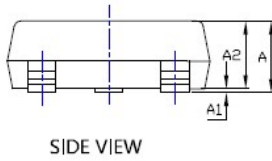
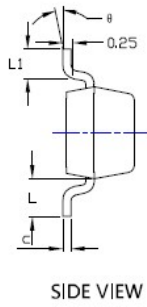
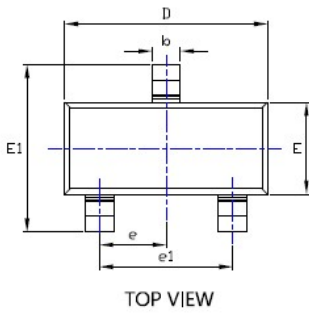


Figure9. Normalized Maximum Transient Thermal Impedance

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## ■ SOT-23 Package information



SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS					
	INCHES			MILLimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.035	---	0.045	0.900	---	1.150
A1	0.000	---	0.004	0.000	---	0.100
A2	0.035	0.038	0.041	0.900	0.975	1.050
b	0.012	0.016	0.020	0.300	0.400	0.500
c	0.004	---	0.008	0.100	---	0.200
D	0.110	0.114	0.118	2.800	2.900	3.000
E	0.047	0.051	0.055	1.200	1.300	1.400
E1	0.089	0.094	0.100	2.250	2.400	2.550
e	0.037 TYP			0.950 TYP		
e1	0.071	0.075	0.079	1.800	1.900	2.000
L	0.022 REF			0.550 REF		
L1	0.012	0.016	0.200	0.300	0.400	0.500
e	0*	---	8*	0*	---	8*

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

# YJL3415A

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