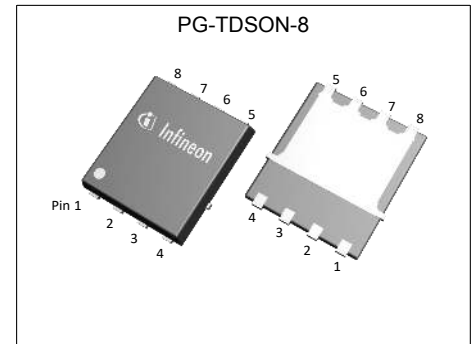


# MOSFET

## OptiMOS™5 Power-Transistor, 60 V

### Features

- Ideal for high-frequency switching
- Optimized for chargers
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Qualified for standard grade applications

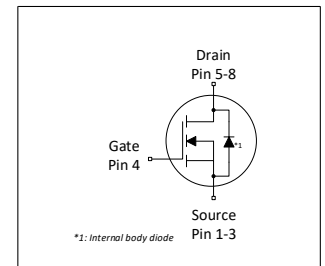


### Product validation

Qualified according to JEDEC Standard

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	6.9	m $\Omega$
$I_D$	57	A
$Q_{oss}$	15	nC
$Q_G(0V..4.5V)$	8.7	nC



Type / Ordering Code	Package	Marking	Related Links
ISC0703NLS	PG-TDSON-8	0703NL	-

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	57 40 13	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	228	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	13	mJ	$I_D=32\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	44 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}^2)$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	2.5	3.4	°C/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	°C/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	50	°C/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.1	1.6	2.3	V	$V_{DS}=V_{GS}$ , $I_D=15\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.8 7.6	6.9 8.9	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=32\text{ A}$ $V_{GS}=4.5\text{ V}$ , $I_D=16\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1.2	-	$\Omega$	-
Transconductance	$g_{fs}$	-	65	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=32\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	1100	1400	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	250	320	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	14	24	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	3.0	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=32\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Rise time	$t_r$	-	2.0	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=32\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	9.4	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=32\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Fall time	$t_f$	-	2.8	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=32\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	3.3	-	nC	$V_{DD}=30\text{ V}$ , $I_D=32\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	1.7	-	nC	$V_{DD}=30\text{ V}$ , $I_D=32\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	$Q_{gd}$	-	3.1	-	nC	$V_{DD}=30\text{ V}$ , $I_D=32\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	$Q_{sw}$	-	4.6	-	nC	$V_{DD}=30\text{ V}$ , $I_D=32\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	8.7	11	nC	$V_{DD}=30\text{ V}$ , $I_D=32\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.0	-	V	$V_{DD}=30\text{ V}$ , $I_D=32\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	17	23	nC	$V_{DD}=30\text{ V}$ , $I_D=32\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	15	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge	$Q_{oss}$	-	15	-	nC	$V_{DS}=30\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	41	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	228	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.88	1.1	V	$V_{GS}=0\text{ V}, I_F=32\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	28	-	ns	$V_R=30\text{ V}, I_F=32\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	21	-	nC	$V_R=30\text{ V}, I_F=32\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

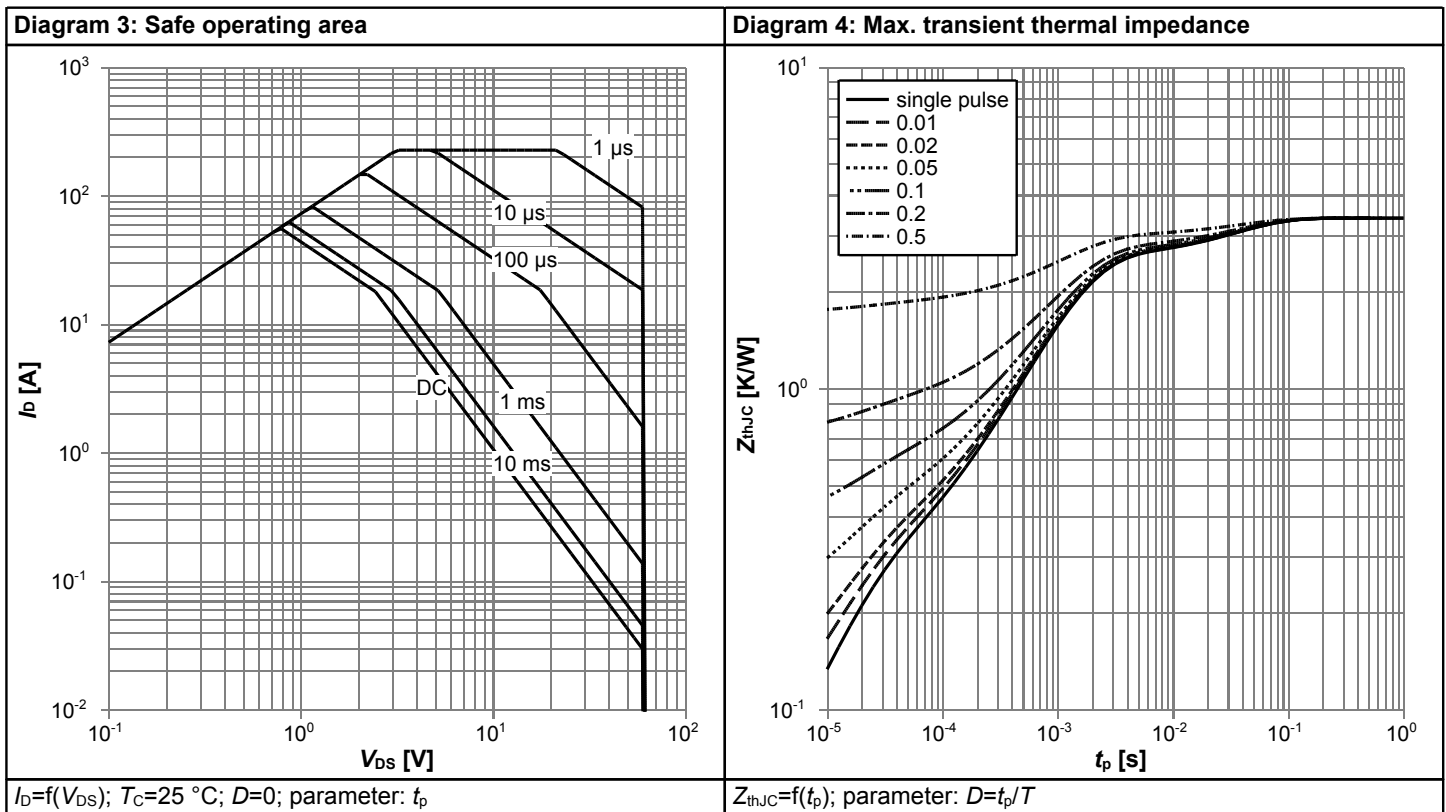
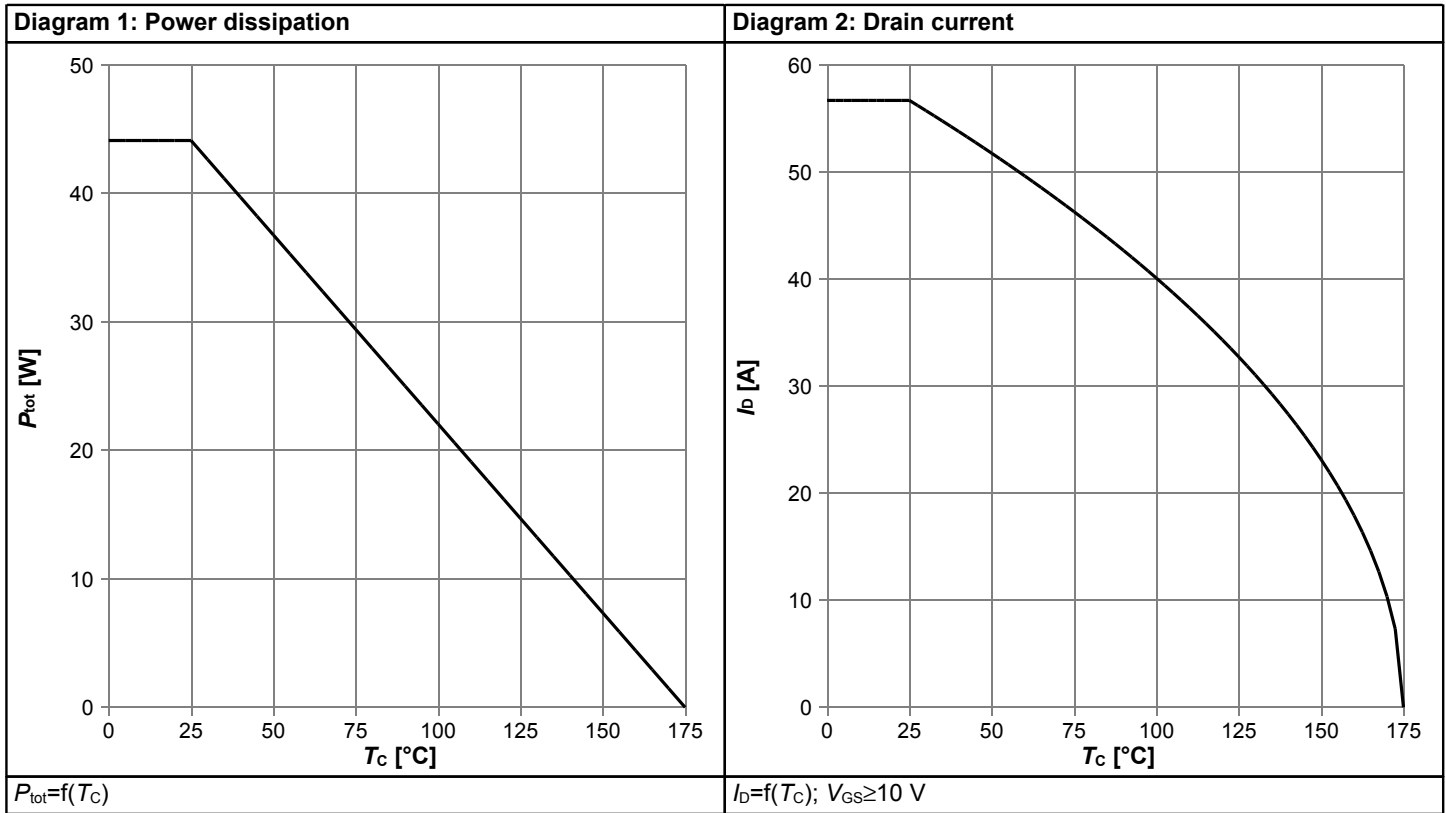
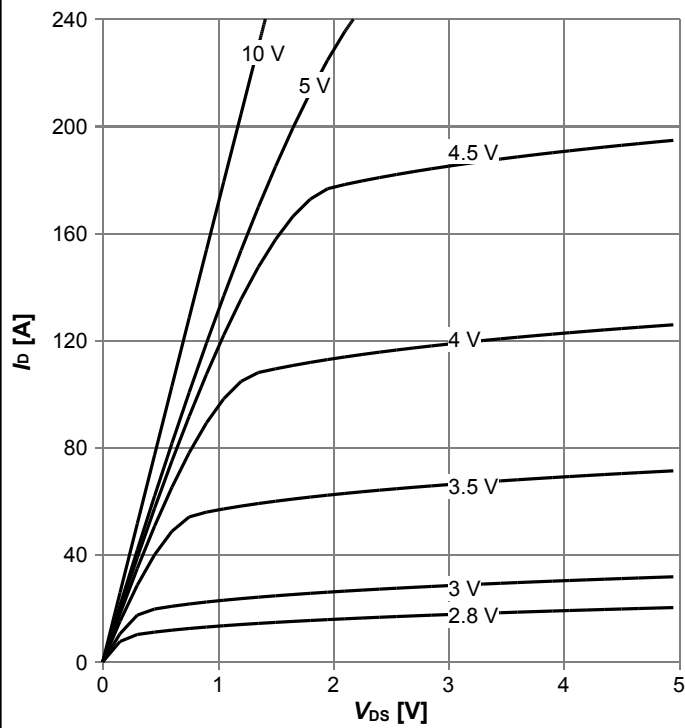
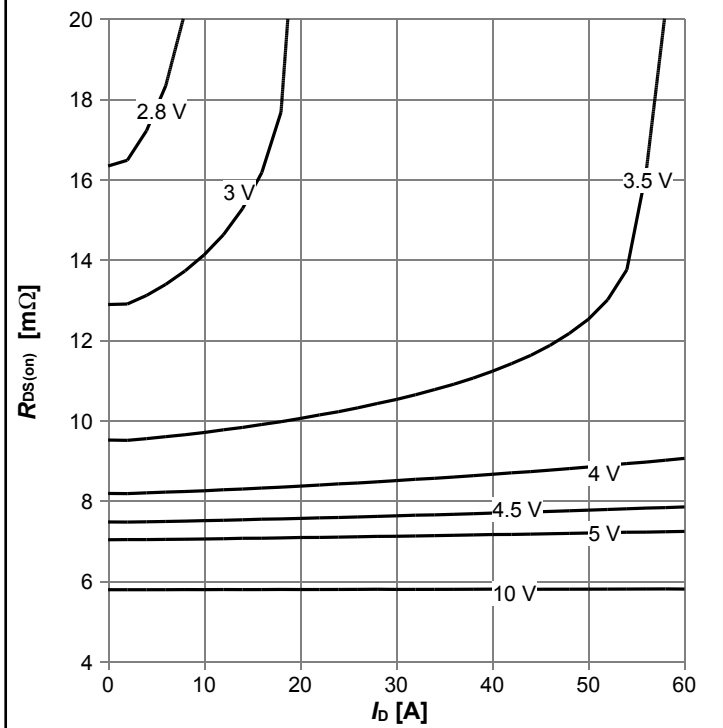


Diagram 5: Typ. output characteristics



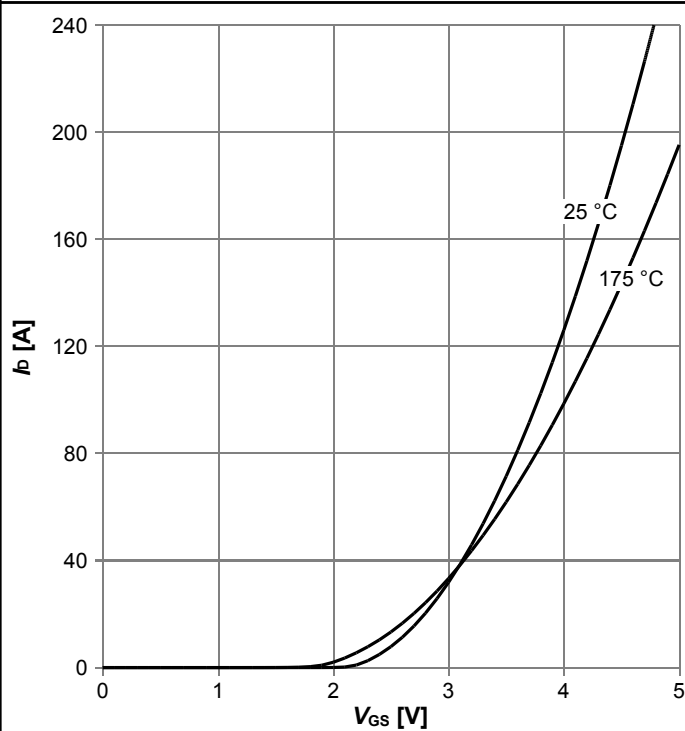
$I_D = f(V_{DS})$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



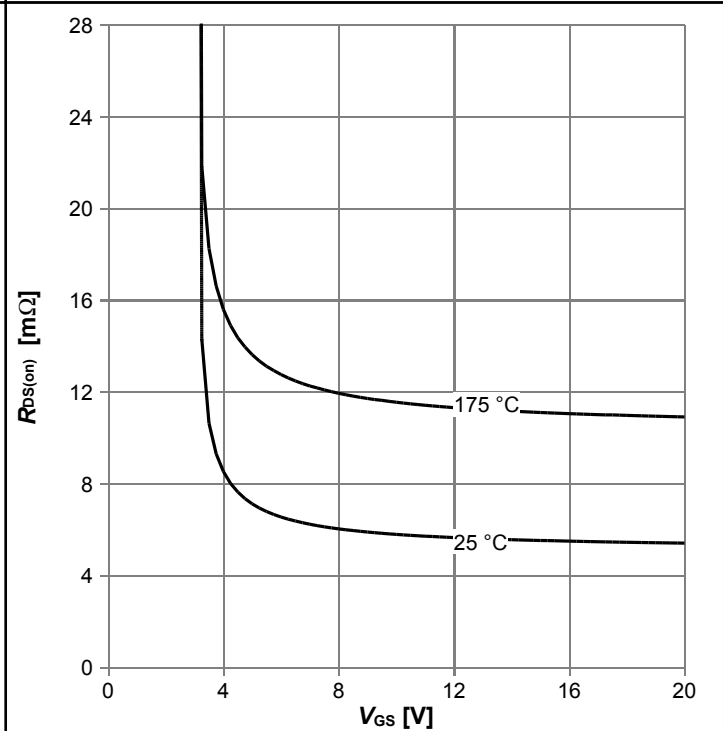
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



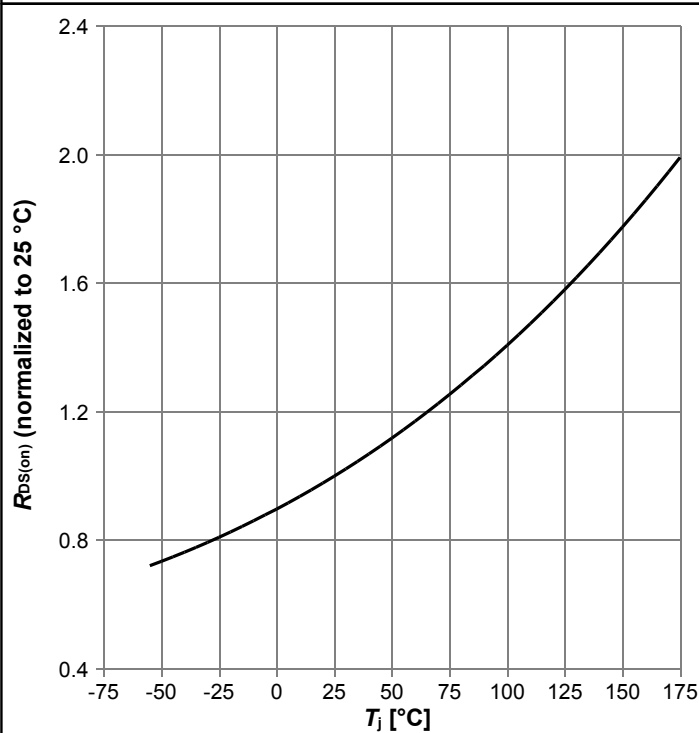
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

Diagram 8: Typ. drain-source on resistance



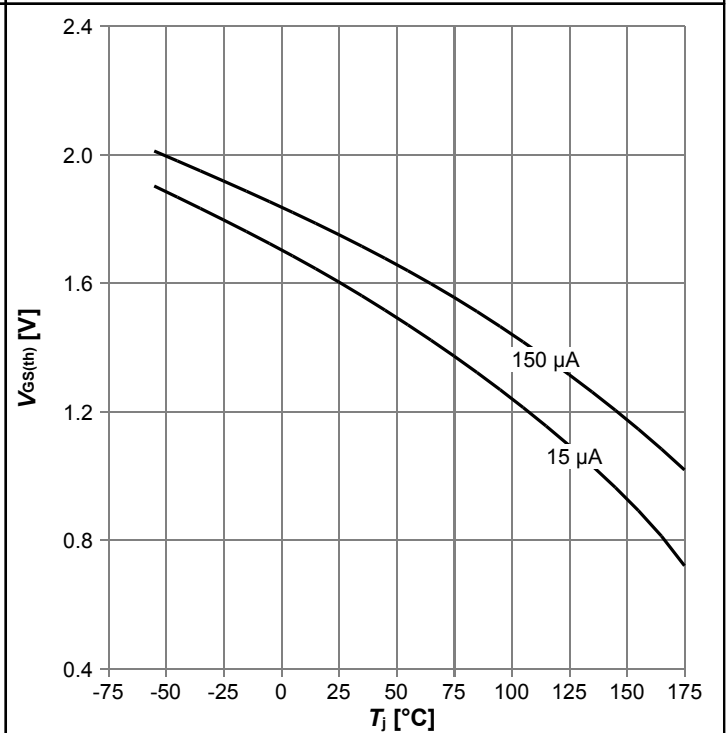
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 32\text{ A}$ ; parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



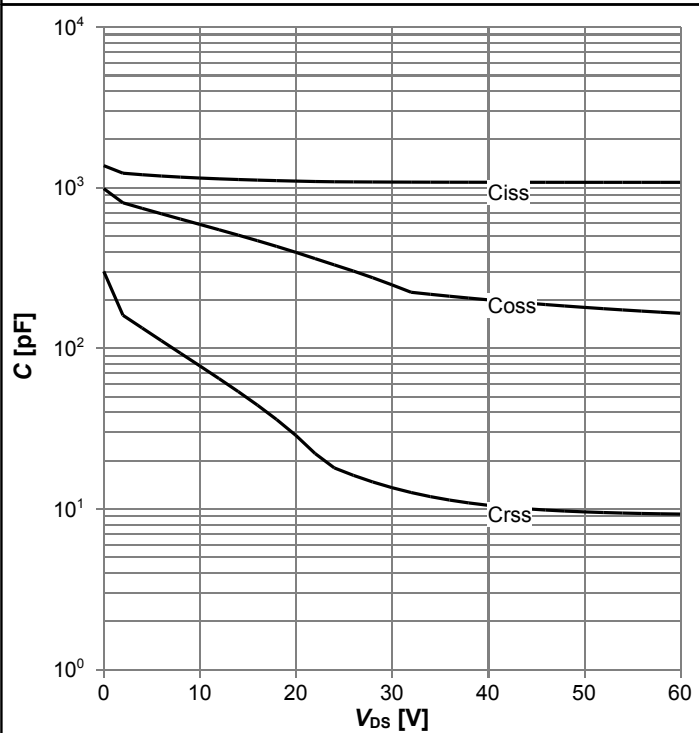
$R_{DS(on)}=f(T_j)$ ,  $I_D=32$  A,  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



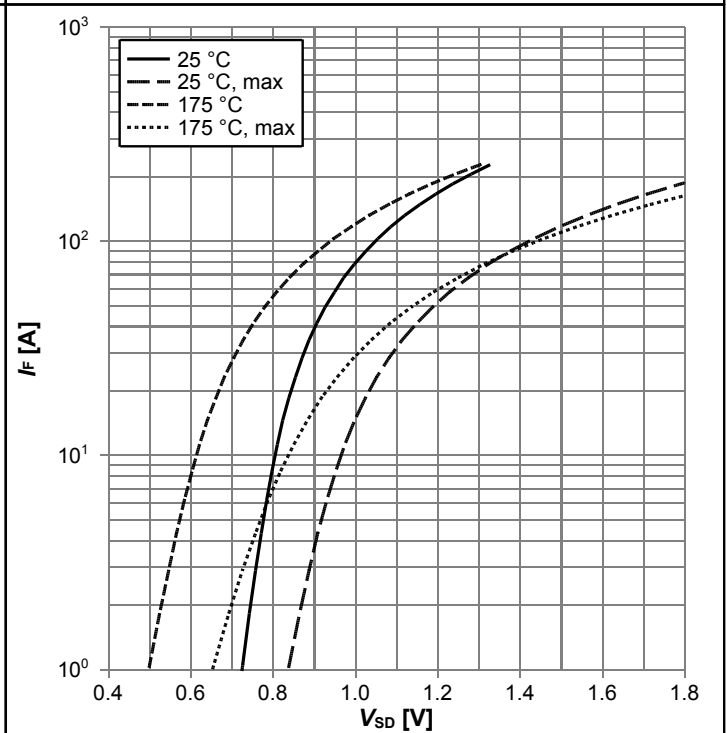
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

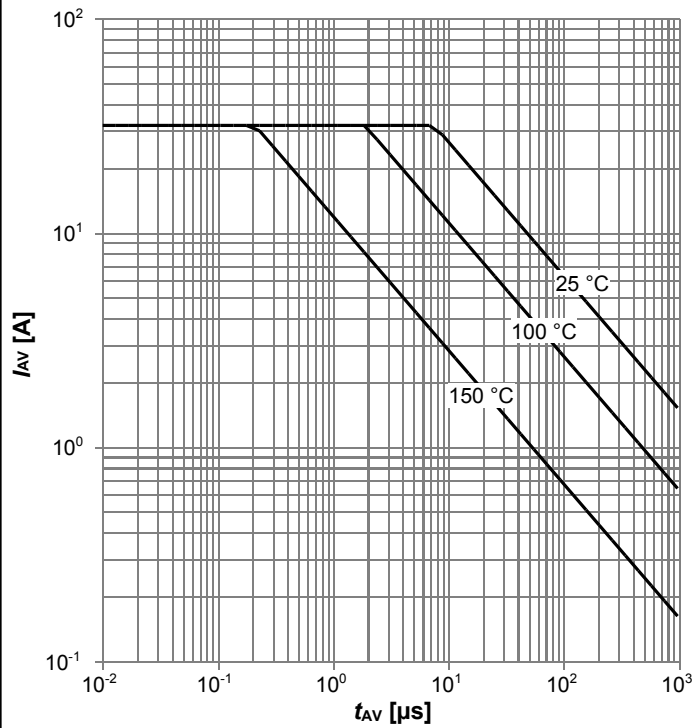
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

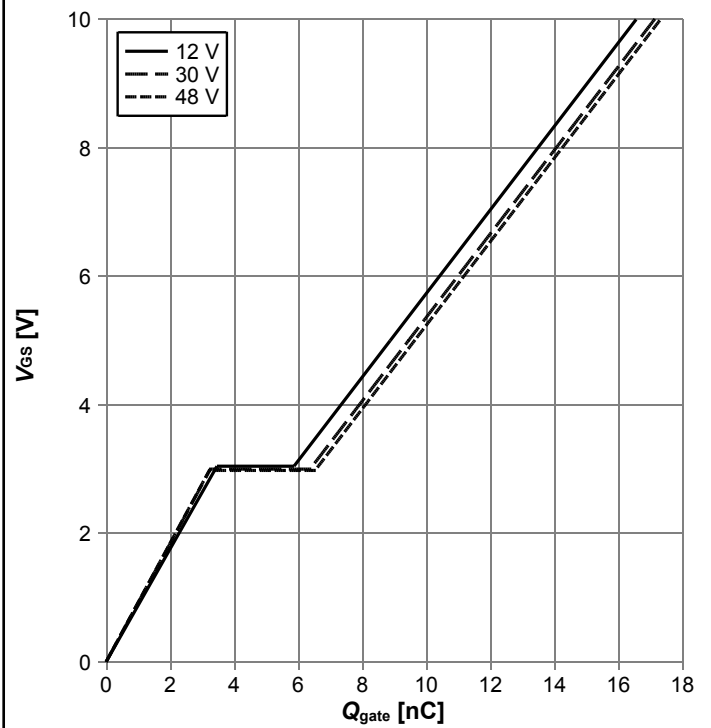


**Diagram 13: Avalanche characteristics**



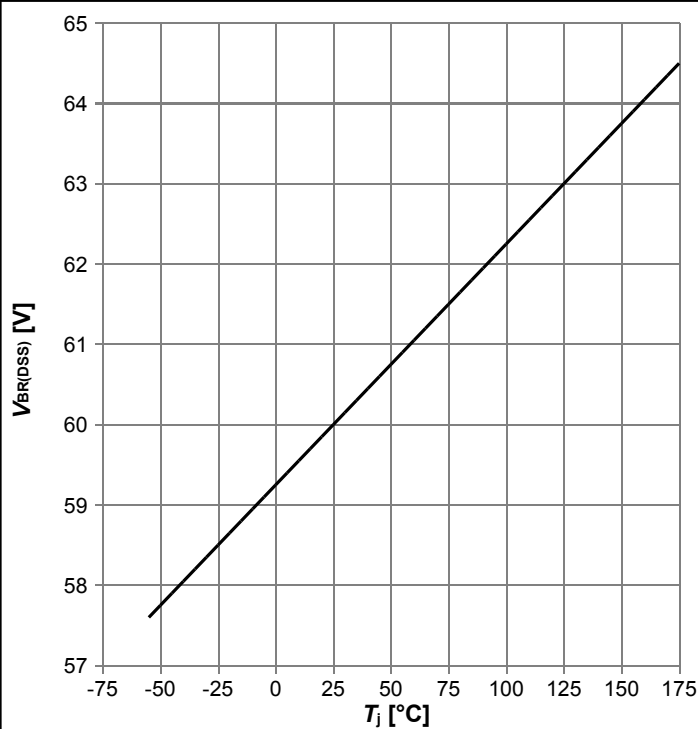
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



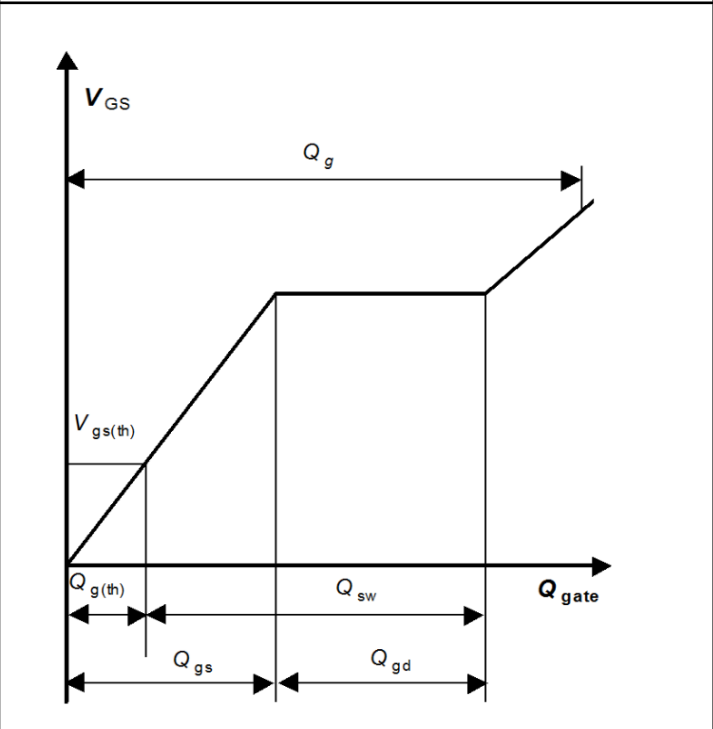
$V_{GS}=f(Q_{gate}), I_D=32$  A pulsed,  $T_j=25$  °C; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

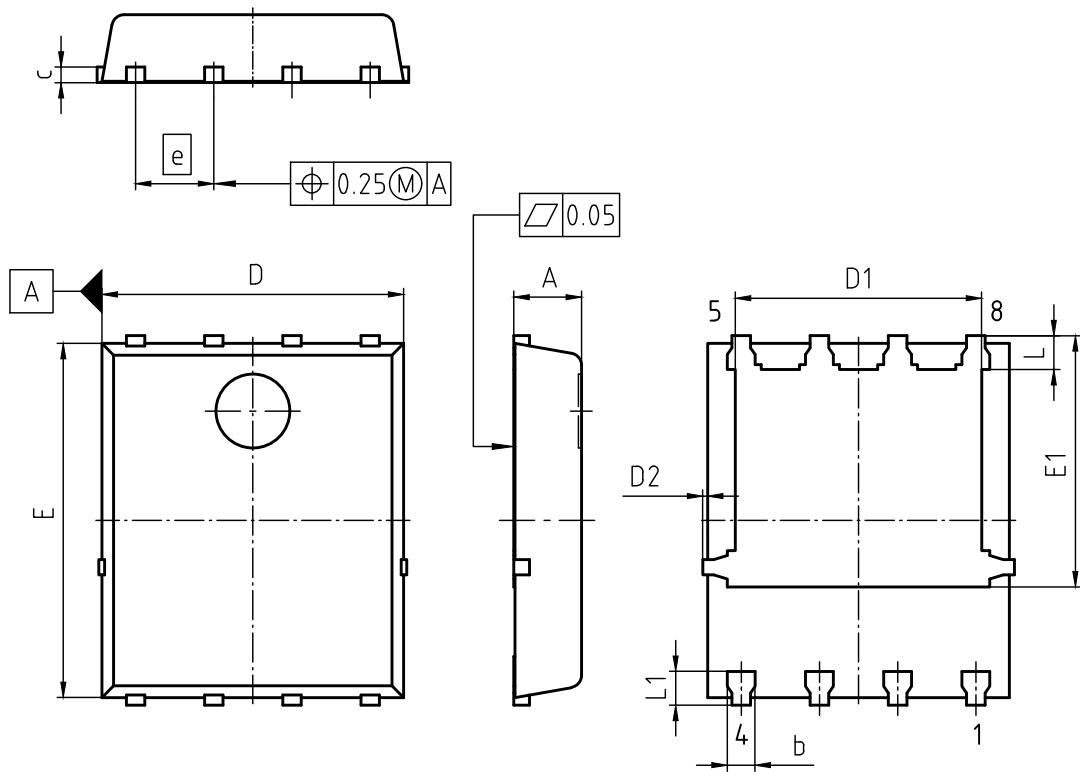


$V_{BR(DSS)}=f(T_j); I_D=1$  mA

**Diagram Gate charge waveforms**



## 5 Package Outlines



PACKAGE - GROUP NUMBER: PG-TDSON-8-U08		
REVISION: 01	DATE: 12.02.2021	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
b	0.34	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	4.05	4.25
e	1.27	
L	0.45	0.65
L1	0.45	0.65

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE INTRUSION 0.1 MM  
PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED,  
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

## Revision History

ISC0703NLS

**Revision: 2021-03-15, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-03-15	Release of final version

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