S1C17W15 (rev 1.00)





16-bit Single Chip Microcontroller • Low power operation from 1.2V with a single alkaline or silver

- oxide button battery. Low power consumption standby driving at HALT 0.5 μ A (TBD) .
- *super economy mode Built-in LCD Driver: 30 SEG x 8 COM (max.)
- Internal 4ch R/F converters enable to realize various sensing.

DESCRIPTIONS

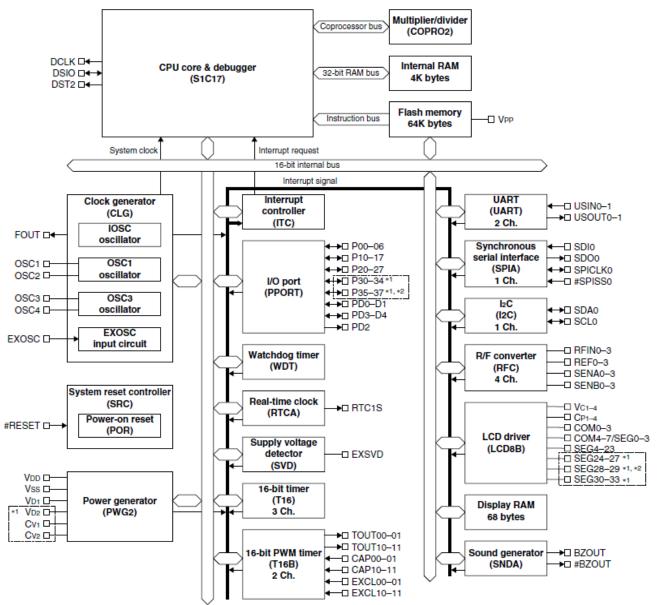
The S1C17W15 is a 16-bit MCU that features low-voltage operation from 1.2 V even though the Flash memory is included. The embedded high-efficiency DC-DC converter generates the constant-voltage to drive the IC with lower power consumption than 4-bit MCUs. This IC includes a real-time clock, a stopwatch, an LCD driver, and a PWM timer capable of being used to generate drive waveforms for a motor driver as well as a high-performance 16-bit CPU. It is suitable for battery-driven applications that require an LCD display and timers.

FEATURES

Model	S1C17W15					
CPU						
CPU Core	Seiko Epson original 16-bit RISC CPU Core S1C17					
Other	On-chip debuager					
Embedded Flash memory	On only debugger					
Capacity	64K bytes (for both instructions and data)					
Erase/program count	50 times (min.) * Programming by the debugging tool ICDmini					
Other	Security function to protect from reading/programming by ICDmini					
oulei	On-board programming function using ICDmini					
Embedded RAM						
Capacity	4K bytes					
Embedded display RAM	H bytes					
Capacity	68 bytes					
Clock generator (CLG)	oo bytes					
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)					
System clock frequency	1.1 MHz (max.) VDD = 1.2 to 1.6 V					
(operating frequency)	4.2 MHz (max.) VDD = 1.2 to 1.6 V 4.2 MHz (max.) VDD = 1.6 to 3.6 V					
IOSC oscillator circuit	700 kHz (typ.) embedded oscillator					
(boot clock source)	23 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)					
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator					
	Oscillation stop detection circuit included					
OSC3 oscillator circuit						
	4.2 MHz (max.) crystal/ceramic oscillator					
	500 kHz, 1, 2, and 4 MHz-switchable embedded oscillator					
EV000 de de instat	500 Hz to 2 MHz CR oscillator (an external R is required)					
EXOSC clock input	4.2 MHz (max.) square or sine wave input					
Other	Configurable system clock division ratio					
	Configurable system clock used at wake up from SLEEP state					
	Operating clock frequency for the CPU and all peripheral circuits is selectable.					
I/O port (PPORT)						
Number of general-purpose I/O ports	Input/output port: 35 bits (max., 100-pin package or chip)					
	32 bits (max., 80-pin package)					
	27 bits (max., 64-pin package)					
	Output port: 1 bit (max.)					
	Pins are shared with the peripheral I/O.					
Number of input interrupt ports	31 bits (max., 100-pin package or chip)					
	28 bits (max., 80-pin package)					
	23 bits (max., 64-pin package)					
Number of ports that support universal port	23 bits					
multiplexer (UPMUX)	A peripheral circuit I/O function selected via software can be assigned to each port.					
Timers						
Watchdog timer (WDT)	Generates NMI or watchdog timer reset.					
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters					
	Theoretical regulation function for 1-second correction					
	Alarm and stopwatch functions					
16-bit timer (T16)	Alarm and stopwatch functions 3 channels					
	Alarm and stopwatch functions 3 channels Generates the SPIA master clock.					
16-bit timer (T16) 16-bit PWM timer (T16B)	Alarm and stopwatch functions 3 channels Generates the SPIA master clock. 2 channels					
	Alarm and stopwatch functions 3 channels Generates the SPIA master clock. 2 channels Event counter/capture function					
	Alarm and stopwatch functions 3 channels Generates the SPIA master clock. 2 channels Event counter/capture function PWM waveform generation function					
16-bit PWM timer (T16B)	Alarm and stopwatch functions 3 channels Generates the SPIA master clock. 2 channels Event counter/capture function					
	Alarm and stopwatch functions 3 channels Generates the SPIA master clock. 2 channels Event counter/capture function PWM waveform generation function					
16-bit PWM timer (T16B)	Alarm and stopwatch functions 3 channels Generates the SPIA master clock. 2 channels Event counter/capture function PWM waveform generation function					
16-bit PWM timer (T16B) Supply voltage detector (SVD)	Alarm and stopwatch functions 3 channels Generates the SPIA master clock. 2 channels Event counter/capture function PWM waveform generation function Number of PWM output or capture input ports: 2 ports/channel					

Serial interfaces 2 channel Baud-rate generator included, IrDA1.0 supported Synchronous Serial Interface (SPIA) 1 channel 2 to 16-bit variable data length The 16-bit timer (T16) can be used for the baud-rate generator in master mode. I ² C (I2C) 1 channel Buzer output function 512 Hz to 16 kHz output frequencies One-shot output function 0ne-shot output function Pitch: 128 Hz to 16 kHz ~ C3 to C6 Duration: 7 notes/rests (Half note/rest to thirty-second note/rest) Tempo: 16 tempos (30 to 480) Tie may be specified.		Generates an interrupt or reset according to the detection level evaluation.						
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PC (2C) 1 channel Sound generator (SNDA) Buzzer output function S12 Hz to 16 Hz output frequencies Melody generation function Crite 4 store (GD Carlos Ca		The 16-bit timer (T16) can be used for the baud-rate generator in master mode.						
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Sound generator (SNDA) T2 Hz to 16 Hz output frequencies Buzzer output function 51 Hz to 16 Hz output frequencies Melody generation function Picht 28 Hz 16 ft 4Hz output frequencies Duration: 7 notes/rests (Half not/rest to thirty-second note/rest) Tome-shot output function LCD driver (LCD24A) Te may be specified. LCD output 29 SEG x 5-8 COM (max); 32 SEG x 1-4 COM (max); (60-pin package) LCD contrast 32 levels Cher 11 do 15 bits power supply included, external voltage can be applied. RF conversion channels 4 channels (Up to two sensors can be connected to each channel.) Supported sensors DC-bits resistive sensors, AC-bits resistive sensors (Ch.0 only) Mutheried/Wider (COPRO2) The met typic included, external voltage the voltage level (can be enabled/disabiled using a register). Supported sensors DC-bits resistive sensors, AC-bits resistive sensors (Ch.0 only) Mutheried/Wider (COPRO2) Reset when the met pin is set to low. Affices PT pin Reset when the reset pin is set to low. Power on reset Reset when the watchdog timer overflows (can be enabled/disabiled using a register). Supply voltage detector reset Reset when the watchdog timer overeflows (can be enabled/disabiled using a register).		Baud-rate generator included						
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LCD output 30 SEG x 5-8 COM (max), 32 SEG x 1-4 COM (max), (80-pin package) LCD contrast 32 Bex x 5-8 COM (max), 32 SEG x 1-4 COM (max), (80-pin package) LCD contrast 32 Bevels Other 114 or 1/3 bias power supply included, external voltage can be applied. RF converter (RFC) Conversion method Conversion method CR oscillation type with 2-bit counters Number of conversion channels. 4 channels (Up to two sensors can be connected to each channel.) Supported sensors DC-bias resistive sensors, AC-bias resistive sensors (Ch.0 only) Multiplierd/divef (COPRO2)		Tie may be specified.						
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LCD contrast 32 levels Other 14 or 1/3 bits power supply included, external voltage can be appled. RF convertion (RFC) CR oscillation type with 24-bit counters Number of conversion channels 4 channels (Up to two sensors can be connected to each channel.) Supported sensors DC-bits resistive sensors, AC-bits resistive sensors (Ch.0 only) Multipler/divider (COPRO2) Anithmetic functions 16-bit x 16-bit multiplier 16-bit x 16-bit multiplier 16-bit x 12-bit multiplier 16-bit x 16-bit multiplier Reset Power on reset Reset when the nop 01 bP01/P02/P03 keys are pressed simultaneously (can be enable/disabled using a register). Supply voltage detector reset Reset when the watch/og timer overflows (can be enable/disabled using a register). Power supply voltage 12 to 3.6 V VDD operating voltage for super economy mode 2.6 to 3.6 V <t< td=""><td></td><td></td></t<>								
Other 14/a or 1/3 bias power supply included, external voltage can be applied. RF converter (RFO) Conversion method CR oscillation type with 24-bit counters Number of conversion channels 4 channels (Up to two sensors can be connected to each channel.) Supported sensors DC-bias resistive sensors, AC-bias resistive sensors (Ch.0 only) Multiplier/divider (COPRO2) 16-bit x 16-bit x 22-bit multiplier Antimetic functions 16-bit x 16-bit x 22-bit multiplier Reset 32-bit x 32-bit divider Reset Reset at power on. Rey entry reset Reset at power on. Rey entry reset Reset when the valchog timer overflows (can be enabled/disabled using a register). Watchdog timer reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Non-maskable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 2 to 3.6 V (100-pin/80-pin package or chip) Ob operati								
RF convertion (RFC) CR oscillation type with 24-bit counters Conversion channels 4 channels (Up to two sensors can be connected to each channel.) Supported sensors DC-bias resistive sensors, AC-bias resistive sensors (Ch. 0 only) Multiplier/divider (COPRO2) 16-bit x 16-bit multiplier Antimetic functions 16-bit x 16-bit x 10-bit x								
Conversion method CR oscillation type with 24-bit counters Number of conversion channels 4 channels (Up to two sensors can be connected to each channel.) Supported sensors DC-bias resistive sensors, AC-bias resistive sensors (Ch.0 only) Multiplier/divider (COPRO2) Anithmetic functions 16-bit x 16-bit x 12-bit multiplier 16-bit x 16-bit x 32-bit x 32-bit multiplier Reset 32-bit x 32-bit divider Reset Reset at power on. Revent Reset at power on. Revent Reset when the reset point is set to low. Power-on reset Reset when the valchdog timer overflows (can be enabled/disabled using a register). Support of the set of the method to the supply voltage detector detects the set voltage level (can be enabled/disabled using a register). Non-maskable Interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable Interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable Interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable Interrupt 2 sto 3.6 V (we = 7.5 V external power supply oils required.) Vob operating voltage for super economy mode (10 to pin/80-pin package or chip) 2 sto 3.6 V (we = 7.5 V external power supply is required.) </td <td></td> <td>1/4 or 1/3 bias power supply included, external voltage can be applied.</td>		1/4 or 1/3 bias power supply included, external voltage can be applied.						
Number of conversion channels 4 channels (Up to two sensors can be connected to each channel.) Supported sensors DC-bias resistive sensors (AC-bias resistive sensors (Ch.0 only) Multiplier/divider (COPRO2) 16.bit × 16-bit multiplier Antimetic functions 16.bit × 16-bit multiplier 32.bit × 32-bit multiplier 16.bit × 16-bit multiplier Power-on reset Reset when the reset pin is set to low. Power-on reset Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register). Supply voltage detector reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Non-maskable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 18 to 3.6 V (v _{se} = 7.5 V external power supply is required.) VDD operating voltage 12 to 3.6 V (v _{se} = 7.5 V external power supply is required.) OVD operating voltage for super accommy mode 2.5 to 3.6 V (v _{se} = 7.5 V external power supply is required.) Operating temperature range 14 to to 85 °C Operating temperature range 40 to 85 °C Oursent consumption 5.1 µA								
Supported sensors DC-bias resistive sensors, AC-bias resistive sensors (Ch.0 only) Multiplerd/div/der (COPRO2) Arithmetic functions 16-bit × 16-bit multipler 16-bit × 16-bit x 16-bit x 16-bit multipler 32-bit x 32-bit x 32-bit div/der #RESET pin Reset #RESET pin Reset when the reset pin is set to low. Power-on reset Reset at power on. Key entry reset Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register). Supply voltage detector reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Non-maskable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 12 to 3.6 V (Vpp = 7.5 V external power supply is required.) VDD operating voltage 12 to 3.6 V (Vpp = 7.5 V external power supply is required.) VDD operating voltage for Flash programming 12 to 3.6 V (Vpp = 7.5 V external power supply is required.) VDD operating voltage for Flash programming 12 to 3.6 V (Vpp = 7.5 V external power supply is required.) VDD operating voltage for Flash programming 12 to 3.6 V (Vpp = 7.5 V external power supply is required.) VDD operating voltage for Flash programming </td <td></td> <td></td>								
Multiplier/divider (COPRO2) 16-bit × 16-bit multiplier Arithmetic functions 16-bit × 16-bit + 32-bit multiplier 16-bit × 16-bit + 32-bit multiplier 16-bit × 16-bit × 16-bit multiplier Reset Reset them the reset pin is set to low. Power-on reset Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register). Key entry reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Supply voltage detector reset Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register). Non-maskable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 1.2 to 3.6 V VDD operating voltage 1.2 to 3.6 V VDD operating voltage for Flash programming 1.2 to 3.6 V (lop-in/80-pin package or chip) Operating voltage for super economy mode 2.5 to 3.6 V (lop-in/80-pin package or chip) Operating temperature 0.15 μA Operating temperature range -40 to 85 °C Current comsumption 0.15 μA SLEEP mode 0.5 μA 0.5C1=0FF, OSC1=0FF, OSC1=0FF UAU mode 8 μA <								
Arithmetic functions 16-bit x 16-bit multiplier Rest 32-bit + 32-bit multiply and accumulation unit 32-bit + 32-bit divider Reset when the reset pin is set to low. Power-on reset Reset when the PO0 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register). Key entry reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Supply voltage detector reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Non-maskable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt External interrupt: 1 system (8 levels) Power supply voltage 12 to 3.6 V VDD operating voltage for super economy mode 2.5 to 3.6 V (100-pin/80-pin package or chip) Operating voltage for super economy mode 2.5 to 3.6 V (100-pin/80-pin package or chip) Operating voltage for super economy mode 1.6 to 3.6 V VDD operating voltage for super economy mode 0.6 S $^{\circ}$ Operating temperature .40 to 85 $^{\circ}$ C Current consumption .18 to 3.6 V (100-pin/80-pin package or chip) SLEEP mode .0 S $^{\circ}$ La 2.4 kHz, RTC=ON 0.3 A OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bia), Super economy mode (100		DC-bias resistive sensors, AC-bias resistive sensors (Ch.0 only)						
Ite-bit × 16-bit × 32-bit aveltiply and accumulation unit 32-bit × 32-bit divider Reset #RESET pin Reset when the reset pin is set to low. Power-on reset Reset at power on. Key entry reset Reset at power on. Watchdog timer reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Supply voltage detector reset Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register). Non-maskable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt External interrupt: 1 system (3 levels) Power supply voltage Thermal interrupt: 1 system (3 levels) Power supply voltage for super economy mode 2.5 to 3.6 V (100-pin/80-pin package or chip) Operating voltage for Fisah programming 1.8 to 3.6 V (100-pin/80-pin package or chip) Operating temperature - Operating temperature - Operating temperature - Osc1=32 kHz, RTC=ON 0.3 µ A OsC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 1.2 µA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super econom								
32-bit 32-bit divider 32-bit 32-bit divider #Reset #Reset when the reset pin is set to low. Power-on reset Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register). Watchdog timer reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Supply voltage detector reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Non-maskable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt External interrupt: 1 system (8 levels) Power supply voltage 12 to 3.6 V VDD operating voltage 1.2 to 3.6 V (100-pin/80-pin package or chip) Operating temperature Operating temperature Operating temperature 4.40 to 85 °C Current consumption 5.1 µA SLEEP mode 0.15 µA OSC1=32 kHz, RTC=ON Cup = 7.5 V external power only mode (100-pin/80-pin package or chip) 1.2 µA OSC1=32 kHz, RTC=ON Cup = 0.5 µA 0.5 µA 0.5 µA 0.5 µA 0.5 µA 0.5 µA 0.5 µA	Arithmetic functions							
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#RESET pin Reset when the reset pin is set to low. Power-on reset Reset when the reset pin is set to low. Reset when the PO0 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register). Reset when the watchdog timer overflows (can be enabled/disabled using a register). Supply voltage detector reset Reset when the watchdog timer overflows (can be enabled/disabled using a register). Non-maskable interrupt Reset when the watchdog timer overflows (can be enabled/disabled using a register). Non-maskable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 4 systems (Reset, address misaligned interrupt, debug, NMI) Programmable interrupt 12 to 3.6 V VDD operating voltage for Super economy mode 1.5 to 3.6 V (type 7.5 V external power supply is required.) VDD operating voltage for Super economy mode 2.5 to 3.6 V (type 7.5 V external power supply is required.) VDD operating voltage for Super economy mode 2.5 to 3.6 V (type 7.5 V external power supply is required.) VDD operating voltage for Super economy mode 2.5 to 3.6 V (type 7.5 V external power supply is required.) VDD operating voltage for Super economy mode 2.5 to 3.6 V (type 7.5 V external power supply is required.) Super advalue 0.5 µA 0.5 µA <		32-bit ÷ 32-bit divider						
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Vob operating voltage for super economy mode 2.5 to 3.6 V (100-pin/80-pin package or chip) Operating temperature -40 to 85 °C Current consumption 0.15 μA SLEEP mode 0.15 μA IOSC=OFF, OSC1=OFF, OSC3=OFF HALT mode 0.5 μA OSC1=32 kHz, RTC=ON 0.3 μA OSC1=32 kHz, RTC=ON, Super economy mode (100-pin/80-pin package or chip) 1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) RUN mode 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 20 OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin								
Operating temperature range -40 to 85 °C Current consumption SLEEP mode 0.15 μA IOSC=OFF, OSC1=OFF, OSC3=OFF 0.5 μA HALT mode 0.5 μA OSC1=32 kHz, RTC=ON 0.3 μA OSC1=32 kHz, RTC=ON, Super economy mode (100-pin/80-pin package or chip) 1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) RUN mode 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 9 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP14-100pin		2.5 to 3.6 V (100-pin/80-pin package or chip)						
Operating temperature range -40 to 85 °C Current consumption								
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HALT mode 0.5 μA OSC1=32 kHz, RTC=ON 0.3 μA OSC1=32 kHz, RTC=ON, Super economy mode (100-pin/80-pin package or chip) 1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) RUN mode 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin	SLEEP mode	0.15 µA						
HALT mode 0.5 μA OSC1=32 kHz, RTC=ON 0.3 μA OSC1=32 kHz, RTC=ON, Super economy mode (100-pin/80-pin package or chip) 1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) RUN mode 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin		IOSC=OFF, OSC1=OFF, OSC3=OFF						
0.3 µA OSC1=32 kHz, RTC=ON, Super economy mode (100-pin/80-pin package or chip) 1.2 µA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) RUN mode 8 µA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 µA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 µA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin	HALT mode	0.5 μΑ						
1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) RUN mode 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin		0.3 µA						
OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) RUN mode 8 µA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 µA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 µA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin								
Super economy mode (100-pin/80-pin package or chip) RUN mode 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin								
RUN mode 8 µA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 µA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 µA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin								
OSC1=32 kHz, RTC=ON, CPU=OSC1 4 µA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 µA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin	PLIN mode							
OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form 1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin	Ron mode	OSC1=32 kHz, RTC=ON, CPU=OSC1						
250 µA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 Shipping form I SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin								
Shipping form SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin								
1 SQFN9-64pin 2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin		OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3						
2 TQFP13-64pin 3 TQFP14-80pin 4 QFP15-100pin	Shipping form							
3 TQFP14-80pin 4 QFP15-100pin	1	SQFN9-64pin						
4 QFP15-100pin	2	TQFP13-64pin						
	3	TQFP14-80pin						
5 Die form (Pad pitch: 80 µm (min.))								
	5	Die form (Pad pitch: 80 µm (min.))						

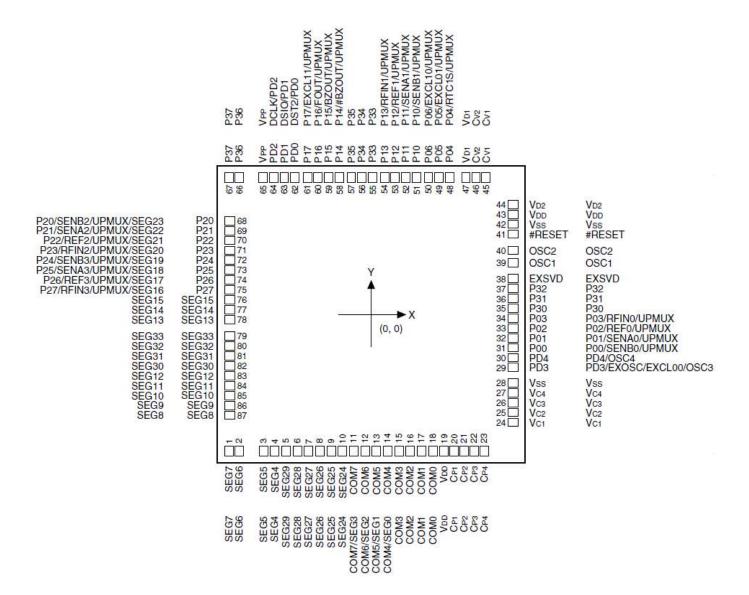
BLOCK DIAGRAM



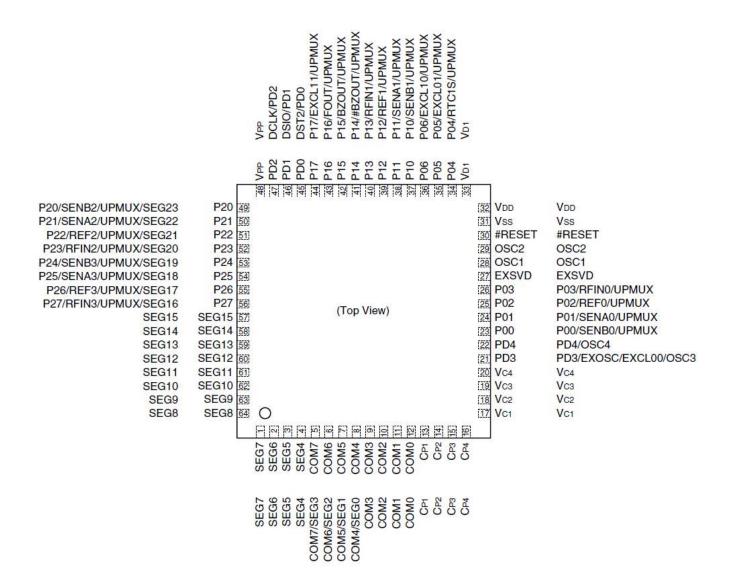
*1 These pins do not exist in the 64-pin package. *2 These pins do not exist in the 80-pin package.

PIN CONFIGURATION DIAGRAM

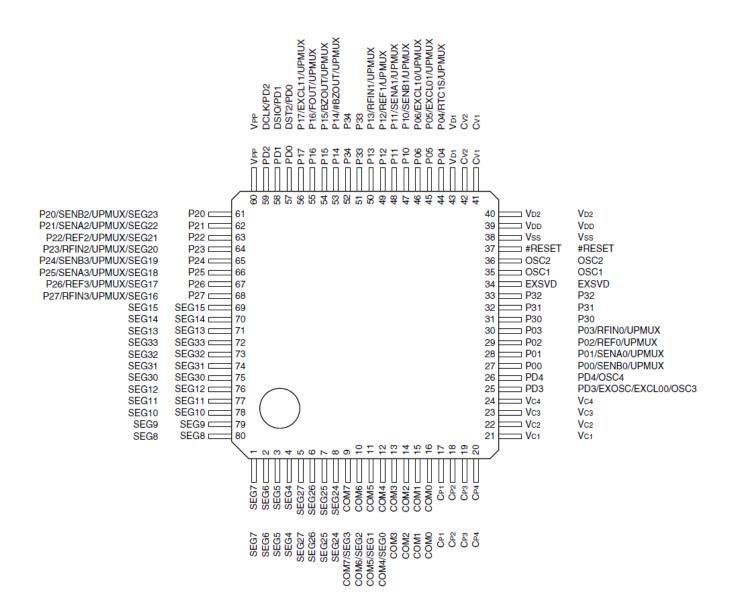
Die form



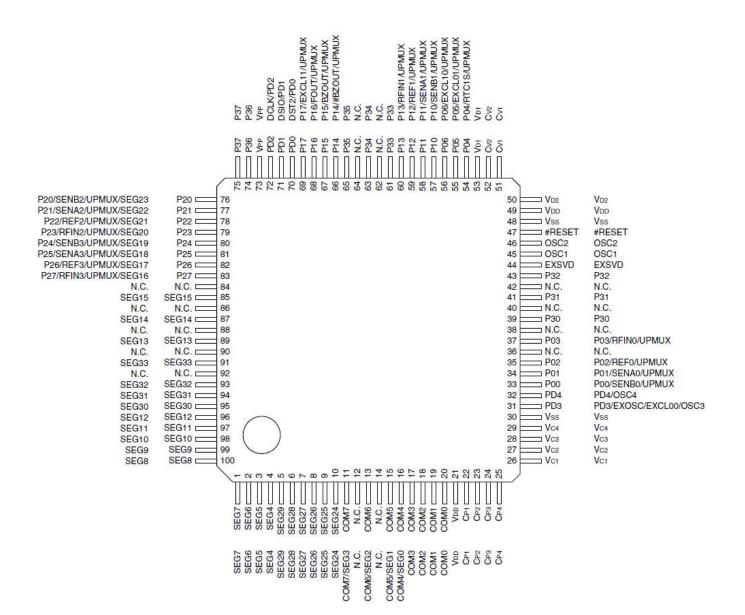
SQFN9-64pin, TQFP13-64pin



TQFP14-80pin



QFP15-100pin



■ PIN DESCRIPTIONS

I O I/O

P A

Assigned signal:

: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:	

= Input = Output = Input/output = Power supply = Analog signal = High impedance state

Initial state:

A= Analog signalHi-Z= High impedance stateI (Pull-up)= Input with pulled upI (Pull-down)= Input with pulled downHi-Z= High impedance stateO (H)= High level outputO (L)= Low level output

O (L) Tolerant fail-safe structure:

= Over voltage tolerant fail-safe type I/O cell included (see the "I/O Ports" chapter)

name VDD V VSS V VPP V VD1 V VD2 V CV1-2 C VC1-4 V CP1-4 C OSC1 C OSC2 C	Assigned signal VDD VSS VPP VD1 VD2 CV1-2 VC1-4 CP1-4 OSC1 OSC2 #RESET P00	I/O P P A A A A A A A A A A A A A A A A A A A	Initial state - - - - - - - - - - - - - -	fail-safe structure - - - - - - - - - - - - -	Function Power supply (+) GND Power supply for Flash programming DC-DC converter output DC-DC converter stabilization capacitor connect pin DC-DC converter charge pump capacitor connect pins LCD panel driver power supply LCD power supply booster capacitor connect pins	64pin	80pin	100pin /Chip / / / / / / / /
VSS V VPP V VD1 V VD2 V CV1-2 C VC1-4 V CP1-4 C OSC1 C OSC2 C	VSS VPP VD1 VD2 CV1-2 VC1-4 CP1-4 OSC1 OSC2 #RESET P00	P P A A A P A A A	- - - - - - -	-	GND Power supply for Flash programming DC-DC converter output DC-DC converter stabilization capacitor connect pin DC-DC converter charge pump capacitor connect pins LCD panel driver power supply	✓ ✓ ✓ −		✓ ✓ ✓
VPP V VD1 V VD2 V CV1-2 C VC1-4 V CP1-4 C OSC1 C OSC2 C	VPP VD1 VD2 CV1-2 VC1-4 CP1-4 OSC1 OSC2 #RESET P00	P A A A P A A A		-	Power supply for Flash programming DC-DC converter output DC-DC converter stabilization capacitor connect pin DC-DC converter charge pump capacitor connect pins LCD panel driver power supply	✓ ✓ - -	\ \ \ \	✓ ✓ ✓
VD1 V VD2 V CV1-2 C VC1-4 V CP1-4 C OSC1 C OSC2 C	VD1 VD2 CV1-2 VC1-4 CP1-4 OSC1 OSC2 #RESET P00	A A A A A A A		-	DC-DC converter output DC-DC converter stabilization capacitor connect pin DC-DC converter charge pump capacitor connect pins LCD panel driver power supply	-		✓ ✓
VD2 V CV1-2 C VC1-4 V CP1-4 C OSC1 C OSC2 C	VD2 CV1-2 VC1-4 CP1-4 OSC1 OSC2 #RESET P00	A P A A A		-	DC-DC converter stabilization capacitor connect pin DC-DC converter charge pump capacitor connect pins LCD panel driver power supply	-	√ √	√ √
CV1-2 C VC1-4 V CP1-4 C OSC1 C OSC2 C	CV1-2 VC1-4 CP1-4 OSC1 OSC2 #RESET P00	A P A A A		-	DC-DC converter charge pump capacitor connect pins LCD panel driver power supply	-	<i>\</i>	
VC1-4 V CP1-4 C OSC1 C OSC2 C	VC1-4 CP1-4 OSC1 OSC2 #RESET P00	P A A A	-		LCD panel driver power supply		-	1
CP1-4 C OSC1 C OSC2 C	CP1-4 OSC1 OSC2 #RESET P00	A A A	-			1		
OSC1 C OSC2 C	OSC1 OSC2 #RESET P00	A A		-	LCD power supply booster capacitor connect pins		1	1
OSC2 C	OSC2 #RESET P00	A	-	-	LOB power supply becater supulities connect pind	1	1	1
	#RESET P00		-		OSC1 oscillator circuit input	1	1	1
	P00	I		-	OSC1 oscillator circuit output	1	1	1
#RESET #			I (Pull-up)	-	Reset input	1	1	1
P00 P		I/O	Hi-Z	-	I/O port	1	1	1
L	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
S	SENB0	I/O/A			R/F converter Ch.0 sensor B oscillator pin	1	1	1
P01 P	P01	I/O	Hi-Z	-	I/O port	1	1	1
U	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
S	SENA0	I/O/A			R/F converter Ch.0 sensor A oscillator pin	1	1	1
P02 P	P02	I/O	Hi-Z	-	I/O port	1	1	1
U	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
R	REF0	I/O/A			R/F converter Ch.0 reference oscillator pin	1	1	1
P03 P	P03	I/O	Hi-Z	-	I/O port	1	1	1
L	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
R	RFIN0	I/O/A			R/F converter Ch.0 oscillation input	1	1	1
P04 P	P04	I/O	Hi-Z	-	I/O port	1	1	1
F	RTC1S	0			Real-time clock 1-second cycle pulse output	1	1	1
U	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
P05 P	P05	I/O	Hi-Z	-	I/O port	1	1	1
U	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
E	EXCL01	Ι			16-bit PWM timer Ch.0 event counter input 1	1	1	1
P06 P	P06	I/O	Hi-Z	-	I/O port	1	1	1
L	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
E	EXCL10	Ι			16-bit PWM timer Ch.1 event counter input 0	1	1	1
P10 P	P10	I/O	Hi-Z	1	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
s	SENB1	I/O			R/F converter Ch.1 sensor B oscillator pin	1	1	1
P11 P	P11	I/O	Hi-Z	1	I/O port	1	1	1
ι	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
S	SENA1	I/O			R/F converter Ch.1 sensor A oscillator pin	1	1	1

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	64pin	Package 80pin	100pin /Chip
P12	P12	I/O	Hi-Z	1	I/O port	1	1	✓.
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
	REF1	I/O			R/F converter Ch.1 reference oscillator pin	1	1	1
P13	P13	I/O	Hi-Z	1	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
	RFIN1	0			R/F converter Ch.1 oscillation input	1	1	1
P14	P14	I/O	Hi-Z	1	I/O port	1	1	1
	#BZOUT	0			Sound generator inverted output	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
P15	P15	I/O	Hi-Z	1	I/O port	1	1	1
	BZOUT	0			Sound generator output	1	1	1
	UPMUX	I/O	_		User-selected I/O (universal port multiplexer)	1	1	1
P16	P16	I/O	Hi-Z	1	I/O port	1	1	1
	UPMUX	I/O	_		User-selected I/O (universal port multiplexer)	1	1	1
	FOUT	0			Clock external output	1	1	1
P17	P17	I/O	Hi-Z	1	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
	EXCL11	Α			16-bit PWM timer Ch.1 event counter input 1	1	1	1
P20	P20	I/O	Hi-Z	1	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
	SENB2	I/O			R/F converter Ch.2 sensor B oscillator pin	1	1	1
	SEG23	А			LCD segment output		1	1
P21	P21	1/0	Hi-Z	1	I/O port			· ·
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		1	· ·
	SENA2	I/O			R/F converter Ch.2 sensor A oscillator pin			· ·
	SEG22	A	_		LCD segment output		1	-
P22	P22	I/O	Hi-Z	1	I/O port			· ·
	UPMUX	I/O			User-selected I/O (universal port multiplexer)			· ·
	REF2	I/O			R/F converter Ch.2 reference oscillator pin	1	1	1
	SEG21	А			LCD segment output			1
P23	P23	I/O	Hi-Z	1	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		· ·	· ·
	RFIN2	I/O			R/F converter Ch.2 oscillation input	1	1	1
	SEG20	А			LCD segment output	1	1	1
P24	P24	I/O	Hi-Z	1	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		· ·	· ·
	SENB3	I/O			R/F converter Ch.3 sensor B oscillator pin	1	1	1
	SEG19	A	_		LCD segment output		· ·	· ·
P25	P25	I/O	Hi-Z	1	I/O port		· ·	· ·
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		· ·	· ·
	SENA3	I/O	_		R/F converter Ch.3 sensor A oscillator pin		· ·	· ·
	SEG18	A	1		LCD segment output		· ·	· ·
P26	P26	1/0	Hi-Z		I/O port	· ·	✓ ✓	✓ ✓
	UPMUX	I/O	-		User-selected I/O (universal port multiplexer)	· ·	· ·	· ·
	REF3	A	-		R/F converter Ch.3 reference oscillator pin	 ✓	✓ ✓	✓ ✓
	SEG17	A	-		LCD segment output	· ·	✓ ✓	✓ ✓
P27	P27	1/0	Hi-Z	1	I/O port	 ✓	✓ ✓	✓ ✓
/	UPMUX	I/O		•	User-selected I/O (universal port multiplexer)	✓ ✓	✓ ✓	✓ ✓
	RFIN3	I/O	-		R/F converter Ch.3 oscillation input		✓ ✓	✓ ✓
	SEG16	A	4		LCD segment output	✓ ✓	✓ ✓	✓ ✓

Din/nod	Assigned		Initial	Tolerant		Package		
Pin/pad name	Assigned signal	I/O	Initial state	fail-safe structure	Function	64pin	80pin	100pin /Chip
P30	P30	I/O	Hi-Z	1	I/O port	~	1	<i>\</i>
P31	P31	I/O	Hi-Z	~	I/O port	1	1	1
P32	P32	I/O	Hi-Z	1	I/O port	1	1	1
P33	P33	I/O	Hi-Z	1	I/O port	~	1	1
P34	P34	I/O	Hi-Z	1	I/O port	~	1	1
P35	P35	I/O	Hi-Z	1	I/O port	1	1	1
P36	P36	I/O	Hi-Z	1	I/O port	1	1	1
P37	P37	I/O	Hi-Z	1	I/O port	1	1	1
PD0	DST2	0	O (L)	1	On-chip debugger status output	1	1	1
	PD0	I/O			I/O port	1	1	1
PD1	DSIO	I/O	I (Pull-up)	1	On-chip debugger data input/output	1	1	1
	PD1	I/O			I/O port	1	1	1
PD2	DCLK	I/O	O(H)	✓	On-chip debugger clock output	1	1	1
	PD2	0			Output port	1	1	1
PD3	PD3	I/O	Hi-Z	-	I/O port	1	1	1
	EXOSC	I			Clock generator external clock input	1	1	1
	EXCL00	Ι			16-bit PWM timer Ch.0 event counter input 0	1	1	1
	OSC3	Α			OSC3 oscillator circuit input	1	1	1
PD4	PD4	I/O	Hi-Z	-	I/O port	1	1	1
	OSC4	Α			OSC3 oscillator circuit output	1	1	1
COM0-3	COM0-3	Α	Hi-Z	-	LCD common output	1	1	1
COM4	COM4	Α	Hi-Z	-	LCD common output	1	1	1
	SEG0	Α			LCD segment output	1	1	1
COM5	COM5	Α	Hi-Z	-	LCD common output	1	1	1
	SEG1	Α			LCD segment output	1	1	1
COM6	COM6	Α	Hi-Z	-	LCD common output	1	1	1
	SEG2	Α			LCD segment output	1	1	1
COM7	COM7	Α	Hi-Z	-	LCD common output	1	1	1
	SEG3	Α			LCD segment output	1	1	1
SEG4-15	SEG4-15	Α	Hi-Z	-	LCD segment output	1	1	1
SEG24-27	SEG24-27	Α	Hi-Z	-	LCD segment output	-	1	1
SEG28-29	SEG28–29	Α	Hi-Z	-	LCD segment output	-	-	1
SEG30-33	SEG30-33	Α	Hi-Z	-	LCD segment output	-	1	1
EXSVD	EXSVD	А	A (I)	_	External power supply voltage detection input	1	1	1

Note: In the peripheral circuit descriptions, the assigned signal name is used as the pin name.

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Peripheral circuit	Signal to be assigned	I/O	Channel number n	Function
Synchronous serial	SDIn	I	<i>n</i> =0	SPIA Ch.n data input
interface (SPIA)	SDOn	0		SPIA Ch.n data output
(SFIA)	SPICLKn	I/O		SPIA Ch.n clock input/output
	#SPISSn	I		SPIA Ch.n slave-select input
I ² C (I2C) UART (UART)	SCLn	I/O	<i>n</i> =0	I2C Ch.n clock input/output
	SDA <i>n</i>	I/O		I2C Ch.n data input/output
	USIN <i>n</i>	I	<i>n</i> =0,1	UART Ch.n data input
	USOUTn	0		UART Ch.n data output
16-bit PWM timer	TOUTn0/CAPn0	I/O	<i>n</i> -0,1	T16B Ch.n PWM output/capture input 0
(T16B)	TOUTn1/CAPn1	I/O		T16B Ch.n PWM output/capture input 1

Note: Do not assign a function to two or more pins simultaneously.

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