Features

- ESD Protect for 4 Lines with Bi-directional
- Provide ESD protection for the protected line to
  IEC 61000-4-2 (ESD) ±20kV (air), ±12kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 7A (8/20μs)
  Cable Discharge Event (CDE)
- Small SOT23-5L package saves board space
- Protect four I/O lines or four power lines
- Fast turn-on and Low clamping voltage
- Low operating voltage: < 5V
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part available

Applications

- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

Description

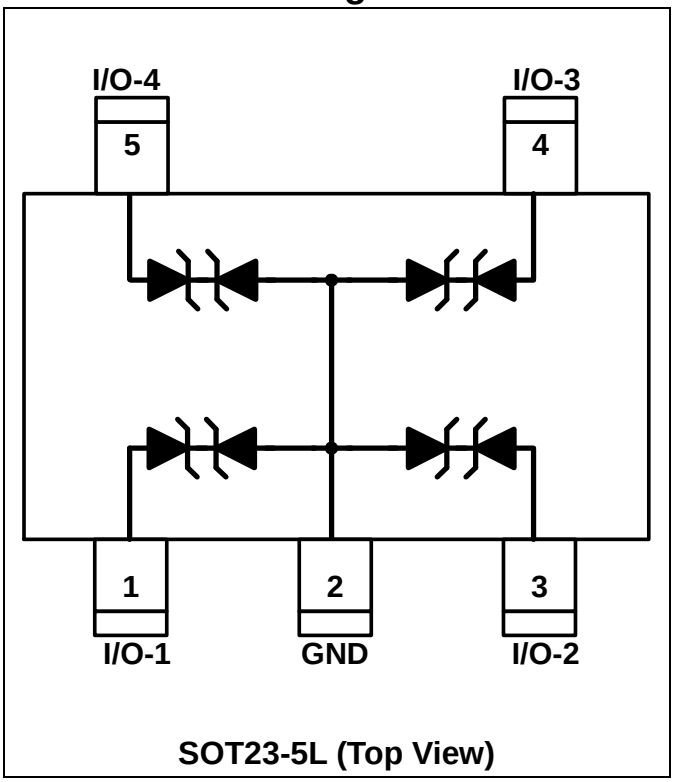
AZ2025-04S is a design which includes four bi-directional surge rated clamping cells to protect four power lines, or four control lines, or four low speed data lines in an electronic systems. The AZ2025-04S has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ2025-04S is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control/data lines, protecting any downstream components.

AZ2025-04S is bi-directional and may be used on lines where the signal swings above and below ground.

AZ2025-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



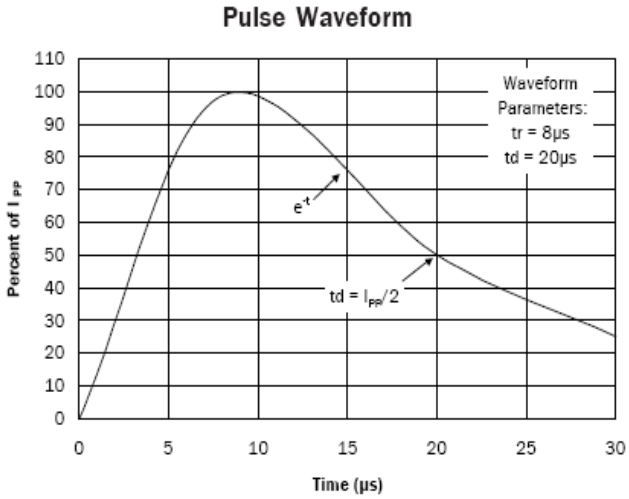
SOT23-5L (Top View)

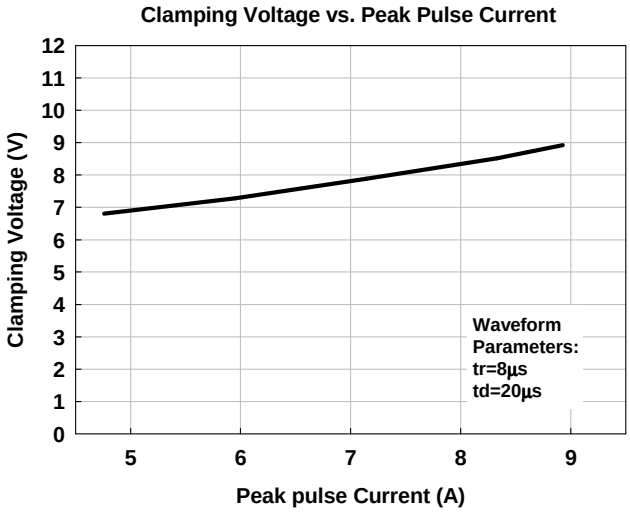
SPECIFICATIONS

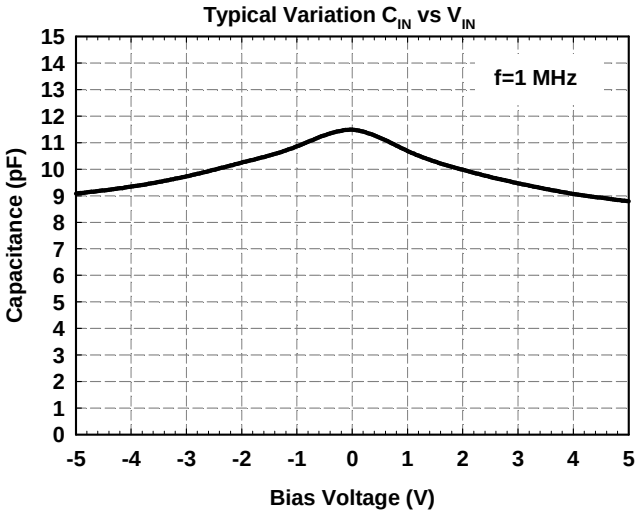
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20us)	I_{PP}	8.5	A
Operating Supply Voltage (Pin-1, -3, -4, -5 to Pin-2)	V_{DC}	6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1}	±22 ±15	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

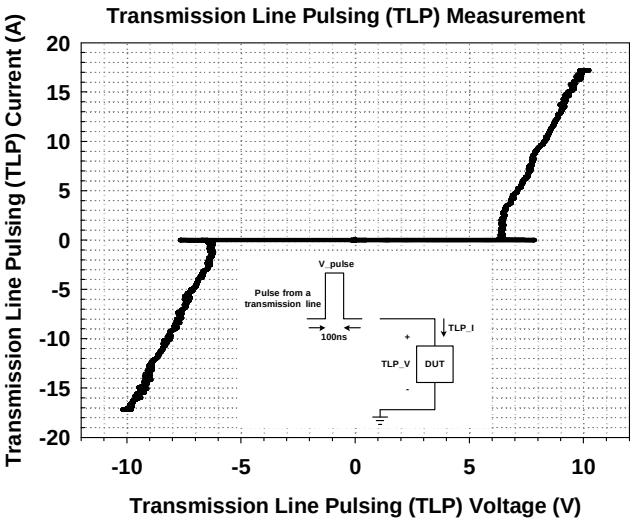
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1, -3, -4, -5 to Pin-2, T=25 °C			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C. Pin-1, -3, -4, -5 to Pin-2.			2.5	µA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C. Pin-1, -3, -4, -5 to Pin-2.	6.1		9	V
Clamping Voltage	V_{CL}	I_{PP}=5A, tp=8/20us, T=25 °C. Pin-1, -3, -4, -5 to Pin-2.		7	8	V
Clamping Voltage	V_{CL}	I_{PP}=7A, tp=8/20us, T=25 °C. Pin-1, -3, -4, -5 to Pin-2.		8	9	V
ESD Holding Voltage	V_{hold}	IEC 61000-4-2 6kV, T=25 °C, Contact mode, Pin-1, -3, -4, -5 to Pin-2.		10.5		V
Channel Input Capacitance	C_{IN}	V_R= 0V, f = 1MHz, T=25 °C. Pin-1, -3, -4, -5 to Pin-2.		12	15	pF

Typical Characteristics









Applications Information

The AZ2025-04S is designed to protect four lines against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The usage of the AZ2025-04S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin-1, -3, -4,and -5. The pin 2 is connected to a ground plane on the board. Since AZ2025-04S is bi-directional, these connections can be reversed (protected line to pin 2, ground to pin 1 or 3 or 4 or 5). In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ2025-04S should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ2025-04S.
- Place the AZ2025-04S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

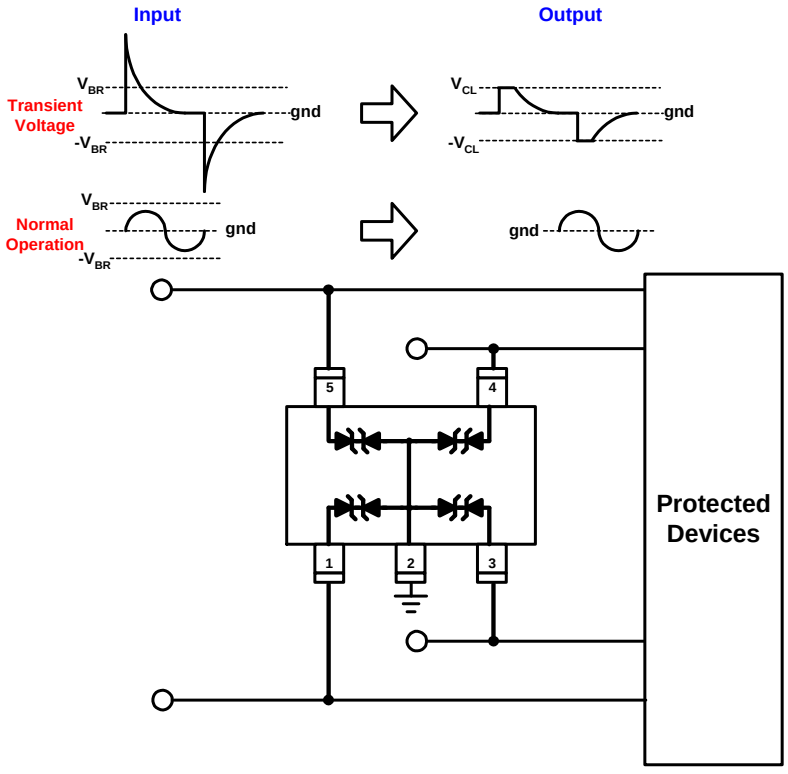


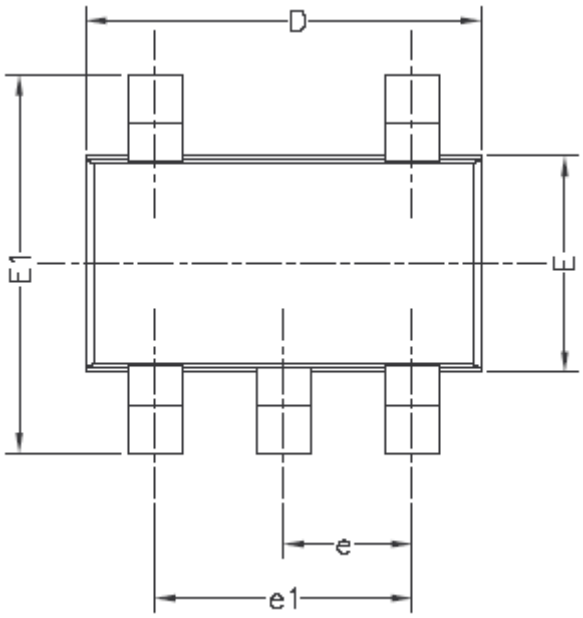
Fig. 1

Mechanical Details

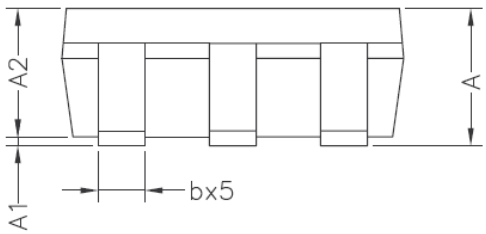
SOT23-5L

PACKAGE DIAGRAMS

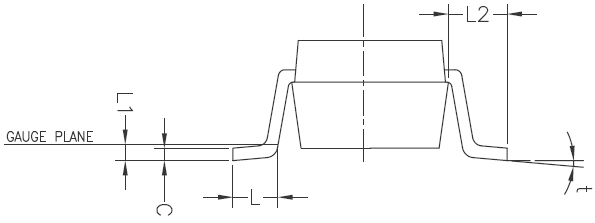
TOP VIEW



SIDE VIEW



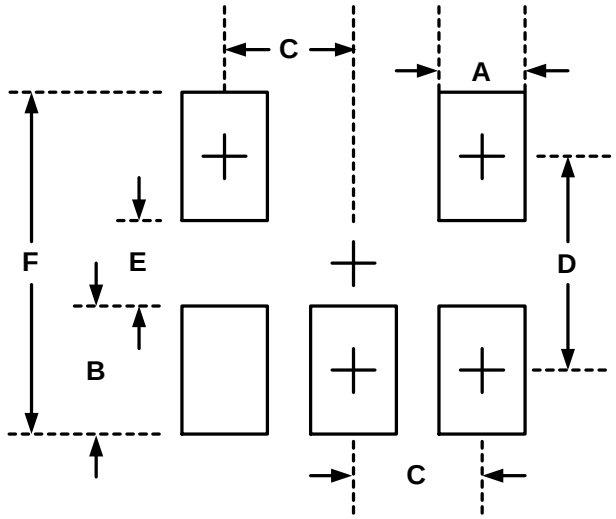
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.95	1.45	0.037	0.057
A1	0	0.15	0.000	0.006
A2	0.9	1.3	0.035	0.051
b	0.3	0.5	0.012	0.020
C	0.08	0.21	0.003	0.008
D	2.72	3.12	0.107	0.123
E	1.4	1.8	0.055	0.071
E1	2.6	3	0.102	0.118
e	0.95BSC		0.037BSC	
e1	1.8	2	0.071	0.079
L	0.3	0.6	0.012	0.024
L1	0.2BSC		0.008BSC	
L2	0.6REF		0.024REF	
Θ	0	8	0	8

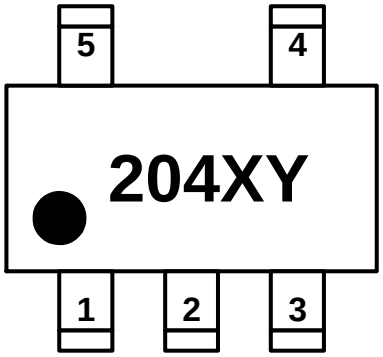
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



204 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ2025-04S	204XY
AZ2025-04S (Green part)	**222XY**

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZ2025-04S.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2007/08/08	Original Release.
Revision 2008/09/29	Add the marking code for Green part.
Revision 2008/12/26	Update the PACKAGE DIMENSIONS.
Revision 2008/12/29	Correct the typo at V_{DC}.
Revision 2011/06/18	1. Update the Company Logo. 2. Add the Ordering Information.