Freescale Semiconductor
Data Sheet: Technical Data

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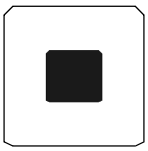
RoHS

MMM7210



LGA–170

MMM7210

WCDMA/GSM/EDGE Transceiver

Ordering Information

Device	Device Marking	Package
MMM7210B	MMM7210	170 pin LGA

1 Introduction

The MMM7210 transceiver is a highly integrated transceiver that supports 3GPP WCDMA/GSM/EGPRS wireless standards. The digital input/output of the MMM7210 interfaces directly to a baseband processor using either Freescale legacy interface (FLI) or standard 3G DigRF interfaces.

The MMM7210 receiver has five independent RF inputs which encompass all wireless band combinations. Each path supports three primary modes of operation: a reduced current and gain state to support WCDMA with an external LNA and interstage SAW, an EGPRS mode in which the LNA is connected directly to a SAW, and a high linearity mode to support WCDMA operation when directly matched to a duplexor. The three different modes provide approximately the same input impedances such that, even though the input match is optimized for one mode, all three modes are usable. Multi-mode RF inputs are converted to a common baseband path which is shared between WCDMA and EGPRS. This common baseband path is optimized for die area and current consumption through the use of a

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high dynamic range SD ADC. The receiver uses a homodyne configuration for WCDMA and a VLIF configuration for EGPRS.

The transmitter (Tx) includes six independent RF outputs, four of these paths are dedicated to WCDMA and two to EGPRS. Three of the WCDMA outputs are dedicated to high band and one for low band. The two EGPRS outputs support the standard quad band configuration. The hybrid power control system provides closed loop operation for all modes and power levels of EGPRS and provides closed loop power control for WCDMA at high powers. To achieve the current drain goals driven by FOMA, the power control system explicitly supports use of switched power supply for the WCDMA amplifiers.

2 Features

Listed below are key features of the MMM7210.

- Five Rx inputs each supporting both WCDMA and GSM/EDGE
  - GSM850 plus WCDMA bands V and VI
  - EGSM and WCDMA band VIII
  - DCS plus WCDMA bands III and IX
  - PCS and WCDMA band II
  - WCDMA bands I, IV, and X
- Six Tx outputs
  - Freescale's polar GSM/EDGE modulation
    - Low-band cellular/EGSM
    - High-band DCS/PCS
  - Direct launch WCDMA
    - WCDMA bands V, VI, VIII, FOMA 800
    - WCDMA bands III, IV, IX (FOMA 1700), X
    - Band II (PCS band)
    - Band I (UMTS band)
- DigRF 3G interface or Freescale legacy interface
- Auxiliary SPI to control LNAs, PAs, switching regulator, and antenna switch
- Simplified timing and control through a MCU core
- IQ auto calibration
- Polar modulation auto calibration
- Smart AOC Tx power control minimizes factory calibration
- 9.25 mm × 7.65 mm package

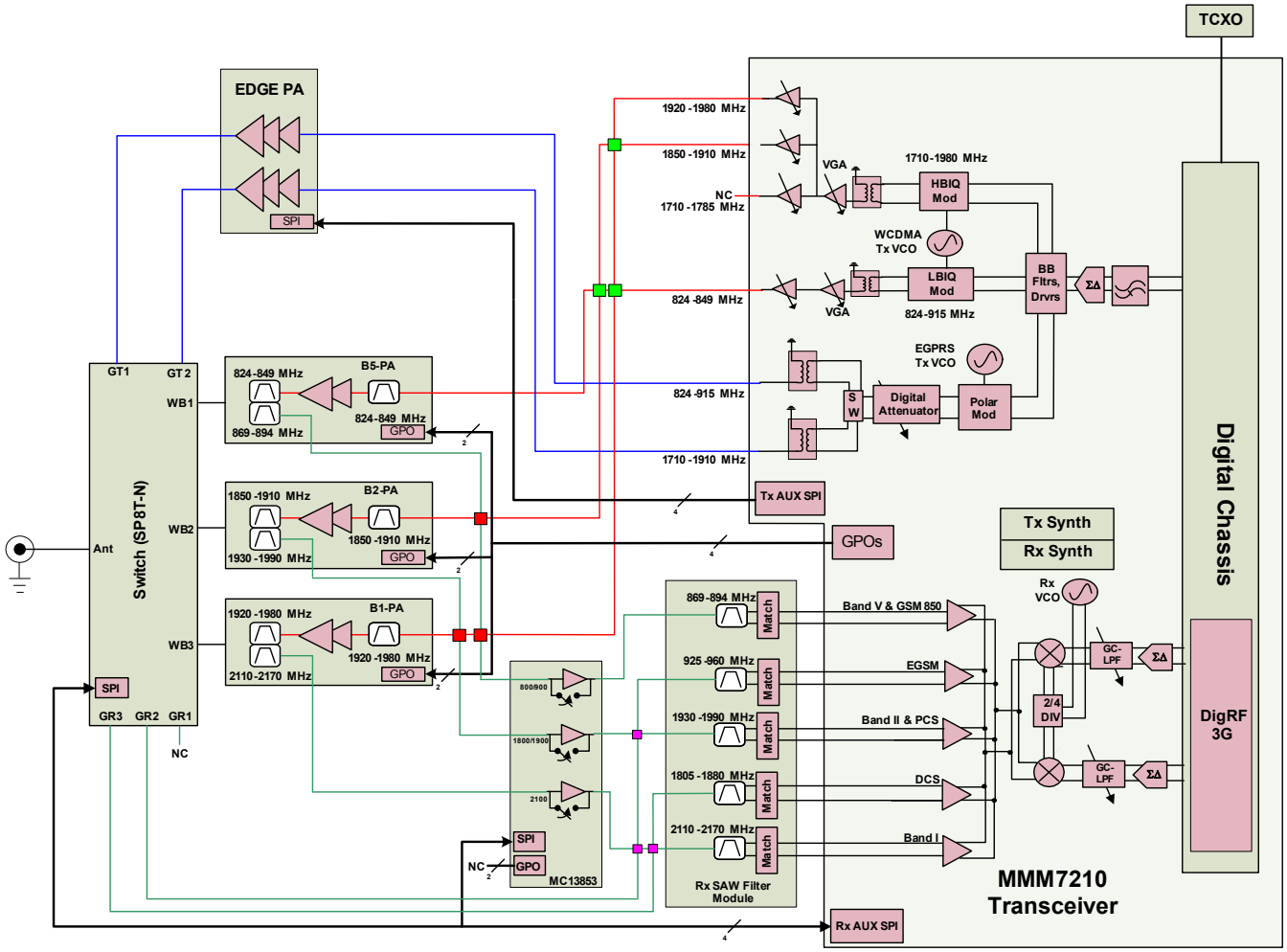


Figure 1. System Block Diagram

3 MMM7210 Signal Description

Table 1. MMM7210 Signal Descriptions

Pin Number	Pin	Alternate	Count	Type	Input/Output Voltage Range	Note
RF						
41, 42	RxCell	—	2	RF IN	—	GSM850 plus bands V and VI.
43, 44	RxEgsm	—	2	RF IN	—	EGSM and band VIII.
47, 48	RxDcs	—	2	RF IN	—	DCS, band III, and band IX.
45, 46	RxPcs	—	2	RF IN	—	PCS and band II.
49, 50	RxUmts	—	2	RF IN	—	Bands I, IV, and X.
35	TxGsmLb	—	1	RF OUT	—	DCS and PCS.

Table 1. MMM7210 Signal Descriptions (continued)

Pin Number	Pin	Alternate	Count	Type	Input/Output Voltage Range	Note
36	TxGsmHb	—	1	RF OUT	—	GSM850 and EGSM.
30	TxWcdmaLb	—	1	RF OUT	—	Bands V, VI, and VIII.
29	TxWcdmaDcs	—	1	RF OUT	—	Bands III, IV, and X.
28	TxWcdmaPcs	—	1	RF OUT	—	Band II.
27	TxWcmdaUmts	—	1	RF OUT	—	Band I.
Test						
38, 40, 61, 62	AnaTest[3:0]	—	4	ANA INOUT	0.1–1.975 V	Traditional test mux. Purely analog.
125	HssData	—	1	DIG OUT	0.1–1.975 V	—
123	HssClk	—	1	DIG OUT	0.1–1.975 V	Reference clock for high speed serial interface analogous to DigRF SysClk.
124	HssFrm	—	1	DIG OUT	0.1–1.975 V	Frame signal for HSS mux.
160	ScanMode	—	1	DIG IN	0.1–1.975 V	Dedicated pin to enable test mode to be used as needed (for scan mode).
107	BDM	—	1	DIG INOUT	0.1–1.975 V	BDM is a debug port for the MCU.
154	TxMon	—	1	DIG INOUT	0.1–1.975 V	TxMon is the Tx pin of a UART used as a monitor.
18	RxMon	—	1	DIG INOUT	0.1–1.975 V	RxMon is the Rx pin of the UART used to allow direct access to the MCU. Driving impedance must be tri-state when used with serial flash.
137	DbGpio0	—	1	DIG INOUT	0.1–1.975 V	Digital GPO's for debug and test.
148	DbGpio1	—	1	DIG INOUT	0.1–1.975 V	Digital GPO's for debug and test.
Analog						
97	CobraSf	—	1	ANA INOUT	0.1–1.975 V	Bypass cap for WCDMA Tx VCO.
51, 69	SF[1:0]	—	2	ANA INOUT	0.1–1.975 V	Bypass cap for RF VCO super filters. One for 2G Rx and Tx and one for 3G Rx.
87	CLK_SF	—	1	ANA INOUT	0.1–1.975 V	ClkSynth VCO SF pin
2	REF_BYP	—	1	ANA INOUT	0.1–1.975 V	Bypass cap for reference plus visibility for trim.
4	TCXO_IN	—	1	ANA IN	0–2.4 V	TCXO input. Takes 0.8 V sin wave.
3	TCXO_PWR	—	1	ANA OUT	2.475 Maximum	Supply for TCXO. Allows MMM7210 to enable / disable the TCXO. The TCXO regulator is 2.4 V.
96	Vramp	—	1	ANA OUT	0.1–2.2 V	Controls GSM PA Vramp and provides bias signal to WCDMA PAs.

Table 1. MMM7210 Signal Descriptions (continued)

Pin Number	Pin	Alternate	Count	Type	Input/Output Voltage Range	Note
156	PacIn	—	1	ANA IN	0.1–2.3 V	Detector input for power control subsystem.
167	AocAdcCdCap	—	1	ANA INOUT	0.1–1.975 V	Reference for PAC ADC.
144	TxDacRef	—	1	ANA OUT	0.1–1.975 V	Vgc input voltage to WCDMA transmit (internal control signal).
98	WcdmaTxZero	—	1	ANA INOUT	0.1–1.975 V	Zero for WCDMA Tx PLL. Loop filter monitor point for 3G Tx PLL.
Baseband Interface						
8, 9	RxData3G	—	2	ANA OUT	0.1–1.975 V	DigRF 3G line driver.
6, 7	TxData3G	—	2	ANA IN	0.1–1.975 V	DigRF 3G line receiver.
140	SysClk	—	1	DIG OUT	0.1–1.975 V	Provides TXCO divided by two in legacy mode and at startup in DigRF 3G mode. Transitions to 1248 MHz/48 in DigRF 3G high speed mode.
128	SysClkEn	STANDBY	1	DIG IN	0.1–1.975 V	DigRF 3G function. Initiates the transition out of deep sleep starting with turning on the TXCO and super filters. STANDBY is legacy mode to enable TCXO.
99	AuxRef[0]	—	1	ANA OUT	0.1–1.975 V	Buffered copy of TCXO divided by two as a nominally 1V sin wave.
89, 76	AuxRef[2:1]	—	2	ANA OUT	0.1–1.975 V	Buffered copies of the TCXO divided by two as square waves at the nominally 1.8 V digital interface voltage. Programmable slew rate.
113	AuxRefEn	—	1	DIG IN	0.1–1.975 V	Enables any of the AuxClk outputs. Starts up the TCXO when SysClkEn is low.
116	RESETB	—	1	DIG IN	0.1–1.975 V	Reset pin.
126	RefEnB	—	1	DIG IN	0.1–1.975 V	Enables TCXO on SysClk without waking up MMM7210. Primarily for use in PDA mode.
136	INTERRUPT	—	1	DIG OUT	0.1–1.975 V	General purpose interrupt not intended for normal operation.
103	LOW_BATT_B	—	1	DIG IN	0.1–1.975 V	Asserted by PM IC when battery voltage drops below threshold. Terminates 2GTx to keep phone from shutting down.
Freescale Legacy Interface						
127	MelodyTxDataI	TMS	1	DIG IN	0.1–1.975 V	Tx SSI as two bit serial stream
115	MelodyTxDataQ	TDI	1	DIG IN	0.1–1.975 V	
151	MelodyRxDataI	TDO	1	DIG OUT	0.1–1.975 V	Rx SSI as two bit serial streams.

Table 1. MMM7210 Signal Descriptions (continued)

Pin Number	Pin	Alternate	Count	Type	Input/Output Voltage Range	Note
150	MelodyRxDataQ	—	—	—	0.1–1.975 V	—
138	MelodyFrmIn	TCK	1	DIG IN	0.1–1.975 V	Legacy 3G framing in. Overloaded with JTAG clk.
162	MelodyFrmOut	TMS	1	DIG OUT	0.1–1.975 V	Legacy 3G framing in. Overloaded with JTAG state machine ctl.
15	Melody4XClk	—	1	DIG OUT	0.1–1.975 V	Legacy AFC'd clock. Will be either a jittered 15.36 MHz clock derived from the 1248 MHz or a 15.6 MHz derived by 1248 / 80 as determined by the capability of the clock PLL in BB.
19	WspiDataIn	NRTST	1	DIG IN	0.1–1.975 V	Connected to WB QSPI on BB. Overloaded with JTAG reset.
155	WspiData4Wire	—	1	DIG OUT	0.1–1.975 V	SPI read back for normal mode SPI. Connected to WB QSPI on BB.
153	WspiClk	—	1	DIG IN	0.1–1.975 V	WCDMA SPI clock.
143	WspiFrm	—	1	DIG IN	0.1–1.975 V	WCDMA SPI frame.
20	MspiData	—	1	DIG INOUT	0.1–1.975 V	GSM SPI data input. Note: Mspi and Wspi are multiplexed inside of MMM7210 transceiver.
164	MspiDout	—	1	DIG OUT	0.1–1.975 V	GSM SPI readback.
165	MspiClk	—	1	DIG IN	0.1–1.975 V	GSM SPI clock.
166	MspiFrm	—	1	DIG IN	0.1–1.975 V	GSM SPI frame.
11	RxStrb	—	1	DIG IN	0.1–1.975 V	L1 strobe for receiver.
10	TxStrb	—	1	DIG IN	0.1–1.975 V	L1 strobe equivalent to Tx TAS.
101	TpcBit	—	1	DIG IN	0.1–1.975 V	Defines AOC direction as read on RmpStrb.
139	RmpStrb	—	1	DIG IN	0.1–1.975 V	L1 strobe equivalent to TPC TAS.
114	BlnkStrb	—	1	DIG IN	0.1–1.975 V	Reserved for future use.
13	IfcMode1	—	1	DIG IN	0.1–1.975 V	Sets interface mode to BB interface. Sensed only as part of sequence out of reset.
147	IfcMode2	—	1	DIG IN	0.1–1.975 V	Sets interface mode to proprietary interface. Sensed only as part of sequence out of reset.
104	RxTxData	—	1	DIG INOUT	0.1–1.975 V	DigRF 2G data pin.
17	RxTxDataBbp	—	1	DIG OUT	0.1–1.975 V	DigRF 2G data out pin for normal mode SPI.
152	RxTxFrm	—	1	DIG INOUT	0.1–1.975 V	DigRF 2G framing pin.
16	Strb	—	1	DIG IN	0.1–1.975 V	DigRF 2G strobe.

Table 1. MMM7210 Signal Descriptions (continued)

Pin Number	Pin	Alternate	Count	Type	Input/Output Voltage Range	Note
FE Control						
105,106 129,142	FeGpo[3:0]	—	4	DIG OUT	0.1–1.975 V	GPOs, primarily but not necessarily to control PAs.
100	RxAuxSpiClk	GPO4	1	DIG OUT	0.1–1.975 V	Clock for auxiliary Rx SPI. Optional GPO
102	RxAuxSpiData	GPO5	1	DIG INOUT	0.1–1.975 V	Data for RxAuxSpi. Optional GPO.
112	RxAuxSpiFrm	GPO6	1	DIG OUT	0.1–1.975 V	Frame for auxiliary Rx SPI. Optional GPO.
91	AuxSpiVdd1p8	—	1	ANA OUT	0.1–1.975 V	Provides power to digital interface of FE ICs. Also serves as a conditioned enable signal. (1.8 V).
119	TxAuxSpiClk	—	1	DIG OUT	0.1–1.975 V	Clock for auxiliary Tx SPI.
130	TxAuxSpiData	—	1	DIG INOUT	0.1–1.975 V	Data for auxiliary Tx SPI.
131	TxAuxSpiFrm	—	1	DIG OUT	0.1–1.975 V	Frame for auxiliary Tx SPI.
118	SwitcherClk	—	1	DIG OUT	0.1–1.975 V	Divided down reference to serve as switcher clock. 26 MHz down to 6.5 MHz using a fractional divider.
117	BypNext	Cth	1	DIG INOUT	0.1–1.975 V	Bi-direction GPIO. Optional gain switch control (logic low = PA high gain state).
Supplies						
52, 58, 79	VddIn	—	3	VDD	2.675–2.875 V	Supplies most analog regs on MMM7210. Connect to VRF1 (2.775 V). Turned off in deep sleep mode to minimize leakage.
75	VddTcxo	—	1	VDD	2.675–2.875 V	Independent supply to TCXO and bandgap reference. Connected to PMIC VRFREF (2.775 V). Only turned off when handset is off.
161	VddIfc	—	1	VDD	1.775–1.975 V	Supply for CMOS pins on digital interface. Connect to PMIC SW2 (1.8 V). Bypass network must be designed to attenuate digital supply noise.
25, 94	VccTx2	—	2	VDD	2.675–2.875 V	First pin connects to Tx modulator and VGA (and external driver chokes). Connect to VRF2 (2.775 V). Must be strongly decoupled from VddIn to contain WCDMA envelope. The second pin connects to the PA bias driver.
134	VccTx1	—	1	VDD	2.675–2.875 V	Tx PLL and regs. Connect to VRF1 (2.775 V).
32	VccTxCp	—	1	VDD	2.675–2.875 V	WCDMA Tx CP. Connect to VRF1 (2.775 V). Needs to be bypassed with high level of attenuation at 26 MHz.

Table 1. MMM7210 Signal Descriptions (continued)

Pin Number	Pin	Alternate	Count	Type	Input/Output Voltage Range	Note
23	TxRegByp	—	1	VDD	—	Pin for external bypass on 2.1V Tx regulator.
90	VddDigIn	—	1	VDD	1.775–1.975 V	Input to the digital regulator. May be tied to a 1.8 V switcher (regulate down to 1.2 V internally).
88, 21	VddDigOut	—	2	VDD	1.1–1.65 V (0.95V for DSM)	Direct input to digital core to allow use of external switcher (1.2 V typ.). External bypass cap (1 uF) required if internal regulator is used.
39	Vdd2p4_byp	—	1	VDD	—	Pin for external bypass of master 2.4 V regulator.
83	Vdd1p2_byp	—	1	VDD	—	Pin for external bypass of master 1.2 V regulator.
63	Vdd1p4_byp	—	1	VDD	—	Pin for external bypass of master 1.4 V regulator.
92	Fuse_EPM_AVDD	—	1	VDD	—	Fuse supply voltage for burning the fuse state.
135	ESDDIG	—	1	GND	—	ESD Ground for DigCore.
	AGnd		51	GND	—	Grounds for analog/RF circuits.
	DGnd		7	GND	—	Grounds for digital core and CMOS line drivers/receivers.
	Total		170			

4 Electrostatic Discharge Characteristics

MMM7210 complies to the ESD characteristics listed below:

- Human Body Model (HBM) to 2000V except for the pins listed in Table 2 which meet 300V
- Machine Model (MM) to 150V except for the pins listed in Table 2 which meet 30V
- Charge Device Model (CDM) to 200V except for the pins listed in Table 2 which meet 50V

Table 2. ESD Exceptions

LGA Pad	Description
41	RXCELL_N
42	RXCELL_P
43	RXEGSM_N
44	RXEGSM_P
45	RXPCS_N

Table 2. ESD Exceptions (continued)

LGA Pad	Description
46	RXPCS_P
47	RXDCS_N
48	RXDCS_P
49	RXUMTS_N
50	RXUMTS_P
27	TXWCDMAUMTS
28	TXWCDMAPCS
29	TXWCDMADCS
30	TXWCDMALB
35	TXGSMLB
36	TXGSMHB
94	VCCTX2A

5 Electrical Characteristics

Table 3. General Specifications
(Specifications for T_a = 25° C unless otherwise noted)

Parameter	Minimum	Typical	Maximum	Unit
Operating Analog Supply Voltage (Less VCOs)	2.675	2.775	2.875	V
Operating Digital Supply Voltage	1.775	1.875	1.975	V
Operating Digital Core Supply Voltage	1.1	1.2	1.65	V
Operating Temperature	-30	27	85	°C
Absolute Maximum Voltage (50A DGO)	—	—	3.1	V
Current Drain - Deep Sleep Mode (DSM) Analog Supplies (2.775 V) Digital Supplies (1.875 V) Digital Core Supply (1.2 V)	—	 5 1 22	 24.4 6.5 100	µA
Current Drain - PDA DSM Analog Supplies (2.775 V) Digital Supplies (1.875 V) Digital Core Supply (1.2 V)	—	 1.8 1.8 2.8	 2.5 2.2 3.4	mA
Current Drain - Standby Analog Supplies (2.775 V) Digital Supplies (1.875 V) Digital Core Supply (1.2 V)	—	 9 3.5 5.7	 12 4 7.3	mA

Table 3. General Specifications (continued)
(Specifications for T_a = 25° C unless otherwise noted)

Parameter	Minimum	Typical	Maximum	Unit
WCDMA Current Drain - Rx Simplex Analog Supplies (2.775 V) Digital Supplies (1.875 V) Digital Core Supply (1.2 V)	—	 63.0 1.6 16.4	 79 6.5 21	mA
WCDMA Current Drain - Tx Simplex (WCDMA Signal at -5 dBm) Analog Supplies (2.775 V) Digital Supplies (1.875 V) Digital Core Supply (1.2 V)	—	 64.0 3.6 9.6	 77.3 4 11.6	mA
GSM Current Drain - Rx Analog Supplies (2.775 V) Digital Supply (1.875 V) Digital Core (1.275 V)	—	 78 1.1 12	 93 4 13.5	mA
GSM Current Drain - Rx Dual Mode Analog Supplies (2.775 V) Digital Supply (1.875 V) Digital Core (1.275 V)	—	 71 1.1 12	 87 4 13.5	mA
GSM Current Drain - Tx Analog Supplies (2.775 V) Digital Supply (1.875 V) Digital Core (1.275 V) EDGE Analog Supplies (2.775 V) Digital Supply (1.875 V) Digital Core (1.275 V)	—	 65 3 10.5 76 3 10.8	 106 4 12.9 91.5 4 11.2	mA

5.1 WCDMA Receiver Performance

5.1.1 3G Rx Top Level Performance Summary

A summary of top level WCDMA receiver performance is shown in Table 4.

Table 4. Top Level 3G Rx Performance Summary

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Rx					
RF Input 1 (Band I, IV and X)	—	2110	—	2170	MHz
RF Input 2 (Band II)	—	1930	—	1990	MHz
RF Input 3 (Band III and IX)	—	1805	—	1880	MHz
RF Input 4 (Band V and VI)	—	869	—	885	MHz
RF Input 5 (Band VIII)	—	925	—	960	MHz

Table 4. Top Level 3G Rx Performance Summary (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Differential Input impedance[1] 2100 Band 1900 Band 1800 Band 900 Band 800 Band	—	—	 17-j69 9-j61 9-j60 14-j74 13-j80	—	 ohms ohms ohms ohms ohms
Band I					
Blocking	Desired: (Rx + 200kHz) = -91.5 dBm F1= ±10 MHz WCDMA Blocker ≥ - 43.8 dBm Record SNR in 3.84 MHz BW	-4.7	6.4	—	dB
Blocking	Desired: (Rx + 200kHz) = -91.5 dBm F1= ±15 MHz WCDMA Blocker ≥ - 31.8dBm Record SNR in 3.84 MHz BW	-4.7	3.3	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -80.5 dBm F1= ±5 MHz WCDMA Blocker ≥ - 39.8dBm Record SNR in 3.84 MHz BW	-4.7	12.9	—	dB
Cascaded IP3	Desired: (Rx + 200kHz) = -91.5 dBm F1= Rx ± 10Mhz (CW), -33.8 dBm F2= Rx ± 20 MHz (WCDMA); -33.8 dBm Record SNR in 3.84 MHz BW	1.3	2.4	—	dB
Cascaded IP2	Desired: (Rx + 200kHz) = -91.5 dBm F1= Rx ± 15Mhz (CW) ≥ - 31.8dBm F2= Rx ± (15 MHz +300kHz) (CW); - 31.8dBm Record SNR in 3.84 MHz BW	-1.7	6.2	—	dB
Sensitivity	RF input is 1MHz offset tone. SNR = -7.7dBm	–	-107.5	-105.7	dBm
Band II					
Blocking	Desired: (Rx + 200kHz) = -92 dBm F1= ±10 MHz WCDMA Blocker ≥ - 46.3 dBm Record SNR in 3.84 MHz BW	-4.7	6.7	—	dB
Blocking	Desired: (Rx + 200kHz) = -92 dBm F1= ±15 MHz WCDMA Blocker ≥ - 34.3dBm Record SNR in 3.84 MHz BW	-4.7	4.5	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -85 dBm F1= ±5 MHz WCDMA Blocker ≥ - 42.3dBm Record SNR in 3.84 MHz BW	-4.7	10.3	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -85 dBm F1= ±2.7 MHz GMSK Blocker ≥ - 47.3dBm Record SNR in 3.84 MHz BW	-4.7	5.4	—	dB

Table 4. Top Level 3G Rx Performance Summary (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Cascaded IP3	Desired: (Rx + 200kHz) = -92.0 dBm F1= Rx ± 10Mhz (CW), -36.2 dBm F2= Rx ± 20 MHz (WCDMA); -36.2 dBm Record SNR in 3.84 MHz BW	1.3	4.0	—	dB
Cascaded IP2	Desired: (Rx + 200kHz) = -92 dBm F1= Rx ± 15Mhz (CW) => - 34.3 dBm F2= Rx ± (15 MHz +300kHz) (CW); - 34.3 dBm Record SNR in 3.84 MHz BW	-1.7	6.6	—	dB
Sensitivity	RF input is 1MHz offset tone. SNR = -7.7dB	–	-109.0	-106	dBm
Band III					
Blocking	Desired: (Rx + 200kHz) = -91 dBm F1= ±10 MHz WCDMA Blocker≥ - 45.3 dBm Record SNR in 3.84 MHz BW	-4.7	8.1	—	dB
Blocking	Desired: (Rx + 200kHz) = -90 dBm F1= ±15 MHz WCDMA Blocker ≥ - 33.3 dBm Record SNR in 3.84 MHz BW	-4.7	5.1	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -84 dBm F1= ±5 MHz WCDMA Blocker ≥ - 41.3 dBm Record SNR in 3.84 MHz BW	-4.7	10.8	—	dB
NarroQPSK, case25 (GTC 5) and Blocking	Desired: (Rx + 200kHz) = -84 dBm F1= ±2.8 MHz GMSK Blocker ≥ - 45.3 dBm Record SNR in 3.84 MHz BW	-4.7	5.5	—	dB
Cascaded IP3	Desired: (Rx + 200kHz) = -92.0 dBm F1= Rx ± 10Mhz (CW), -35.2 dBm F2= Rx ± 20 MHz (WCDMA); -35.2 dBm Record SNR in 3.84 MHz BW	1.3	3.0	—	dB
Cascaded IP2	Desired: (Rx + 200kHz) = -92 dBm F1= Rx ± 15Mhz (CW) => - 34.3 dBm F2= Rx ± (15 MHz +300kHz) (CW); - 34.3 dBm Record SNR in 3.84 MHz BW	-1.7	7.2	—	dB
Sensitivity	RF input is 1MHz offset tone. SNR = -7.7dB.	—	-109.1	-106	dBm
Band IV					
Blocking	Desired: (Rx + 200kHz) = -92 dBm F1= ±10 MHz WCDMA Blocker ≥ - 44.3 dBm Record SNR in 3.84 MHz BW	-4.7	6.0	—	dB
Blocking	Desired: (Rx + 200kHz) = -92 dBm F1= ±15 MHz WCDMA Blocker ≥ - 32.3 dBm Record SNR in 3.84 MHz BW	-4.7	3.2	—	dB

Table 4. Top Level 3G Rx Performance Summary (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Adjacent Channel	Desired: (Rx + 200kHz) = -81 dBm F1= ±5 MHz WCDMA Blocker ≥ - 40.3 dBm Record SNR in 3.84 MHz BW	-4.7	12.8	—	dB
NarroQPSK, case25 (GTC 5) and Blocking	Desired: (Rx + 200kHz) = -85 dBm F1= ±2.7 MHz GMSK Blocker ≥ - 45.3 dBm Record SNR in 3.84 MHz BW	-4.7	2.6	—	dB
Cascaded IP3	Desired: (Rx + 200kHz) = -91.5 dBm F1= Rx ± 10Mhz (CW), -33.8 dBm F2= Rx ± 20 MHz (WCDMA); -33.8 dBm Record SNR in 3.84 MHz BW	1.3	2.4	—	dB
Sensitivity	RF input is 1MHz offset tone. SNR = -7.7dB	–	-107.5	-105.7	dBm
Band V					
Blocking	Desired: (Rx + 200kHz) = -92.4 dBm F1= ±10 MHz WCDMA Blocker ≥ - 46.7dBm Record SNR in 3.84 MHz BW	-4.7	8.4	—	dB
Blocking	Desired: (Rx + 200kHz) = -92.4 dBm F1= ±15 MHz WCDMA Blocker ≥ - 34.7 dBm Record SNR in 3.84 MHz BW	-4.7	5.2	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -81.4 dBm F1= ±5 MHz WCDMA Blocker ≥ - 42.7 dBm Record SNR in 3.84 MHz BW	-4.7	15.0	—	dB
NarroQPSK, case25 (GTC 5) and Blocking	Desired: (Rx + 200kHz) = -83 dBm F1= ±2.7 MHz GMSK Blocker ≥ - 47.7 dBm Record SNR in 3.84 MHz BW	-4.7	8.5	—	dB
Cascaded IP3	Desired: (Rx + 200kHz) = -94.4 dBm F1= Rx± 10Mhz (CW), -36.7 dBm F2= Rx ± 20 MHz (WCDMA); -36.7 dBm Record SNR in 3.84 MHz BW	1.3	4.3	—	dB
Cascaded IP2	Desired: (Rx + 200kHz) = -92.4 dBm F1= Rx ± 15Mhz (CW) => - 31.7 dBm F2= Rx ± (15 MHz +300kHz) (CW); - 31.7 dBm Record SNR in 3.84 MHz BW	-1.7	8.5	—	dB
Sensitivity	RF input is 1MHz offset tone. SNR = -7.7dB	—	-109.1	-106	dBm
Band VI					
Blocking	Desired: (Rx + 200kHz) = -93.4 dBm F1= ±10 MHz WCDMA Blocker ≥ - 45.7 dBm Record SNR in 3.84 MHz BW	-4.7	7.4	—	dB

Table 4. Top Level 3G Rx Performance Summary (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Blocking	Desired: (Rx + 200kHz) = -93.4 dBm F1= ±15 MHz WCDMA Blocker ≥ - 33.7 dBm Record SNR in 3.84 MHz BW	-4.7	3.6	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -82.4 dBm F1= ±5 MHz WCDMA Blocker ≥ - 41.7 dBm Record SNR in 3.84 MHz BW	-4.7	13.5	—	dB
Cascaded IP3	Desired: (Rx + 200kHz) = -94.4 dBm F1= Rx± 10Mhz (CW), -36.7 dBm F2= Rx ± 20 MHz (WCDMA); -36.7 dBm Record SNR in 3.84 MHz BW	1.3	4.3	—	dB
Cascaded IP2	Desired: (Rx + 200kHz) = -92.4 dBm F1= Rx ± 15Mhz (CW) => - 31.7dBm F2= Rx ± (15 MHz +300kHz) (CW); - 31.7 dBm Record SNR in 3.84 MHz BW	-1.7	8.5	—	dB
Sensitivity	RF input is 1MHz offset tone. SNR = -7.7dB	—	-109.1	-106	dBm
Band VIII					
Blocking	Desired: (Rx + 200kHz) = -91.6 dBm F1= ±10 MHz WCDMA Blocker ≥ - 46.6 dBm Record SNR in 3.84 MHz BW	-4.7	7.5	—	dB
Blocking	Desired: (Rx + 200kHz) = -92.6 dBm F1= ±15 MHz WCDMA Blocker ≥ - 35.9 dBm Record SNR in 3.84 MHz BW	-4.7	5.2	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -80.6 dBm F1= ±5 MHz WCDMA Blocker ≥ - 42.9 dBm Record SNR in 3.84 MHz BW	-4.7	14.9	—	dB
NarroQPSK, case25 (GTC 5)and Blocking	Desired: (Rx + 200kHz) = -84.6 dBm F1= ±2.8 MHz GMSK Blocker ≥ - 43.9 dBm Record SNR in 3.84 MHz BW	-4.7	7.4	—	dB
Cascaded IP3	Desired: (Rx + 200kHz) = --92.6 dBm F1= Rx ± 10Mhz (CW), -37.9 dBm F2= Rx ± 20 MHz (WCDMA); -37.9 dBm Record SNR in 3.84 MHz BW	1.3	5.4	—	dB
Cascaded IP2	Desired: (Rx + 200kHz) = -92.6 dBm F1= Rx ± 15Mhz (CW) => - 35.9 dBm	-1.7	6.6	—	dB
Sensitivity	RF input is 1MHz offset tone. SNR = -7.7dB	—	-109.4	-106	dBm

Table 4. Top Level 3G Rx Performance Summary (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Band IX					
Blocking	Desired: (Rx + 200kHz) = -93.0 dBm F1= ±10 MHz WCDMA Blocker ≥ - 45.3 dBm Record SNR in 3.84 MHz BW	-4.7	6.2	—	dB
Blocking	Desired: (Rx + 200kHz) = -93.0 dBm F1= ±15 MHz WCDMA Blocker ≥ - 33.3 dBm Record SNR in 3.84 MHz BW	-4.7	3.1	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -93.0 dBm F1= ±5 MHz WCDMA Blocker ≥ - 41.3 dBm Record SNR in 3.84 MHz BW	-4.7	13.7	—	dB
Cascaded IP3	Desired: (Rx + 200kHz) = -92.0 dBm F1= Rx ± 10Mhz (CW), -35.2 dBm F2= Rx ± 20 MHz (WCDMA); -35.2 dBm Record SNR in 3.84 MHz BW	1.3	3.0	—	dB
Cascaded IP2	Desired: (Rx + 200kHz) = -92 dBm F1= Rx ± 15Mhz (CW)≥ - 34.3 dBm F2= Rx ± (15 MHz +300kHz) (CW); - 34.3 dBm Record SNR in 3.84 MHz BW	-1.7	7.2	—	dB
Sensitivity	RF input is 1MHz offset tone.	—	-109.1	-106	dBm
Band X					
Blocking	Desired: (Rx + 200kHz) = -91.5 dBm F1= ±10 MHz WCDMA Blocker ≥ - 43.8 dBm Record SNR in 3.84 MHz BW	-4.7	6.4	—	dB
Blocking	Desired: (Rx + 200kHz) = -91.5 dBm F1= ±15 MHz WCDMA Blocker≥ - 31.8 dBm Record SNR in 3.84 MHz BW	-4.7	3.4	—	dB
Adjacent Channel	Desired: (Rx + 200kHz) = -80.5 dBm F1= ±5 MHz WCDMA Blocker ≥ - 39.8 dBm Record SNR in 3.84 MHz BW	-4.7	13.0	—	dB
Cascaded IP3	Desired: (Rx + 200kHz) = -91.5 dBm F1= Rx ± 10Mhz (CW), -33.8 dBm F2= Rx ± 20 MHz (WCDMA); -33.8 dBm Record SNR in 3.84 MHz BW	1.3	2.4	—	dB
Sensitivity	RF input is 1MHz offset tone. SNR = -7.7dB	—	-107.5	-105.7	dBm

[1] These impedances are optimized for sensitivity. Deviation from these may reduce performance margins.

5.2 GSM/EGPRS Receiver Performance

5.2.1 2G Rx Performance

Table 5. 2G Rx - All Bands

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
Amplitude Imbalance	After autocal	-0.05	—	0.05	dB
Phase Imbalance	After autocal	-0.5	—	0.5	Degree

Table 6. GSM Rx - Direct Lineup

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
GSM850					
Sensitivity	RF input amplitude = -100 dBm. RF input is +13 kHz above RF channel frequency. Rx programmed to VLIF with LO at +123 kHz. SNR is measured over -250 kHz to 250 kHz bandwidth.	16	18	—	dB
± 600 kHz Blocking	Interferer @600 kHz = CW. Set On channel to -102 dBm CW, set interferer @ Pin = -46 dBm. Record resulting SNR.	9.50	15.00	—	dB
± 1.6 MHz Blocking	Interferer @1.6 MHz = CW. Set On channel to -102 dBm CW, set interferer @ Pin = -36 dBm. Record resulting SNR.	9.50	14.60	—	dB
GSM900					
Sensitivity	RF input amplitude = -100 dBm. RF input is +13 kHz above RF channel frequency. Rx programmed to VLIF with LO at +123 kHz. SNR is measured over -250 kHz to 250 kHz bandwidth.	16	18	—	dB
± 600 kHz Blocking	Interferer @ 600 kHz = CW. Set On channel to -102 dBm CW, set interferer @ Pin = -46 dBm. Record resulting SNR.	9.50	15.10	—	dB
± 1.6 MHz Blocking	Interferer @ 1.6 MHz = CW. Set On channel to -102 dBm CW, set interferer @ Pin = -36 dBm. Record resulting SNR.	9.70	15.10	—	dB
± 3.0 MHz Blocking	Interferer @ 3.0 MHz = CW. Set On channel to -101 dBm CW, set interferer @ Pin = -25 dBm. Record resulting SNR.	9.50	12.80	—	dB
± 400 kHz Edge Blocking	Interferer @ 400 kHz = 8 PSK. Set On channel to -84 dBm CW, set interferer @ Pin = -43 dBm. Record resulting SNR.	11.60	12.80	—	dB
GSM1800					
Sensitivity	RF input amplitude = -100 dBm. RF input is +13 kHz above RF channel frequency. Rx programmed to VLIF with LO at +123 kHz. SNR is measured over -250 kHz to 250 kHz bandwidth.	15.40	17.40	—	dB

Table 6. GSM Rx - Direct Lineup (continued)

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
± 600 kHz Blocking	Interferer @ 600 kHz = CW. Set On channel to -102 dBm CW, set interferer @ Pin = -46 dBm. Record resulting SNR.	9.50	13.30	—	dB
± 1.6 MHz Blocking	Interferer @ 1.6 MHz = CW. Set On channel to -102 dBm CW, set interferer @ Pin = -36 dBm. Record resulting SNR.	9.50	13.70	—	dB
± 3.0 MHz Blocking	Interferer @ 3.0 MHz = CW. Set On channel to -101 dBm CW, set interferer @ Pin = -28 dBm. Record resulting SNR.	9.50	12.50	—	dB
GSM1900					
Sensitivity	RF input amplitude = -100 dBm. RF input is +13 kHz above RF channel frequency. Rx programmed to VLIF with LO at +123 kHz. SNR is measured over -250 kHz to 250 kHz bandwidth.	15.40	17.40	—	dB
± 600 kHz Blocking	Interferer @ 600 kHz = CW. Set On channel to -102 dBm CW, set interferer @ Pin = -46 dBm. Record resulting SNR.	9.50	12.90	—	dB
± 1.6 MHz Blocking	Interferer @ 1.6 MHz = CW. Set On channel to -102 dBm CW, set interferer @ Pin = -36 dBm. Record resulting SNR.	9.50	13.30	—	dB
± 3.0 MHz Blocking	Interferer @ 3.0 MHz = CW. Set On channel to -101 dBm CW, set interferer @ Pin = -28 dBm. Record resulting SNR.	9.50	12.30	—	dB

Table 7. GSM Rx - 3G Lineup

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
GSM850					
Sensitivity	RF input amplitude = -100 dBm. RF input is +13 kHz above RF channel frequency. Rx programmed to VLIF with LO at +123 kHz. SNR is measured over -250 kHz to 250 kHz bandwidth.	11.80	16.80	—	dB
± 600 kHz Blocking	Interferer @ 600 kHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -32 dBm. Record resulting SNR.	9.50	22.90	—	dB
± 1.6 MHz Blocking	Interferer @ 1.6 MHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -22 dBm. Record resulting SNR.	9.50	21.80	—	dB
± 3.0 MHz Blocking	Interferer @ 3.0 MHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -12 dBm. Record resulting SNR.	9.50	16.20	—	dB
GSM900					
Sensitivity	RF input amplitude = -100 dBm. RF input is +13 kHz above RF channel frequency. Rx programmed to VLIF with LO at +123 kHz. SNR is measured over -250 kHz to 250 kHz bandwidth.	11.80	16.80	—	dB
± 600 kHz Blocking	Interferer @ 600 kHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -32 dBm. Record resulting SNR.	9.50	19.70	—	dB
± 1.6 MHz Blocking	Interferer @ 1.6 MHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -22 dBm. Record resulting SNR.	9.50	21.30	—	dB
± 3.0 MHz Blocking	Interferer @ 3.0 MHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -12 dBm. Record resulting SNR.	9.50	16.20	—	dB
GSM1800					
Sensitivity	RF input amplitude = -100 dBm. RF input is +13 kHz above RF channel frequency. Rx programmed to VLIF with LO at +123 kHz. SNR is measured over -250 kHz to 250 kHz bandwidth.	11.80	14.80	—	dB
± 600 kHz Blocking	Interferer @ 600 kHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -32 dBm. Record resulting SNR.	9.50	18.10	—	dB
± 1.6 MHz Blocking	Interferer @ 1.6 MHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -22 dBm. Record resulting SNR.	9.50	19.10	—	dB
± 3.0 MHz Blocking	Interferer @ 3.0 MHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -12 dBm. Record resulting SNR.	9.50	15.90	—	dB
GSM1900					
Sensitivity	RF input amplitude = -100 dBm. RF input is +13 kHz above RF channel frequency. Rx programmed to VLIF with LO at +123 kHz. SNR is measured over -250 kHz to 250 kHz bandwidth.	11.80	13.90	—	dB
± 600 kHz Blocking	Interferer @ 600 kHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -32 dBm. Record resulting SNR.	9.50	17.80	—	dB

Table 7. GSM Rx - 3G Lineup (continued)

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
± 1.6 MHz Blocking	Interferer @ 1.6 MHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -22 dBm. Record resulting SNR.	9.50	18.70	—	dB
± 3.0 MHz Blocking	Interferer @ 3.0 MHz = CW. Set On channel to -88 dBm CW, set interferer @ Pin = -12 dBm. Record resulting SNR.	9.50	—	—	dB

5.3 WCDMA Transmitter Performance

5.3.1 3G General Tx Specifications

Table 8. Tx Cascaded Performance[1]

Parameter	Condition	Min	Typical	Maximum	Unit
RF Output Frequency Range	800 MHz band selected 900 MHz band selected UMTS Extended band US PCS band selected UMTS band selected	824 880 1710 1850 1920	—	849 915 1785 1910 1980	MHz
Minimum Output Power	WCDMA Modulation (Vgc = 0.1 V)	—	-85	-70	dBm
Maximum Output power	W-CDMA Modulation (Vgc = 1.7 V)	9.5	13	—	dBm
Output Impedance[1]	Max. / Min. Output Power	—	50	—	Ω
ACLR @ 5 MHz Offset	W-CDMA Modulation, Pout = -25 to 8 dBm W-CDMA Modulation, Pout = -35 to –25 dBm	—	-46 -42	-42 -36	dBc
ACLR @ 10 MHz Offset	W-CDMA Modulation, Pout = -15 to 8 dBm W-CDMA Modulation, Pout = -25 to –15 dBm	—	-65 -55	-55 -48	dBc
EVM[2]	W-CDMA Modulation, Pout = -55 to 8 dBm W-CDMA Modulation, Pout = -65 dBm W-CDMA Modulation, Pout = -70 dBm	—	4	8 15 30	% rms
Tx Offset Noise - 2100 MHz[3] ±12.5 MHz Offset Noise + 42 MHz Offset Noise + 190 MHz Offset Noise	 W-CDMA Modulation, Pout = 8 dBm W-CDMA Modulation, Pout = 0 dBm W-CDMA Modulation, Pout = 8 dBm W-CDMA Modulation, Pout = 0 dBm W-CDMA Modulation, Pout = 8 dBm W-CDMA Modulation, Pout = 0 dBm	 —	 -122 -128 -129 -136 -136 -140	 -119 -126 -126 -134 -129 -133	 dBm/Hz dBm/Hz dBm/Hz dBm/Hz dBm/Hz dBm/Hz
Tx Offset Noise - 1900 MHz[3] ±12.5 MHz Offset Noise + 80 MHz Offset Noise	 W-CDMA Modulation, Pout = 8 dBm W-CDMA Modulation, Pout = 0 dBm W-CDMA Modulation, Pout = 8 dBm W-CDMA Modulation, Pout = 0 dBm	 —	 -122 -128 -132 -138	 -115 -126 -129 -134	 dBm/Hz dBm/Hz dBm/Hz dBm/Hz

Table 8. Tx Cascaded Performance[1] (continued)

Parameter	Condition	Min	Typical	Maximum	Unit
Tx Offset Noise - 1700 MHz[3]					
±12.5 MHz Offset Noise	W-CDMA Modulation, Pout = 8 dBm		-120	-115	dBm/Hz
	W-CDMA Modulation, Pout = 0 dBm	—	-127	-122	dBm/Hz
+ 95 MHz Offset Noise	W-CDMA Modulation, Pout = 8 dBm		-133	-126	dBm/Hz
	W-CDMA Modulation, Pout = 0 dBm		-138	-134	dBm/Hz
Tx Offset Noise - 900 MHz[3]					
±12.5 MHz Offset Noise	W-CDMA Modulation, Pout = 8 dBm		-126	-119	dBm/Hz
	W-CDMA Modulation, Pout = 0 dBm	—	-129	-126	dBm/Hz
±45 MHz Offset Noise	W-CDMA Modulation, Pout = 8 dBm		-133	-127	dBm/Hz
	W-CDMA Modulation, Pout = 0 dBm		-137	-132	dBm/Hz
Tx Offset Noise - 800 MHz[3]					
±12.5 MHz Offset Noise	W-CDMA Modulation, Pout = 7.5 dBm		-123	-119	dBm/Hz
	W-CDMA Modulation, Pout = 0 dBm	—	-129	-126	dBm/Hz
±45 MHz Offset Noise	W-CDMA Modulation, Pout = 7.5 dBm		-131	-127	dBm/Hz
	W-CDMA Modulation, Pout = 0 dBm		-137	-132	dBm/Hz
Spectrum Emission 2.5 MHz to 3.5MHz Offset[4]	W-CDMA Modulation 1700, 1900, and 2100 bands - Pout = -10 to 8 dBm 850 and 900 bands - Pout = -10 to 7.5 dBm	—	-56	-45	dBc/ 30 KHz
Spectrum Emission 3.5 MHz to 7.5 MHz Offset[4]	W-CDMA Modulation 1700, 1900, and 2100 bands - Pout = -10 to 8 dBm 850 and 900 bands - Pout = -10 to 7.5 dBm	—	-56	-45	dBc/ 1 MHz
Spectrum Emission 7.5 MHz to 8.5 MHz Offset[4]	W-CDMA Modulation 1700, 1900, and 2100 bands - Pout = -10 to 8 dBm 850 and 900 bands - Pout = -10 to 7.5 dBm	—	-62	-49	dBc/ 1 MHz
Spectrum Emission 8.5 MHz to 12.5 MHz Offset[4]	W-CDMA Modulation 1700, 1900, and 2100 bands - Pout = -10 to 8 dBm 850 and 900 bands - Pout = -10 to 7.5 dBm	—	-62	-59	dBc/ 1 MHz
Spurious—All Spurs, Except Harmonics of RF Frequency	W-CDMA Modulation 1700, 1900, and 2100 bands - Pout = 8 dBm 850 and 900 bands - Pout = 7.5 dBm	—	—	-50	dBm/ 1 MHz
Spurious—Harmonics of RF Frequency	W-CDMA Modulation 1700, 1900, and 2100 bands - Pout = 8 dBm 850 and 900 bands - Pout = 7.5 dBm	—	—	-10	dBm/ 1 MHz

1 Output externally matched. (A 50 ohm load must be presented to the Tx output for optimal ACLR performance).

2 Specifications listed are after a closed loop DCOC has been performed.

3 Varies 0.6 dB/dB with output power. (Valid over -5 to +5 dBm output power range).

4 Dominated by linearity and noise of the modulation scheme.

5.4 GSM/EGPRS Transmitter Performance

5.4.1 2G Tx Performance

Table 9. Tx Performance

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
GSM850					
Tx Output Impedance DVGA Mode	50 Ohm nominal	—	“2:1”	—	VSWR
Tx Output Power EDGE	DVGA set to minimum attenuation	0		2.95	dBm
DVGA Range		42	45	48	dB
DVGA Incremental Step Size	Across DVGA range	2.2	3	4.5	dB
ACPR 8PSK ±200 kHz	MOD ORFS - Modulate with 8PSK random data and measure ACPR at various offsets	—	-36	-33	dBref/30 kHz
ACPR 8PSK ± 400 kHz		—	-70	-65	dBref/30 kHz
ACPR 8PSK ± 600 kHz		—	-82	-70	dBref/30 kHz
ACPR 8PSK ± 1800 kHz		—	-85	-73	dBref/100 kHz
ACPR 8PSK ± 3000 kHz		—	-97	-75	dBref/100 kHz
ACPR 8PSK ± 6000 kHz		—	-103	-81	dBref/100 kHz
Phase noise ±10 MHz offset - 8PSK	*** Test condition for Phase noise 10MHz, 20MHz offset. ***	—	—	-156	dBc/Hz
Phase noise ±20 MHz offset - 8PSK	DVGA=bypassed, 0dB, -3dB, -6dB	—	—	-160	dBc/Hz
EVM in 8PSK Mode	DVGA Backoff = 0 dB. System corrected but without remodulation effects	—	1	3	rms %
EVM in 8PSK Mode	DVGA Backoff = 0 dB. System corrected but without remodulation effects	—	3	12	peak %
Tx Output Impedance GSM Bypass Mode	—	—	—	“2:1”	—
Tx Output Power GSM	—	5	—	8	dBm

Table 9. Tx Performance (continued)

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
ACPR GMSK ± 200 kHz	MOD ORFS - Modulate with GMSK random data & measure ACPR at various offsets	—	-36	-33	dBref/30 kHz
ACPR GMSK ± 400 kHz		—	-70	-65	dBref/30 kHz
ACPR GMSK ± 600 kHz		—	-82	-70	dBref/30 kHz
ACPR GMSK ± 1800 kHz		—	-85	-73	dBref/100 kHz
ACPR GMSK ± 3000 kHz		—	-97	-75	dBref/100 kHz
ACPR GMSK ± 6000 kHz		—	-103	-81	dBref/100 kHz
Phase noise ±10 MHz offset - GMSK	*** Test condition for Phase noise 10MHz, 20MHz offset. ***	—	—	-159	dBc/Hz
Phase noise ±20 MHz offset - GMSK	DVGA=bypassed, 0dB, -3dB, -6dB	—	—	-166	dBc/Hz
Global Phase Error in GMSK Mode	—	—	0.6	2	rms deg
Global Phase Error in GMSK Mode	—	—	2.5	7	peak deg
Spurious output - Harmonics	All output power levels	—	-23	-10	dBc
Spurious output - Non-harmonics (spurious leakage level)	All output power levels	—	—	-77	dBm
Performance into load mismatch	—	—	—	TBD	—
GSM900					
Tx Output Impedance DVGA Mode	50 Ohm nominal	–	“2:1”	–	VSWR
Tx Output Power EDGE	DVGA set to minimum attenuation	0	—	2.95	dBm
DVGA Range	—	42	45	48	dB
DVGA Incremental Step Size	Across DVGA range	2.2	3	4.5	dB

Table 9. Tx Performance (continued)

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
ACPR 8PSK ±200 kHz	MOD ORFS - Modulate with 8PSK random data and measure ACPR at various offsets	—	-36	-33	dBref/30 kHz
ACPR 8PSK ± 400 kHz		—	-70	-65	dBref/30 kHz
ACPR 8PSK ± 600 kHz		—	-82	-70	dBref/30 kHz
ACPR 8PSK ± 1800 kHz		—	-85	-73	dBref/100 kHz
ACPR 8PSK ± 3000 kHz		—	-97	-75	dBref/100 kHz
ACPR 8PSK ± 6000 kHz		—	-103	-81	dBref/100 kHz
Phase Noise ±10 MHz offset - 8PSK	*** Test condition for Phase noise 10MHz, 20MHz offset. ***	—	—	-156	dBc/Hz
Phase Noise ±20 MHz offset - 8PSK	DVGA=bypassed, 0dB, -3dB, -6dB	—	—	-160	dBc/Hz
EVM in 8PSK Mode	DVGA Backoff = 0 dB. System corrected but without remodulation effects	—	0.9	3	rms %
EVM in 8PSK Mode	DVGA Backoff = 0 dB. System corrected but without remodulation effects	—	2.8	12	peak %
Tx Output Impedance GSM Bypass Mode		—	—	“2:1”	—
Tx Output Power GSM		5	—	8	dBm
ACPR GMSK ± 200 kHz	MOD ORFS - Modulate with GMSK random data and measure ACPR at various offsets	—	-36	-33	dBref/30 kHz
ACPR GMSK ± 400 kHz		—	-70	-65	dBref/30 kHz
ACPR GMSK ± 600 kHz		—	-82	-70	dBref/30 kHz
ACPR GMSK ± 1800 kHz		—	-85	-73	dBref/100 kHz
ACPR GMSK ± 3000 kHz		—	-97	-75	dBref/100 kHz
ACPR GMSK ± 6000 kHz		—	-103	-81	dBref/100 kHz
Phase Noise ±10 MHz offset - GMSK	*** Test condition for Phase noise 10MHz, 20MHz offset. ***	—	—	-159	dBc/Hz
Phase Noise ±20 MHz offset - GMSK	DVGA=bypassed, 0dB, -3dB, -6dB	—	—	-166	dBc/Hz
Global Phase Error in GMSK Mode		—	0.6	2	rms deg
Global Phase Error in GMSK Mode		—	2.7	7	peak deg
Spurious output - Harmonics	All output power levels	—	-24	-10	dBc
Spurious output - Non-harmonics (spurious leakage level)	All output power levels	—	—	-77	dBm

Table 9. Tx Performance (continued)

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
Performance into load mismatch	—	—	—	TBD	—
GSM1800					
Tx Output Impedance DVGA Mode	50 Ohm nominal	—	“2:1”	—	VSWR
Tx Output Power EDGE	DVGA set to minimum attenuation	0	—	2.35	dBm
DVGA Range		42	45	48	dB
DVGA Incremental Step Size	Across DVGA range	2.2	3	4.5	dB
ACPR 8PSK ±200 kHz	MOD ORFS - Modulate with 8PSK random data and measure ACPR at various offsets	—	-37	-33	dBref/30 kHz
ACPR 8PSK ± 400 kHz		—	-68	-65	dBref/30 kHz
ACPR 8PSK ± 600 kHz		—	-77	-70	dBref/30 kHz
ACPR 8PSK ± 1800 kHz		—	-82	-75	dBref/100 kHz
ACPR 8PSK ± 6000 kHz		—	-96	-75	dBref/100 kHz
Phase Noise ±20 MHz offset - 8PSK	** Test condition for Phase noise 20MHz offset ** DVGA=bypassed, 0dB	—	—	-156	dBc/Hz
EVM in 8PSK Mode	DVGA Backoff = 0 dB. System corrected but without remodulation effects	—	1.7	3	rms %
EVM in 8PSK Mode	DVGA Backoff = 0 dB. System corrected but without remodulation effects	—	5	12	peak %
Tx Output Impedance GSM Bypass Mode		—	—	“2:1”	—
Tx Output Power GSM		5	—	8	dBm
ACPR GMSK ± 200 kHz	MOD ORFS - Modulate with GMSK random data and measure ACPR at various offsets	—	-37	-33	dBref/30 kHz
ACPR GMSK ± 400 kHz		—	-68	-65	dBref/30 kHz
ACPR GMSK ± 600 kHz		—	-72	-70	dBref/30 kHz
ACPR GMSK ± 1800 kHz		—	-82	-75	dBref/100 kHz
ACPR GMSK ± 6000 kHz		—	-96	-75	dBref/100 kHz
Phase Noise ±20 MHz offset - GMSK	** Test condition for Phase noise 20MHz offset. ** DVGA=bypassed, 0dB	—	—	-160	dBc/Hz
Global Phase Error in GMSK Mode	—	—	0.6	3	rms deg
Global Phase Error in GMSK Mode	—	—	2.7	10	peak deg

Table 9. Tx Performance (continued)

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
Spurious output - Harmonics	All output power levels	—	-27	-10	dBc
Spurious output - Non-harmonics (spurious leakage level)	All output power levels	—	—	-77	dBm
Performance into load mismatch		—	—	TBD	—
GSM1900					
Tx Output Impedance DVGA Mode	50 Ohm nominal	—	“2:1”	—	VSWR
Tx Output Power EDGE	DVGA set to minimum attenuation	0		2.35	dBm
DVGA Range		42	45	48	dB
DVGA Incremental Step Size	Across DVGA range	2.2	3	4.5	dB
ACPR 8PSK ±200 kHz	MOD ORFS - Modulate with 8PSK random data and measure ACPR at various offsets	—	-36	-33	dBref/30 kHz
ACPR 8PSK ± 400 kHz		—	-69	-65	dBref/30 kHz
ACPR 8PSK ± 600 kHz		—	-77	-70	dBref/30 kHz
ACPR 8PSK ± 1800 kHz		—	-81	-75	dBref/100 kHz
ACPR 8PSK ± 6000 kHz		—	-94	-75	dBref/100 kHz
Phase Noise ±20 MHz offset - 8PSK	** Test condition for Phase noise 20MHz offset. ** DVGA=bypassed, 0dB	—	—	-156	dBc/Hz
EVM in 8PSK Mode	DVGA Backoff = 0 dB. System corrected but without remodulation effects	—	1.5	3	rms %
EVM in 8PSK Mode	DVGA Backoff = 0 dB. System corrected but without remodulation effects	—	6	12	peak %
Tx Output Impedance GSM Bypass Mode		—	“2:1”	—	—
Tx Output Power GSM		5	—	8	dBm
ACPR GMSK ± 200 kHz	Modulate with GMSK random data and measure ACPR at various offsets	—	-36	-33	dBref/30 kHz
ACPR GMSK ± 400 kHz		—	-69	-65	dBref/30 kHz
ACPR GMSK ± 600 kHz		—	-77	-70	dBref/30 kHz
ACPR GMSK ± 1800 kHz		—	-81	-75	dBref/100 kHz
ACPR GMSK ± 6000 kHz		—	-94	-75	dBref/100 kHz
Phase Noise ±20 MHz offset - GMSK	** Test condition for Phase noise 20MHz offset. ** DVGA=bypassed, 0dB	—	—	-160	dBc/Hz

Table 9. Tx Performance (continued)

Specification Name/Parameter	Conditions	Min	Typ	Max	Units
Global Phase Error in GMSK Mode	—	—	0.8	2	rms deg
Global Phase Error in GMSK Mode	—	—	2.9	10	peak deg
Spurious output - Harmonics	—	—	-34	-10	dBc
Spurious output - Non-harmonics (spurious leakage level)	—	—	-77	dBm	—
Performance into load mismatch	—	—	—	TBD	—

6 MMM7210 Applications Circuit

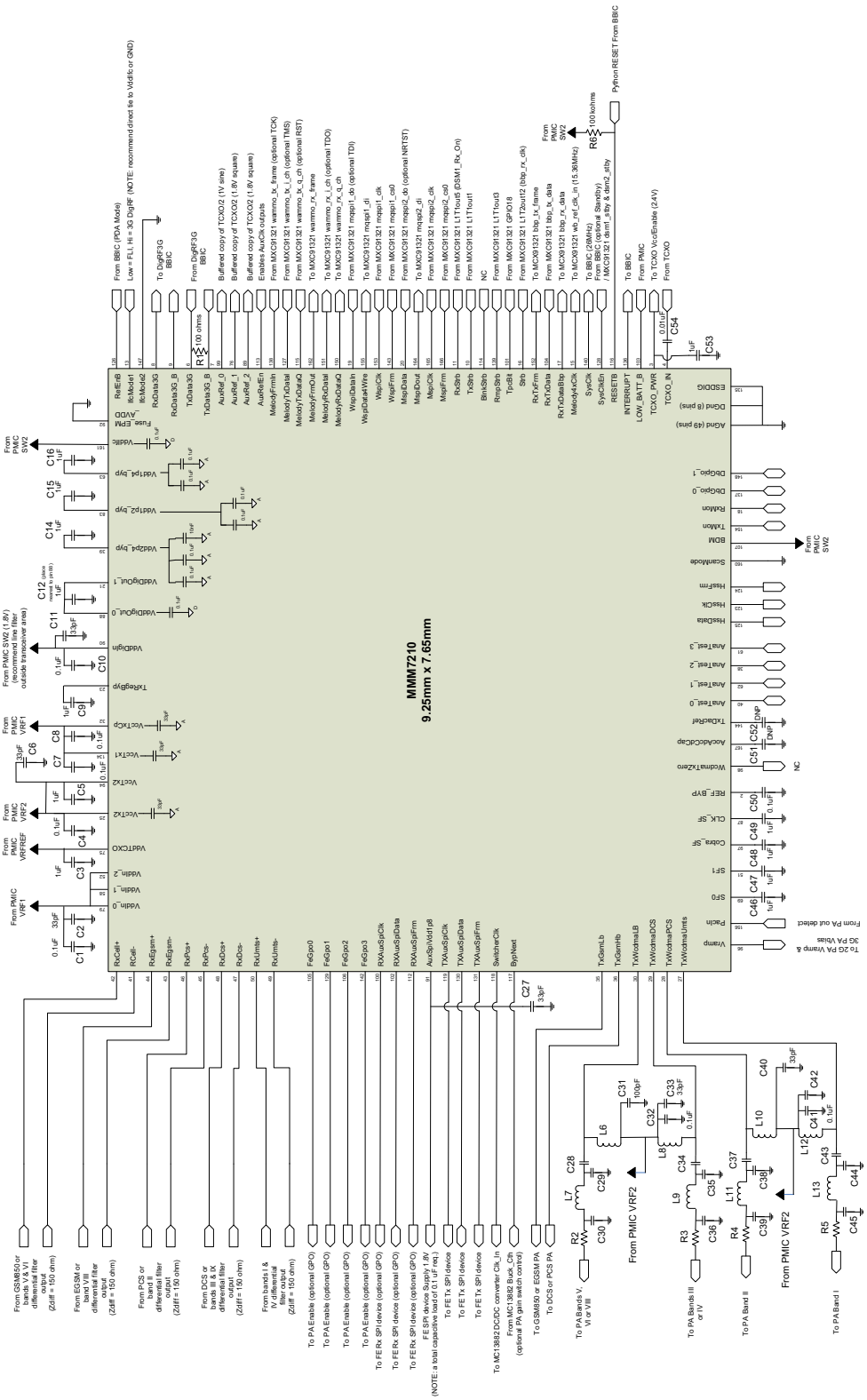


Figure 2. MMM7210 Applications Schematic

Table 10. MMM7210 Applications Schematic Bill of Materials

Reference Designator	Value	Description
C1	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C2	33pF	CAP, 33PF, 16V, Ceramic, 0402
C3	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C4	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C5	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C6	33pF	CAP, 33PF, 16V, Ceramic, 0402
C7	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C8	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C9	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C10	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C11	33pF	CAP, 33PF, 16V, Ceramic, 0402
C12	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C13	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C14	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C15	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C16	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C27	33pF	CAP, 33PF, 16V, Ceramic, 0402
[1]C28	33pF	CAP, 33PF, 16V, Ceramic, 0402
[1]C29	1.0pF	CAP, 1.0PF, 16V, Ceramic, 0402
C30	DNP	CAP, DNP, 16V, Ceramic, 0402
[1]L6	22nH	IND, 22NH, 2%, 400mA, 0402
[1]L7	18nH	IND, 18NH, 2%, 560mA, 0402
C31	100pF	CAP, 100PF, 16V, Ceramic, 0402
C32	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C33	33pF	CAP, 33PF, 16V, Ceramic, 0402
[1]L8	10nH	IND, 10NH, 2%, 400mA, 0402
[1]L9	5.6nH	IND, 5.6NH, 2%, 800mA, 0402
[1]C34	33pF	CAP, 33PF, 16V, Ceramic, 0402
[1]C35	DNP	CAP, DNP, 16V, Ceramic, 0402
[1]C36	DNP	CAP, DNP, 16V, Ceramic, 0402
[1]L10	4.7nH	IND, 4.7NH, 2%, 400mA, 0402
[1]L11	0ohm	RES, 0ohm, 1/16W, 5%, 0402

Table 10. MMM7210 Applications Schematic Bill of Materials (continued)

Reference Designator	Value	Description
[1]C37	33pF	CAP, 33PF, 16V, Ceramic, 0402
[1]C38	DNP	CAP, DNP, 16V, Ceramic, 0402
[1]C39	DNP	CAP, DNP, 16V, Ceramic, 0402
C40	33pF	CAP, 33PF, 16V, Ceramic, 0402
C41	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C42	DNP	CAP, DNP, 16V, Ceramic, 0402
[1]L12	3.3nH	IND, 3.3NH, 2%, 400mA, 0402
[1]L13	0ohms	RES, 0ohm, 1/16W, 5%, 0402
[1]C43	33pF	CAP, 33PF, 16V, Ceramic, 0402
[1]C44	DNP	CAP, DNP, 16V, Ceramic, 0402
[1]C45	DNP	CAP, DNP, 16V, Ceramic, 0402
C46	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C47	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C48	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C49	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C50	0.1uF	CAP, 0.1UF, 16V, Ceramic, 0402
C51	DNP	CAP, DNP, Ceramic, 0402
C52	DNP	CAP, DNP, Ceramic, 0402
C53	1.0uF	CAP, 1.0UF, 6.3V, Ceramic, 0402
C54	0.01uF	CAP, 0.01UF, 16V, Ceramic, 0402
R1	200ohms	RES, 200ohm, 1/16W, 5%, 0402
[1]R2	0ohms	RES, 0ohm, 1/16W, 5%, 0402
[1]R3	0ohms	RES, 0ohm, 1/16W, 5%, 0402
[1]R4	0ohms	RES, 0ohm, 1/16W, 5%, 0402
[1]R5	0ohms	RES, 0ohm, 1/16W, 5%, 0402
R6	10 kohms	RES, 10 kohm, 1/16W, 5%, 0402

[1] Final value may differ upon MMM7210 matching optimization.

7 Package Information and Pinout

The MMM7210 is a 9.25 mm × 7.65 mm package and is shown in Figure 3 and Figure 4. Figure 5 shows the pinout for the MMM7210 and Figure 6 shows the pin map.

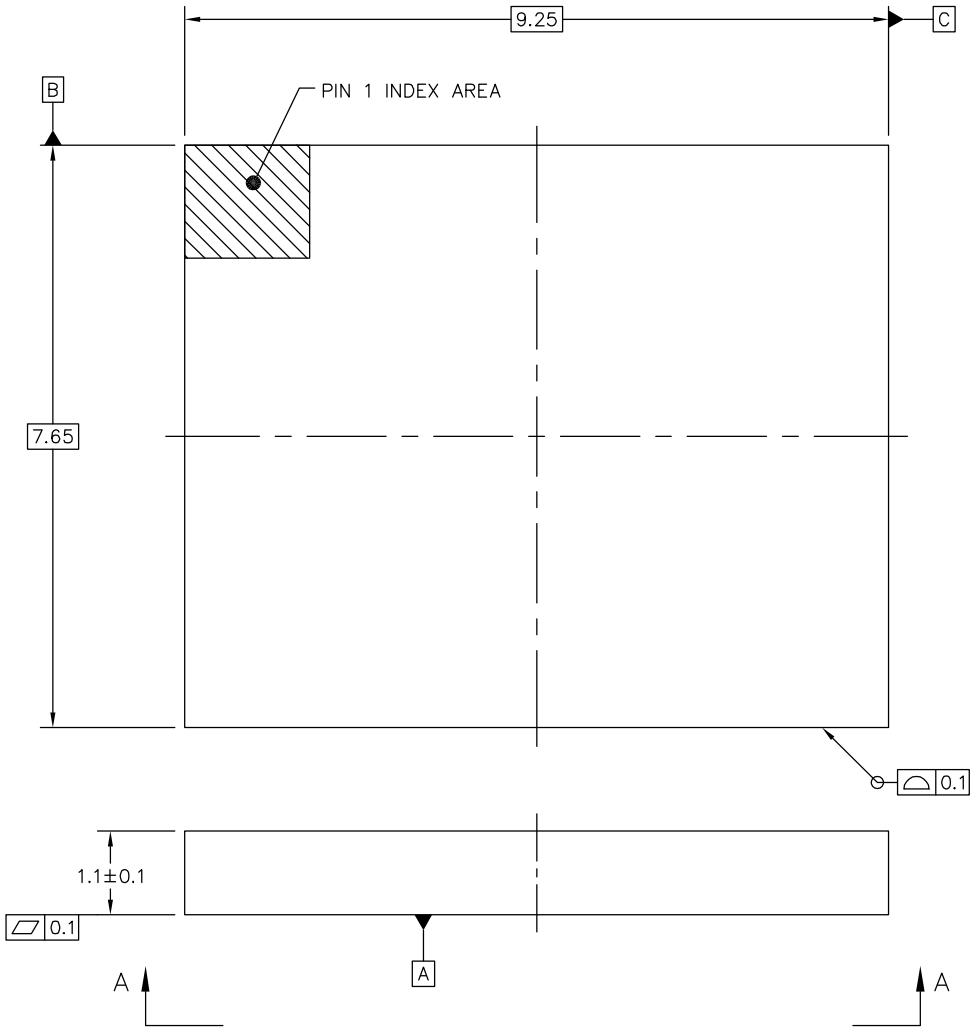
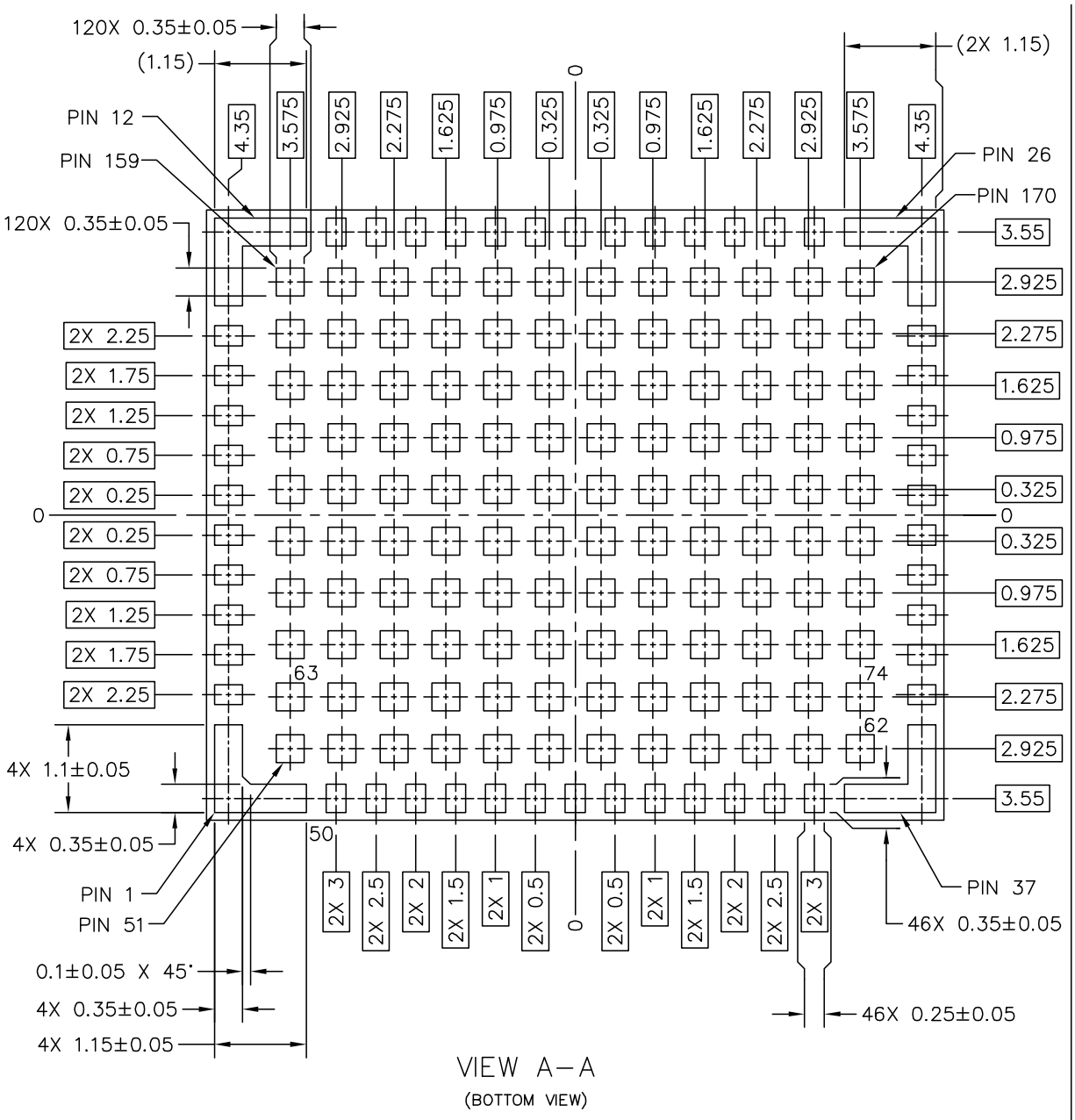


Figure 3. MMM7210 Package Drawing (Top View)



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. ⌖ 0.1Ⓜ A B C / 0.05Ⓜ A APPLIES TO ALL PAD LOCATIONS.

Figure 4. MMM7210 Package Drawing (Bottom View)

Figure 5. MMM7210 Pinout (Top View)

NOTES

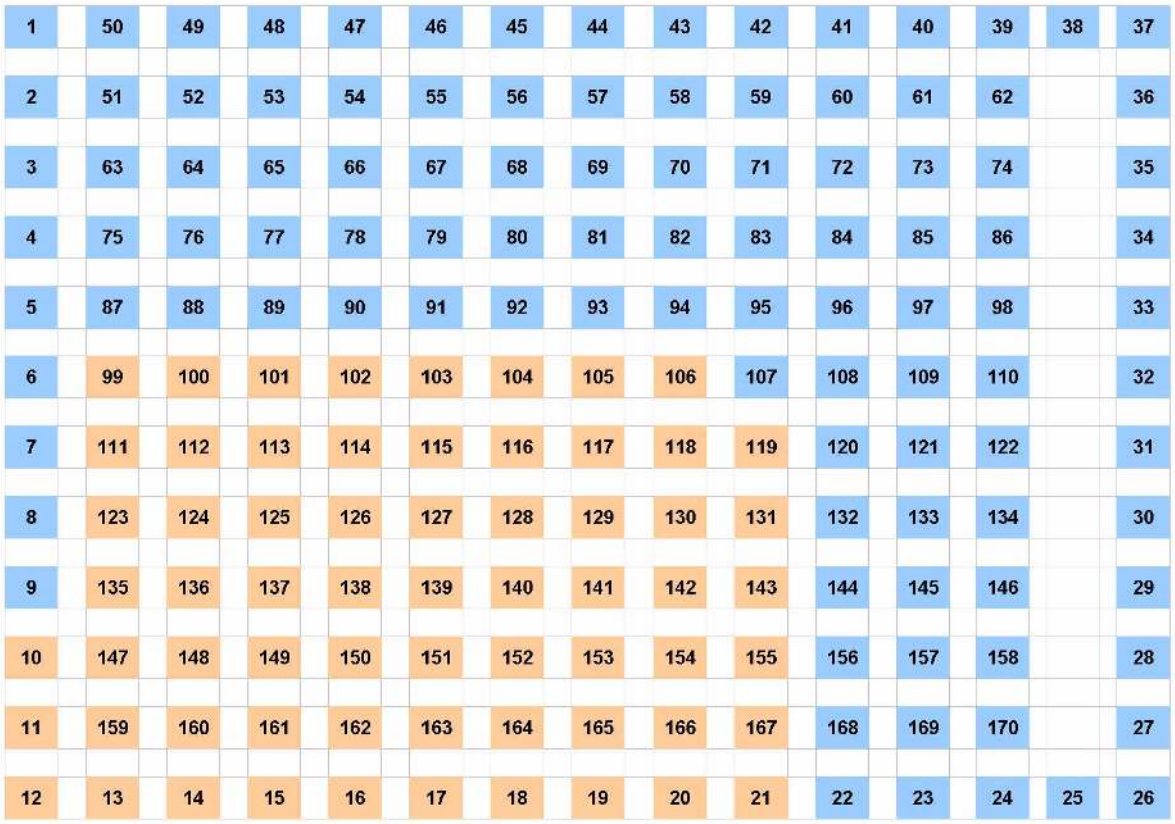


Figure 6. MMM7210 Pin Map (Top View)

8 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

Table 11 summarizes revisions made to this document since Rev. 2.1 was released.

Table 11. Revision History

Location	Revision
Introduction	Provided more detailed introduction. Updates to block diagram.

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