M210x Series

5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/CMOS, Clock Oscillator

FEATURES

Frequencies from 50 MHz to 1.4 GHz
Featuring QiK Chip™ Technology
RF Output: LVPECL/LVDS/CML/CMOS
Tight stability ±20ppm over -40°C to +85°C
Wide operating temperature option available, -55°C to +105°C & -55 to +125C
Superior Jitter Performance (less than 0.25 ps RMS, 12 kHz - 20 MHz)
Operating Voltage: 1.8/2.5/3.3 V

APPLICATIONS

Military Communications
Clock and Data Recovery
SD/HD Video
FPGA/ASIC Clock Generation
Test and Measurement Equipment

ORDERING INFORMATION

M210x	2	8	B	P	C	00.0000 MHz

Product Series
0: 3.3 V
1: 2.5 V
2: 1.8 V

Temperature Range
1: 0°C to +70°C
6: -20°C to +70°C
2: -40°C to +85°C
3: -55°C to +105°C
4: -55°C to +125°C

Stability
3: ± 100 ppm
4: ± 50 ppm
6: ± 25 ppm
8: ± 20 ppm

Enable/Disable Function
B: Enable High (Pin 1)
S: Enable Low (Pin 1)
U: No Enable/Disable Function
G: Enable High (Pin 2)
M: Enable Low (Pin 2)

Output Type
P: LVPECL
M: CML
L: LVDS
C :CMOS

Package/Lead Configurations
N: Leadless Ceramic (9 Pad)
C: Leadless Ceramic (6 Pad)

Example Part Number: M210028BPC 100.0000 MHz

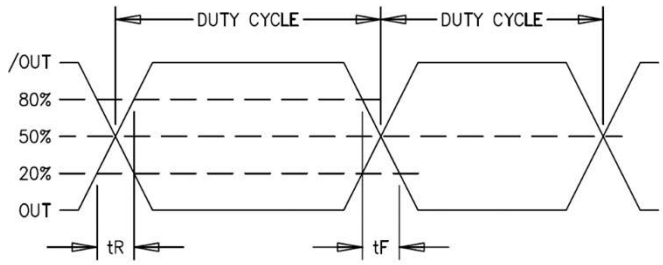
ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency Range	F_0	10 10		1400 135	MHz MHz	LVPECL, LVDS, CML CMOS
Frequency Stabilities						
vs. Operating Temperature	$\Delta F/F$	See ordering information			ppm	[1]
vs. Aging		-3.0 -1.0		+3.0 +1.0	ppm Ppm	1st year Per year after 1st year
RF Output						
Output Type		LVDS/CML/PCEL/CMOS				
Output Load		50 Ohms to (V_{CC} -2) Vdc 100 Ohm differential load 15pF				LVPECL[2] LVDS/CML[2] CMOS[2]
Symmetry (duty cycle)	T_{DC}	45 45 45		55 55 55	%	LVPEL: 50% of waveform LVDS: @ 1.25V CMOS: @ 50% of V_{DD}
Logic "1" Level	V_{OH}	Vcc-1.02 90%V_{DD}			V V	LVPECL CMOS
Logic "0" Level	V_{OL}			Vcc – 1.63 10%V_{DD}	V V	LVPECL CMOS
Differential Output Voltage		250	350	450	mV	LVDS Load
Output Voltage Level		1.1		1.9	V_{pk-pk}	CML
Output Skew			20 15 20		ps ps ps	LVPECL CML LVDS
Common Mode Voltage			1.2		V	LVDS Output
Rise/Fall Time	T_R/T_F		0.23	0.50 6.0	ns ns	LVPECL, LVDS, CML CMOS
Start-up Time	T_{SU}			10	ms	
Other Parameters						
Phase Jitter (RMS) @622.08 MHz	Φ_J		0.25		ps	Integrated 12 kHz – 20 MHz
Enable/Disable						
Enable/Disable Logic (Option B or G)		80% V_{CC}		 0.35	V V	Output Enabled Options Output disabled to HIGH Z
Enable/Disable Logic (Option S or M)		 80% V_{CC}		0.35	V V	Output Enabled Options Output disabled to HIGH Z
Operating Voltage and Current						
Operating Voltage	V_{CC} or V_{DD}	3.135	3.300	3.465	V	M2100
		2.375	2.500	2.625	V	M2101
		1.710	1.800	1.890	V	M2102
Operating Current	I_{CC}			125	mA	LVPECL
				100	mA	LVDS
				110	mA	CML
	I_{DD}			90	mA	CMOS
Notes						
Note 1	Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.					
Note 2	Refer to the load circuit diagram in this data sheet.					

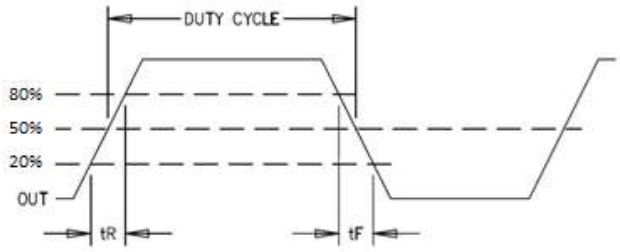
ENVIRONMENTAL CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature	TA	See ordering information			°C	
Storage Temperature	TS	-55		+125	°C	
Shock	Per MIL-STD-202, Method 213, Condition C					
Vibration	Per MIL-STD-202, Methods 201 & 204					
Solderability	Per EIAJ-STD-002					
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10-8 atm cc/s of helium)					
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A					
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B					

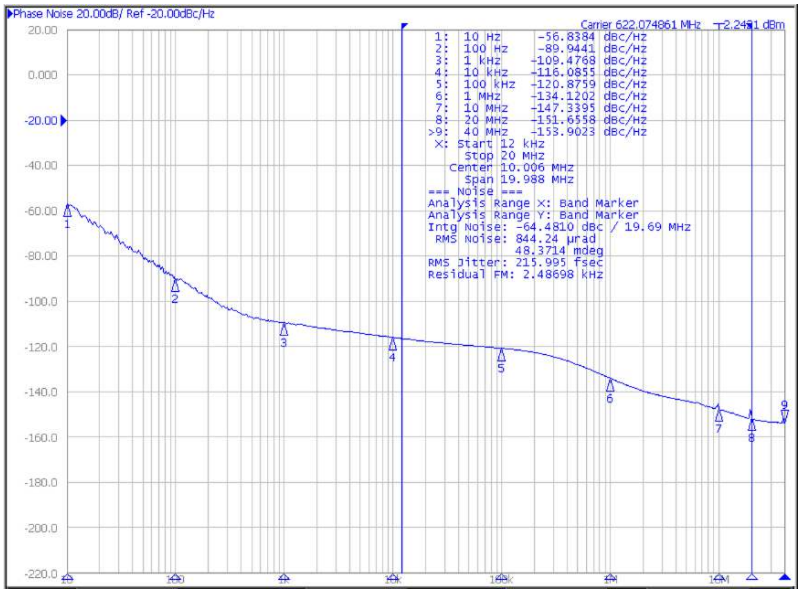
OUTPUT WAVEFORM (LVPECL, LVDS, CML)



OUTPUT WAVEFORM (CMOS)



PHASE NOISE PLOT (@ 622.08MHz)



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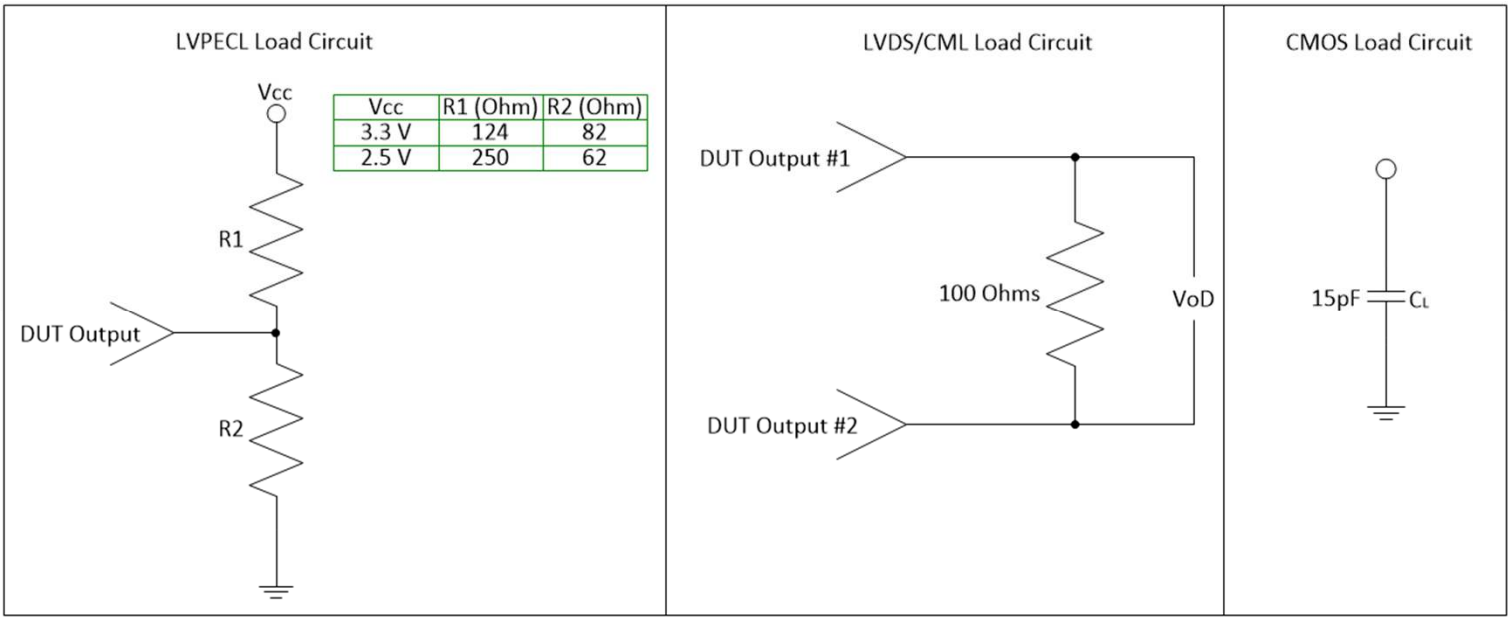
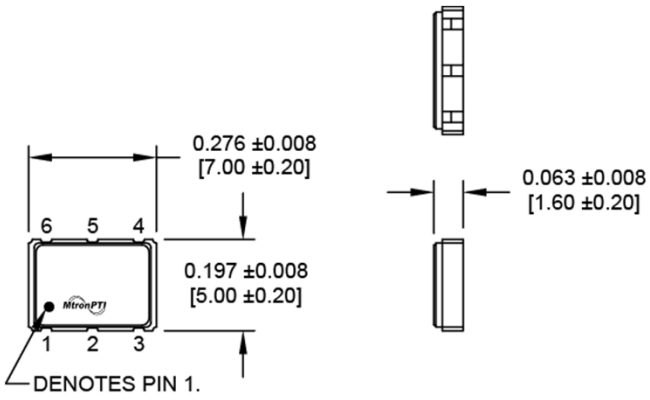
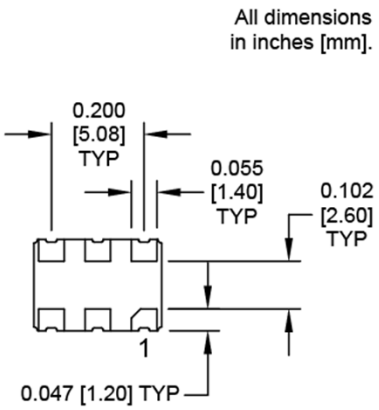
LOAD CIRCUIT DIAGRAMS

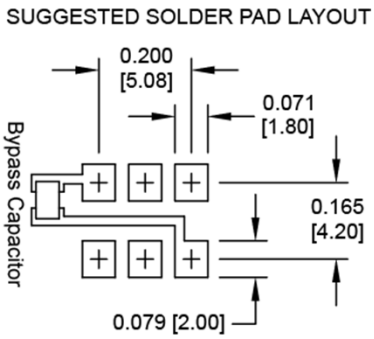


MECHANICAL AND PIN OUT INFORMATION (6-pad package)

Pad	Function
1	Enable/Disable, Voltage Control or N/C
2	Enable/Disable, Voltage Control or N/C
3	Ground
4	Output Q (LVPECL, LVDS, CML, CMOS)
5	Output $\bar{Q}$ (LVPECL, LVDS, CML)
6	Supply Vcc+

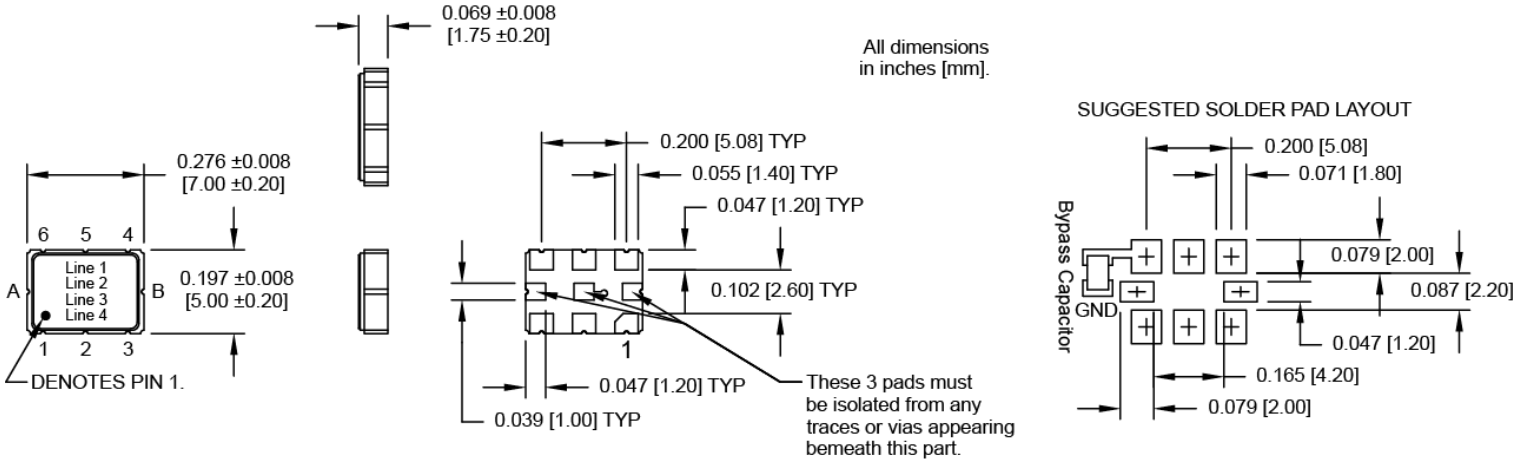






MECHANICAL AND PIN OUT INFORMATION (9-pad package)

Pad	Function
1	Enable/Disable, Voltage Control or N/C
2	Enable/Disable, Voltage Control or N/C
3	Ground
4	Output Q (LVPECL, LVDS, CML, CMOS)
5	Output $\bar{Q}$ (LVPECL, LVDS, CML)
6	Supply Vcc+
A	Do not connect
B	Do not connect
C	Do not connect



HANDLING INFORMATION

Although protection circuitry has been designed into the M210x oscillator, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. MtronPTI utilizes a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation.

ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industrywide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Model	ESD Threshold, Minimum	Unit
Human Body	1500*	V
Charged Device	1500*	V

*MIL-STD-883D, Method 3015, Class 1

ATTENTION
Static Sensitive
Devices
Handle only at
Static Safe Work
Stations

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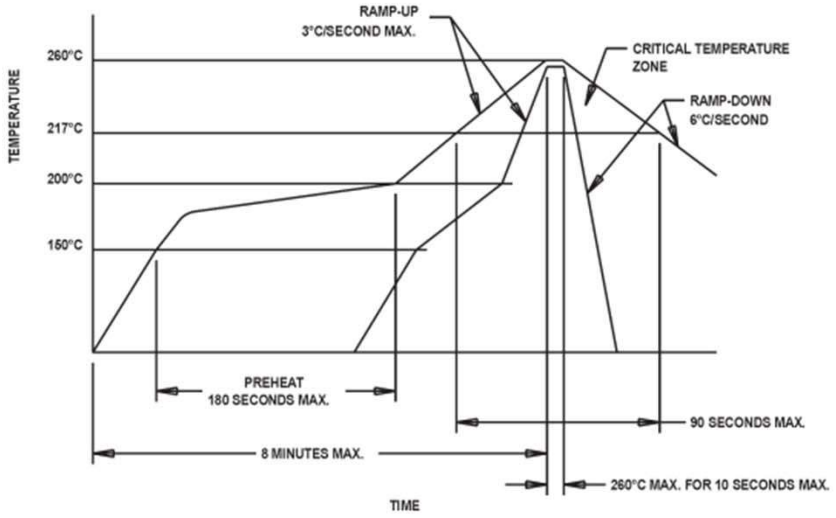
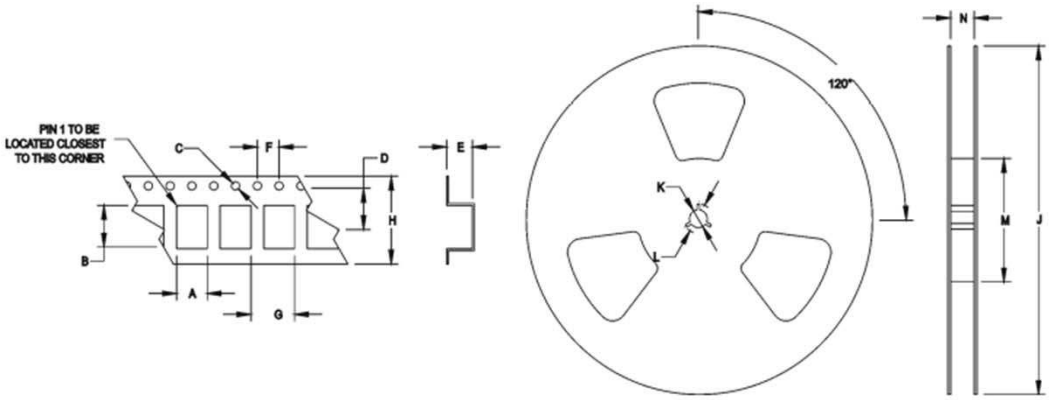
LEAD FREE SOLDER PROFILE



Solder Conditions
Note: Exceeding these limits may damage the device.

TAPE AND REEL SPECIFICATIONS



Standard Tape and Reel: 1000 parts per reel

A	B	C	D	E	F	G	H	J	K	L	M
6.51	9.29	1.5	7.5	2.8	4	8/12	16	180-330	13	21	60-100

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