MAX803 Series, NCP803 Series

Very Low Supply Current 3-Pin Microprocessor Reset Monitor

The MAX803/NCP803 is a cost−effective system supervisor circuit designed to monitor V_{CC} in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 10 μsec of V_{CC} falling through the reset voltage threshold. Reset is maintained active for a timeout period which is trimmed by the factory after V_{CC} rises above the reset threshold. The MAX803/NCP803 has an open drain active−low $\overline{\text{RESET}}$ output. Both devices are available in SOT−23 and SC−70 packages.

The MAX803/NCP803 is optimized to reject fast transient glitches on the V_{CC} line. Low supply current of 0.5 μA (V_{CC} = 3.2 V) make these devices suitable for battery powered applications.

Features

- Precision V_{CC} Monitor for 1.5 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.2 V to 4.9 V Available in 100 mV Steps
- Four Guaranteed Minimum Power−On Reset Pulse Width Available (1 ms, 20 ms, 100 ms, and 140 ms)
- $\overline{\text{RESET}}$ Output Guaranteed to V_{CC} = 1.0 V
- Low Supply Current
- V_{CC} Transient Immunity
- No External Components
- Wide Operating Temperature: −40°C to 105°C
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Computers
- Embedded Systems
- Battery Powered Equipment
- Critical Microprocessor Power Supply Monitoring

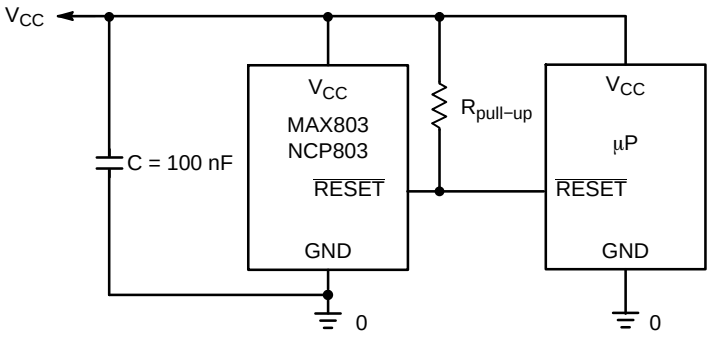

Figure 1. Typical Application Diagram

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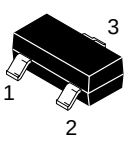
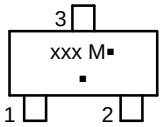
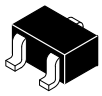
MARKING DIAGRAM

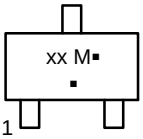


SOT−23 (TO−236) CASE 318





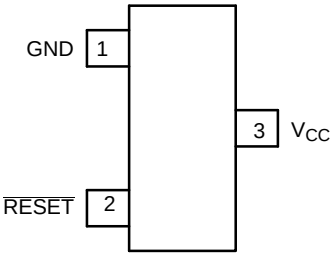
SC−70 (SOT−323) CASE 419



xxx = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION



SOT−23/SC−70

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

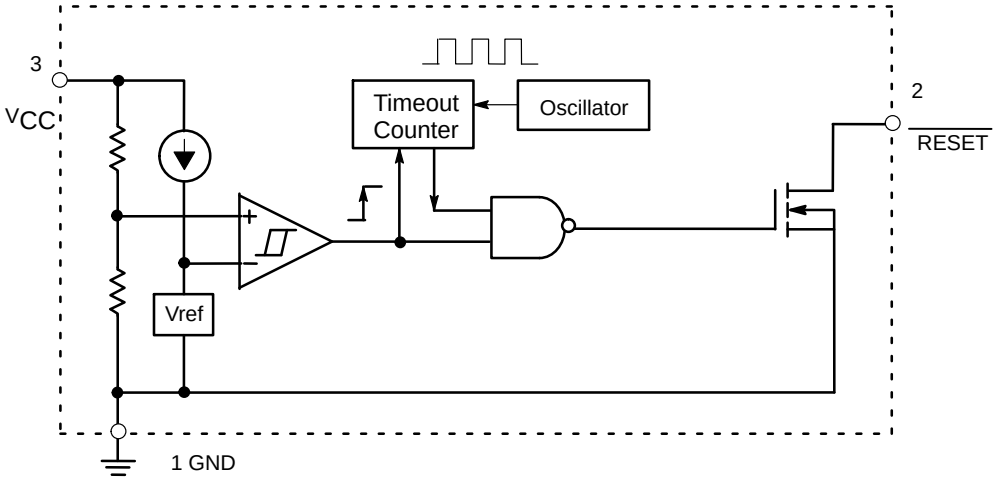


Figure 2. NCP803, MAX803 Series Open−Drain Active−Low Output

PIN DESCRIPTION

Pin No.	Symbol	Description
1	GND	Ground
2	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ output remains low while V_{CC} is below the reset voltage threshold, and for a reset timeout period after V_{CC} rises above reset threshold.
3	V_{CC}	Supply Voltage: C = 100 nF is recommended as a bypass capacitor between V_{CC} and GND.

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Power Supply Voltage (V_{CC} to GND)		V_{CC}	−0.3 to 6.0	V
RESET Output Voltage (CMOS)			−0.3 to (V_{CC} + 0.3)	V
Input Current, V_{CC}			20	mA
Output Current, $\overline{\text{RESET}}$			20	mA
dV/dt (V_{CC})			100	V/μsec
Thermal Resistance, Junction−to−Air (Note 1)	SOT−23 SC−70	$R_{\theta JA}$	301 314	°C/W
Operating Junction Temperature Range		T_J	−40 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)		T_{sol}	+260	°C
ESD Protection Human Body Model (HBM): Following Specification JESD22−A114 Machine Model (MM): Following Specification JESD22−A115			 2000 200	V
Latchup Current Maximum Rating: Following Specification JESD78 Class II	Positive Negative	$I_{Latchup}$	 200 200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This based on a 35x35x1.6mm FR4 PCB with 10mm^2 of 1 oz copper traces under natural convention conditions and a single component characterization.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150°C$$

ELECTRICAL CHARACTERISTICS T_A = −40°C to +105°C unless otherwise noted. Typical values are at T_A = +25°C. (Note 3)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Range					V
T_A = 0°C to +70°C		1.0	–	5.5	
T_A = −40°C to +105°C (Note 4)		1.2	–	5.5	
Supply Current	I_{CC}				μA
V_{CC} = 3.3 V					
T_A = −40°C to +85°C		–	0.5	1.2	
T_A = 85°C to +105°C (Note 5)		–	–	2.0	
V_{CC} = 5.5 V					
T_A = −40°C to +85°C		–	0.8	1.8	
T_A = 85°C to +105°C (Note 5)		–	–	2.5	
Reset Threshold (V_{in} Decreasing) (Note 6)	V_{TH}				V
MAX803SQ463/NCP803SN463					
T_A = +25°C		4.56	4.63	4.70	
T_A = −40°C to +85°C		4.51	–	4.75	
T_A = +85°C to +105°C (Note 5)		4.40	–	4.88	
MAX803SQ438/NCP803SN438					
T_A = +25°C		4.31	4.38	4.45	
T_A = −40°C to +85°C		4.27		4.49	
T_A = +85°C to +105°C (Note 5)		4.16		4.60	
NCP803SN400					
T_A = +25°C		3.94	4.00	4.06	
T_A = −40°C to +85°C		3.90		4.10	
T_A = +85°C to +105°C (Note 5)		3.80		4.20	
MAX803SQ308/NCP803SN308					
T_A = +25°C		3.04	3.08	3.11	
T_A = −40°C to +85°C		3.00	–	3.15	
T_A = +85°C to +105°C (Note 5)		2.92	–	3.23	
MAX803SQ293/NCP803SN293					
T_A = +25°C		2.89	2.93	2.96	
T_A = −40°C to +85°C		2.85	–	3.00	
T_A = +85°C to +105°C (Note 5)		2.78	–	3.08	
NCP803SN263					
T_A = +25°C		2.59	2.63	2.66	
T_A = −40°C to +85°C		2.55	–	2.70	
T_A = +85°C to +105°C (Note 5)		2.50	–	2.76	
NCP803SN232					
T_A = +25°C		2.29	2.32	2.35	
T_A = −40°C to +85°C		2.26	–	2.38	
T_A = +85°C to +105°C (Note 5)		2.20	–	2.45	
NCP803SN160					
T_A = +25°C		1.58	1.60	1.62	
T_A = −40°C to +85°C		1.56	–	1.64	
T_A = +85°C to +105°C (Note 5)		1.52	–	1.68	
MAX803SN120, MAX803SQ120					
T_A = +25°C		1.18	1.20	1.22	
T_A = −40°C to +85°C		1.17	–	1.23	
T_A = +85°C to +105°C (Note 5)		1.14	–	1.26	
Detector Voltage Threshold Temperature Coefficient		–	30	–	ppm/°C
V_{CC} to Reset Delay V_{CC} = V_{TH} to (V_{TH} − 100 mV)		–	10	–	μsec
Reset Active TimeOut Period (Note 6)	t_{RP}				msec
MAX803SN(Q)293D1		1.0	–	3.3	
MAX803SN(Q)293D2/MAX803SN(Q)308D2		20	–	66	
MAX803SN(Q)293D3		100	–	330	
MAX803SN(Q)293		140	–	460	
$\overline{\text{RESET}}$ Output Voltage Low	V_{OL}	–	–	0.3	V
V_{CC} = V_{TH} − 0.2 V					
1.6 V ≤ V_{TH} ≤ 2.0 V, I_{SINK} = 0.5 mA					
2.1 V ≤ V_{TH} ≤ 4.0 V, I_{SINK} = 1.2 mA					
4.1 V ≤ V_{TH} ≤ 4.9 V, I_{SINK} = 3.2 mA					
$\overline{\text{RESET}}$ Leakage Current V_{CC} > V_{TH}, $\overline{\text{RESET}}$ De−asserted	I_{LEAK}	–	–	1	μA

3. Production testing done at T_A = 25°C, over temperature limits guaranteed by design.
4. For NCV automotive devices, this temperature range is T_A = −40°C to +125°C.
5. For NCV automotive devices, this temperature range is T_A = +85°C to +125°C.
6. Contact your ON Semiconductor sales representative for other threshold voltage and timeout options.

TYPICAL OPERATING CHARACTERISTICS

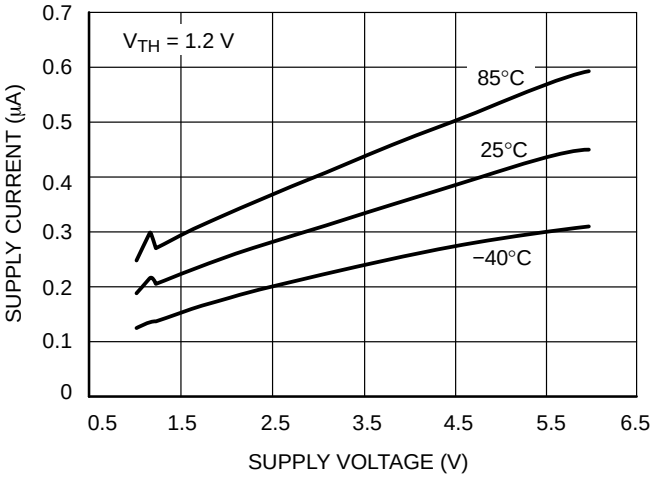


Figure 3. Supply Current vs. Supply Voltage

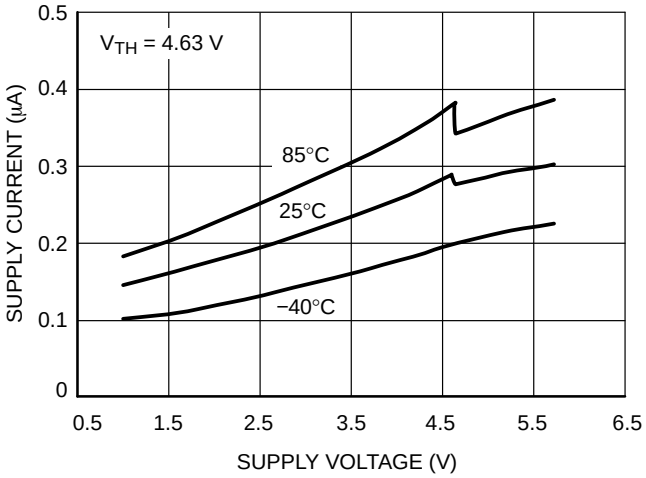


Figure 4. Supply Current vs. Supply Voltage

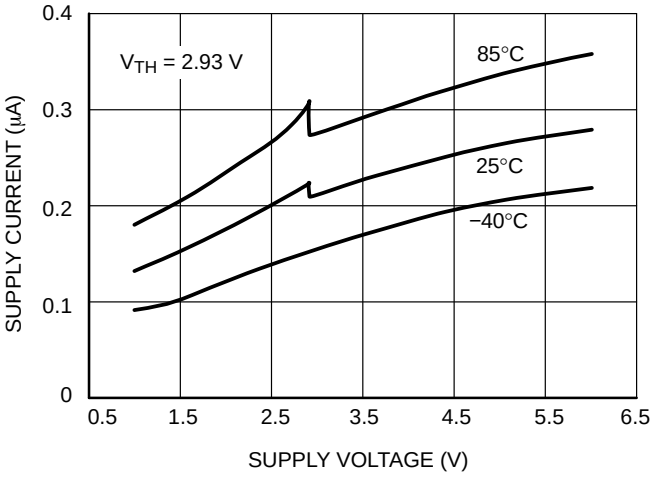


Figure 5. Supply Current vs. Supply Voltage

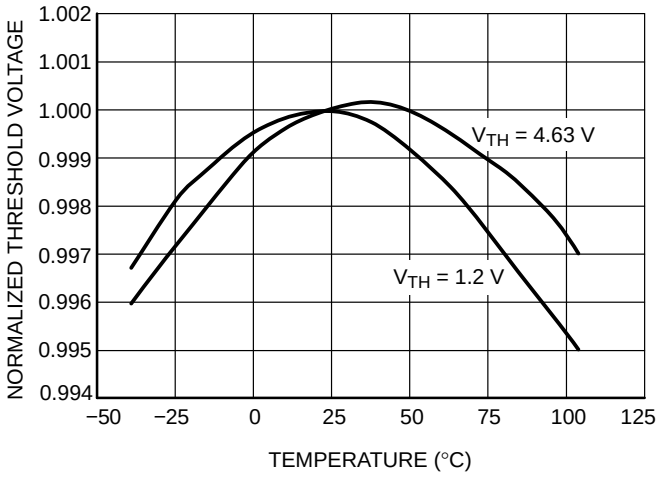


Figure 6. Normalized Reset Threshold Voltage vs. Temperature

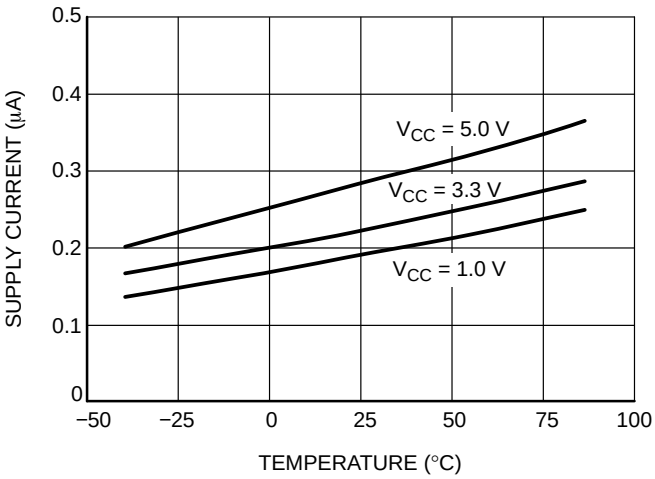


Figure 7. Supply Current vs. Temperature

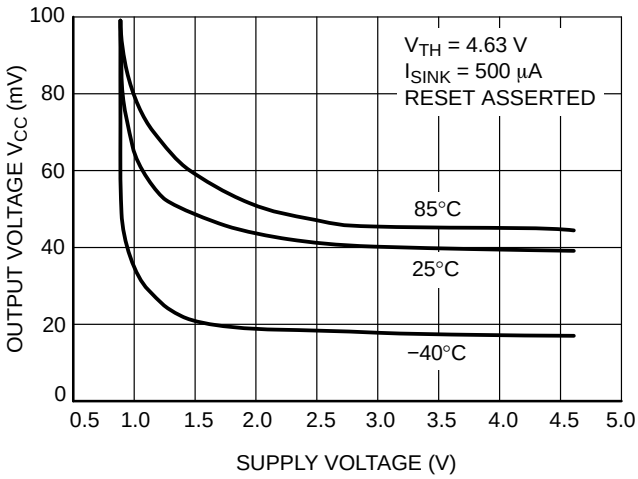


Figure 8. Output Voltage Low vs. Supply Voltage

TYPICAL OPERATING CHARACTERISTICS

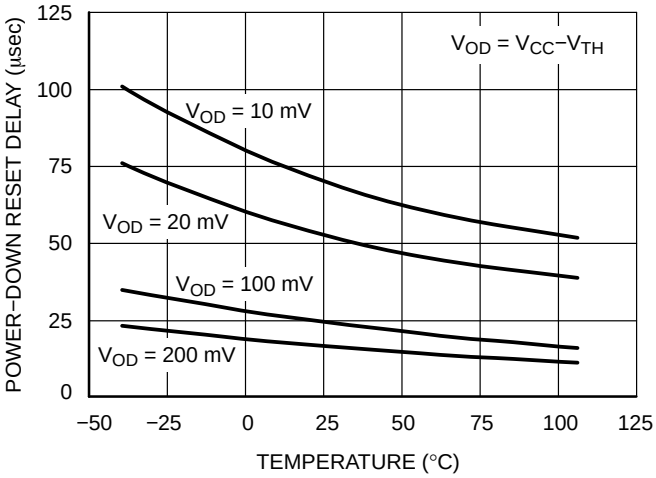


Figure 9. Power−Down Reset Delay vs. Temperature and Overdrive (V_{TH} = 1.2 V)

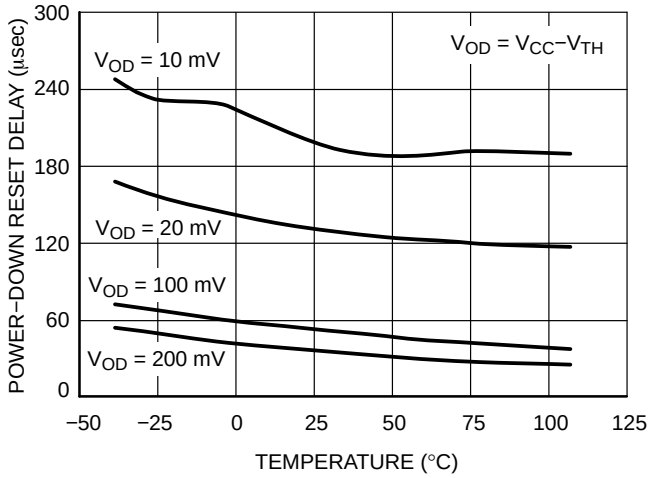


Figure 10. Power−Down Reset Delay vs. Temperature and Overdrive (V_{TH} = 4.63 V)

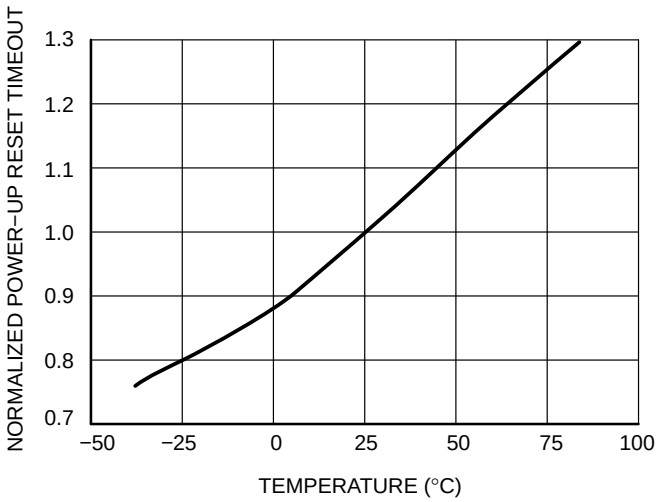


Figure 11. Normalized Power−Up Reset vs. Temperature

Detail Operation Description

The MAX803, NCP803 series microprocessor reset supervisory circuits are designed to monitor the power supplies in digital systems and provide a reset signal to the processor without any external components. Figure 2 shows the timing diagram and a typical application below. Initially consider that input voltage V_{CC} is at a nominal level greater than the voltage detector upper threshold (V_{TH}). And the $\overline{\text{RESET}}$ (RESET) output voltage (Pin 2) will be in the high state for MAX803 and NCP803 devices. If there is an input power interruption and V_{CC} becomes significantly deficient, it will fall below the lower detector threshold (V_{TH-}). This event causes the RESET output to be in the low state for the MAX803 and NCP803 devices. After completion of the power interruption, V_{CC} will rise to its nominal level and become greater than the V_{TH}. This sequence activates the internal oscillator circuitry and digital counter to count. After the count of the timeout period, the reset output will revert back to the original state.

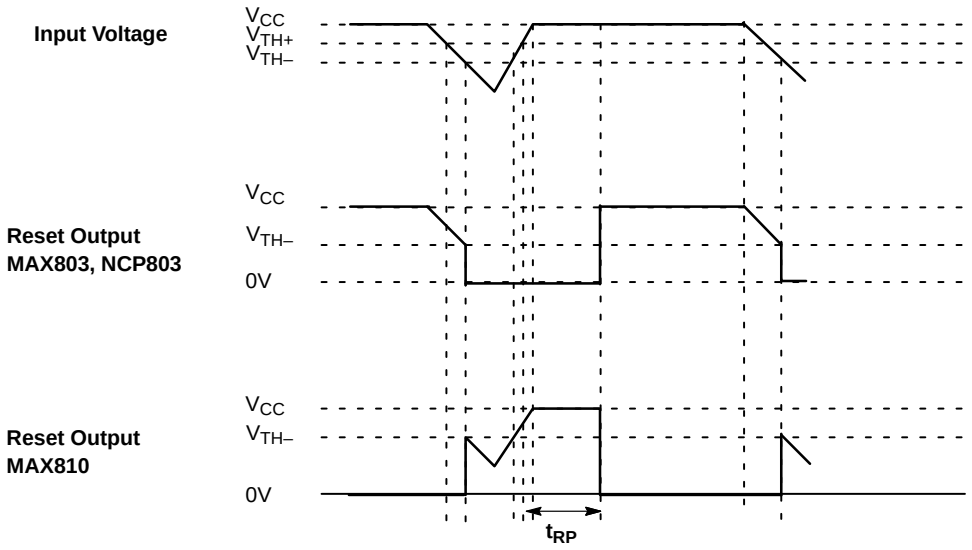
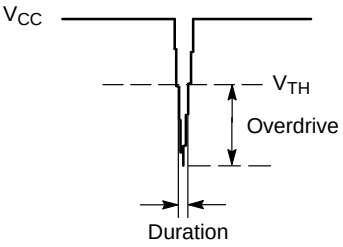


Figure 12. Timing Waveforms

APPLICATIONS INFORMATION

V_{CC} Transient Rejection

The MAX803/NCP803 series provides accurate V_{CC} monitoring and reset timing during power−up, power−down, and brownout/sag conditions, and rejects negative−going transients (glitches) on the power supply line. Figure 13 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. Any combination of duration and overdrive which lies under the curve will not generate a reset signal. Combinations above the curve are detected as a brownout or power−down. Typically, transient that goes 100 mV below the reset threshold and lasts 5.0 μs or less will not cause a reset pulse. Transient immunity can be improved by adding a capacitor in close proximity to the V_{CC} pin of the MAX803.



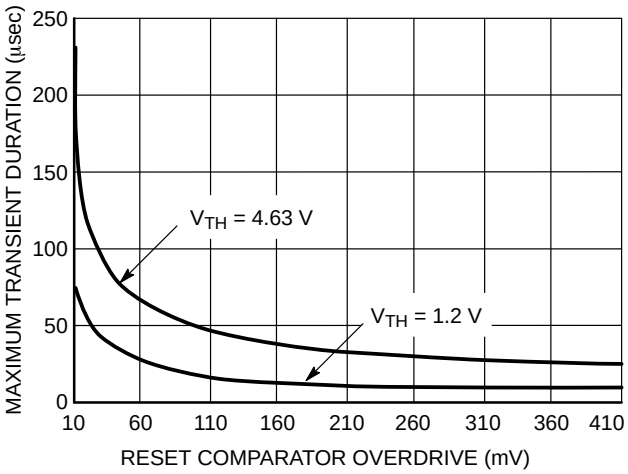


Figure 13. Maximum Transient Duration vs. Overdrive for Glitch Rejection at 25°C

$\overline{\text{RESET}}$ Signal Integrity During Power−Down

The MAX803/NCP803 $\overline{\text{RESET}}$ output is valid to V_{CC} = 1.0 V. Below this voltage the output becomes an "open circuit" and does not sink current. This means CMOS logic inputs to the Microprocessor will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in situations where $\overline{\text{RESET}}$ must be maintained valid to V_{CC} = 0 V, since the NCP803/MAX803 has Open−Drain and active−low output, it typically uses a pullup resistor. With this device, RESET will most likely not maintain an active condition, but will drift to a non−active level due to the pullup resistor and the reduced sinking capability of the open−drain device. Therefore, this device is not recommended for applications where the $\overline{\text{RESET}}$ pin is required to be valid down to V_{CC} = 0 V.

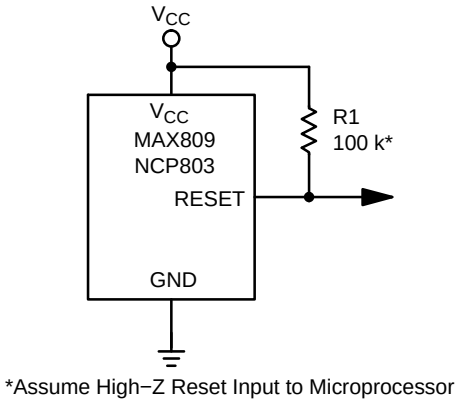


Figure 14. RESET Signal Integrity

MAX803 $\overline{\text{RESET}}$ Output Allows Use With Two Power Supplies

In numerous applications the pullup resistor place on the $\overline{\text{RESET}}$ output is connected to the supply voltage monitored by the IC. Nevertheless, a different supply voltage can also power this output and so level−shift from the monitored supply to reset the microprocessor. However, if the NCP803/MAX803's supply goes blew 1 V, the $\overline{\text{RESET}}$ output ability to sink current will decrease and the result is a high state on the pin even though the supply's IC is under the threshold level. This occurs at a V_{CC} level that depends on the R_{pullup} value and the voltage which is connected.

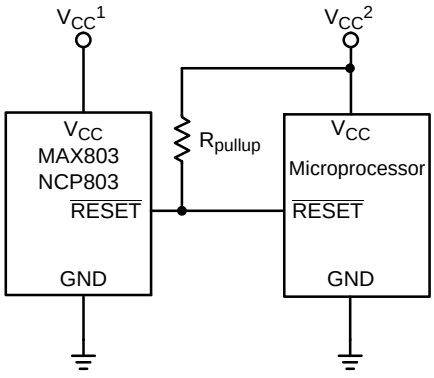


Figure 15. MAX803 $\overline{\text{RESET}}$ Output with Two Supplies

ORDERING, MARKING AND THRESHOLD INFORMATION

Part Number	Vth** (V)	Time out*** (ms)	Description	Marking	Package	Shipping†
NCP803SN160T1G	1.60	140−460	Open Drain $\overline{\text{RESET}}$	SCQ	SOT23−3 (Pb−Free)	3000 / Tape & Reel
NCP803SN232T1G	2.32	140−460		SQR	SOT23−3 (Pb−Free)	
NCP803SN263T1G	2.63	140−460		SQC	SOT23−3 (Pb−Free)	
NCP803SN293T1G	2.93	140−460		SQD	SOT23−3 (Pb−Free)	
NCP803SN308T1G	3.08	140−460		SQE	SOT23−3 (Pb−Free)	
NCP803SN400T1G	4.00	140−460		RAD	SOT23−3 (Pb−Free)	
NCP803SN438T1G	4.38	140−460		SQF	SOT23−3 (Pb−Free)	
NCP803SN463T1G	4.63	140−460		SQG	SOT23−3 (Pb−Free)	
NCP803SN120T1G	1.20	140−460		SSW	SOT23−3 (Pb−Free)	
NCP803SN293D1T1G	2.93	1−3.3		SSX	SOT23−3 (Pb−Free)	
NCP803SN293D2T1G	2.93	20−66		SSY	SOT23−3 (Pb−Free)	
NCP803SN293D3T1G	2.93	100−330		SSZ	SOT23−3 (Pb−Free)	
MAX803SQ120T1G	1.20	140−460		ZV	SC70−3 (Pb−Free)	
MAX803SQ263T1G	2.63	140−460		SX	SC70−3 (Pb−Free)	
MAX803SQ293T1G	2.93	140−460		ZW	SC70−3 (Pb−Free)	
MAX803SQ308T1G	3.08	140−460		ZX	SC70−3 (Pb−Free)	
NCV803SQ308T1G*		140−460		ZA		
MAX803SQ438T1G	4.38	140−460		ZY	SC70−3 (Pb−Free)	
MAX803SQ463T1G	4.63	140−460		ZZ	SC70−3 (Pb−Free)	
MAX803SQ293D1T1G	2.93	1−3.3		YA	SC70−3 (Pb−Free)	
MAX803SQ293D2T1G	2.93	20−66		YB	SC70−3 (Pb−Free)	
MAX803SQ308D2T1G	3.08	20−66		SY	SC70−3 (Pb−Free)	
NCV803SQ308D2T1G*		20−66		CY		
MAX803SQ293D3T1G	2.93	100−330		YC	SC70−3 (Pb−Free)	
NCP803SN293T3G	2.93	140−460		SQD	SOT23−3 (Pb−Free)	10000 / Tape & Reel

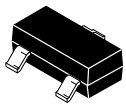
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

**Contact your ON Semiconductor sales representative for other threshold voltage options.

***Contact your ON Semiconductor sales representative for timeout options availability for other threshold voltage options.

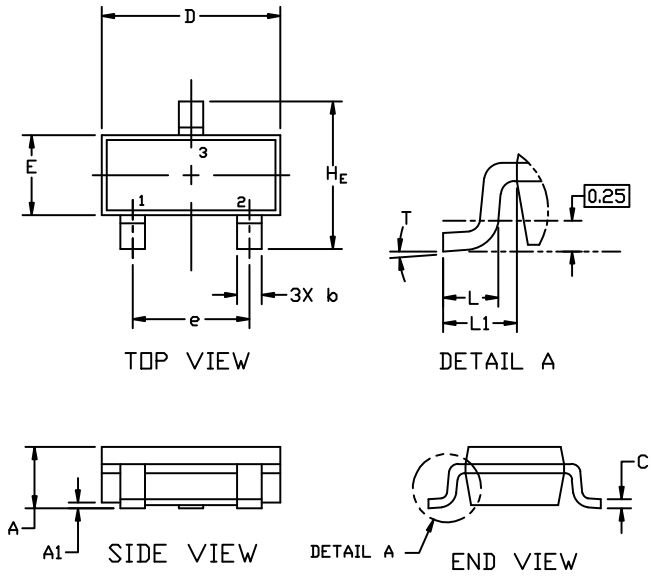
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

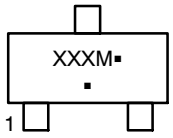


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

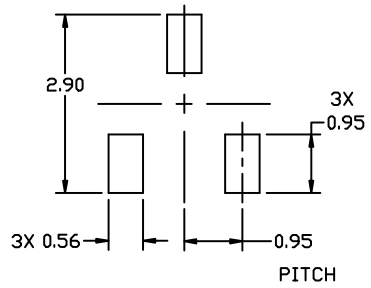
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

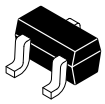
STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

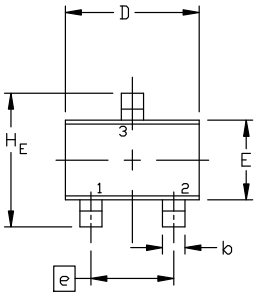
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



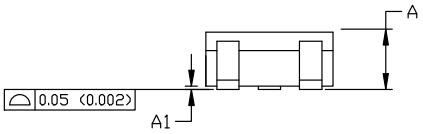
SCALE 4:1

SC−70 (SOT−323)
CASE 419
ISSUE R

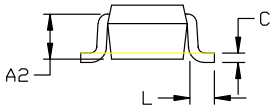
DATE 11 OCT 2022



TOP VIEW



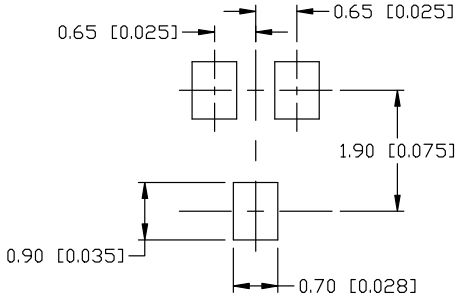
SIDE VIEW



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095



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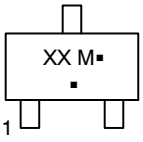
SOLDERING FOOTPRINT

GENERIC MARKING DIAGRAM



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▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

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DESCRIPTION:	**SC−70 (SOT−323)**	**PAGE 1 OF 1**

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