Low Cost 16-Bit Sampling ADC

AD1380

FEATURES

Complete sampling 16-bit ADC with reference and clock
50 kHz throughput
±1/2 LSB nonlinearity
Low noise SHA: 300 µV p-p
32-lead hermetic DIP
Parallel output
Low power: 900 µW

APPLICATIONS

Medical and analytical instrumentation
Signal processing
Data acquisition systems
Professional audio
Automatic test equipment (ATE)
Telecommunications

FUNCTIONAL BLOCK DIAGRAM

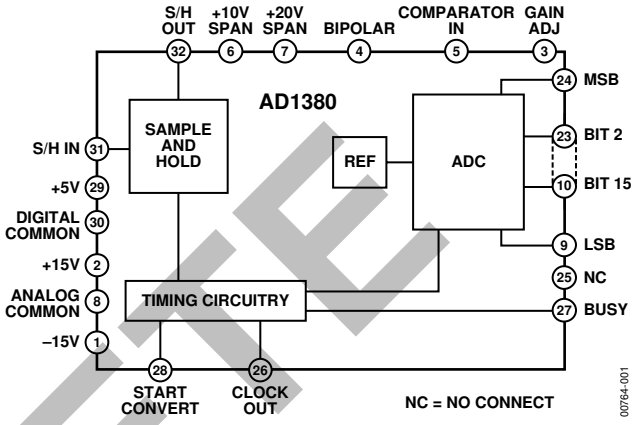

Figure 1.

GENERAL DESCRIPTION

The AD1380 is a complete, low cost 16-bit analog-to-digital converter, including internal reference, clock and sample/hold amplifier. Internal thin-film-on-silicon scaling resistors allow analog input ranges of ±2.5 V, ±5 V, ±10 V, 0 V to +5 V and 0 V to +10 V.

Important performance characteristics of the AD1380 include maximum linearity error of ±0.003% of FSR (AD1380KD) and maximum 16-bit conversion time of 14 µs. Transfer characteristics of the AD1380 (gain, offset and linearity) are specified for the combined ADC/sample-and-hold amplifier (SHA), so total performance is guaranteed as a system. The AD1380 provides data in parallel with corresponding clock and status outputs. All digital inputs and outputs are TTL or 5 V CMOS-compatible.

The serial output function is no longer available after date code 0120.

Rev. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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5/03—Rev. B to Rev. C
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SPECIFICATIONS

Typical at T_A = 25°C, V_S = 15 V, 5 V, combined sample-and-hold ADC, unless otherwise noted.

Table 1.

	AD1380JD			AD1380KD			
Model	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		16			16		Bits
ANALOG INPUTS							
Bipolar		±2.5			±2.5		V
		±5			±5		V
		±10			±10		V
Unipolar		0 to 5			0 to 5		V
		0 to 10			0 to 10		V
DIGITAL INPUTS[1]							
Convert Command	TTL-compatible, trailing edge of positive 50 ns (min) pulse						
Logic Loading		1			1		LSTTL Loads
TRANSFER CHARACTERISTICS[2] (COMBINED ADC/SHA)							
Gain Error		±0.05[3]	±0.1		±0.05[3]	±0.1	% FSR[4]
Unipolar Offset Error		±0.02[3]	±0.05		±0.02[3]	±0.05	% FSR
Bipolar Zero Error		±0.02[3]	±0.05		±0.02[3]	±0.05	% FSR
Linearity Error		±0.006			±0.003		% FSR
Differential Linearity Error		±0.003			±0.003		% FSR
Noise							
10 V Unipolar		85			85		µV rms
20 V Bipolar		115			115		µV rms
THROUGHPUT							
Conversion Time			14			14	µs
Acquisition Time (20 V Step)			6			6	µs
SAMPLE AND HOLD							
Input Resistance		4			4		kΩ
Small Signal Bandwidth		900			900		kHz
Aperture Time		50			50		ns
Aperture Jitter		100			100		ps rms
Droop Rate		50			50		µV/ms
T_{MIN} to T_{MAX}		1			1		mV/ms
Feedthrough		−80			−80		dB
DRIFT (ADC AND SHA)[5]							
Gain			±20			±20	ppm/°C
Unipolar Offset		±2	±5		±2	±5	ppm/°C
Bipolar Zero		±2	±5		±2	±5	ppm/°C
No Missing Codes (Guaranteed)		0 to +70 (13 Bits)			0 to +70 (14 Bits)		°C
DIGITAL OUTPUTS (TTL-COMPATIBLE)							
All Codes Complementary		5			5		LSTTL Loads
Clock Frequency		1.1			1.1		MHz
POWER SUPPLY REQUIREMENTS							
Analog Supplies	+14.5	+15	+15.5	+14.5	+15	+15.5	V
	−14.5	−15	−15.5	−14.5	−15	−15.5	V
Digital Supply	+4.75	+5	+5.25	+4.75	+5	+5.25	V
+15 V Supply Current		25			25		mA
−15 V Supply Current		30			30		mA
+5 V Supply Current		15			15		mA
Power Dissipation		900			900		mW

Model	AD1380JD Min	AD1380JD Typ	AD1380JD Max	AD1380KD Min	AD1380KD Typ	AD1380KD Max	Unit
TEMPERATURE RANGE							
Specified		0 to 70			0 to 70		°C
Operating		−25 to +85			−25 to +85		°C

[1] Logic 0 = 0.8 V max; Logic 1 = 2.0 V min for inputs. Logic 0 = 0.4 V max; Logic 1 = 2.4 V min for digital outputs.
[2] Tested on ±10 V and 0 V to +10 V ranges.
[3] Adjustable to zero.
[4] Full-scale range.
[5]Guaranteed but not 100% production tested.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Logic Supply Voltage	+7 V
Analog Ground to Digital Ground	±0.3 V
Analog Inputs (Pin 6, Pin 7, Pin 31)	$\pm V_S$
Digital Input	−0.3 V to V_{DD} + 0.3 V
Output Short-Circuit Duration to Ground	
Sample/Hold	Indefinite
Data	1 sec for any one output
Junction Temperature	175°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

A 16-bit ADC partitions the range of analog inputs into 2^{16} discrete ranges or quanta. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2 LSB associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors associated with ADCs are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error, and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network.

The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figure 3 and Figure 4. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point that is defined as full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of ADC accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 2).

Monotonic behavior requires that the differential linearity error be less than 1 LSB. However, a monotonic converter can have missing codes. The AD1380 is specified as having no missing codes over temperature ranges noted in the Specifications section.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or the minus full-scale point for bipolar ranges. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as

$$RSS = \sqrt{\in_G{}^2 + \in_O{}^2 + \in_L{}^2}$$

where:

$\in_G$ = *gain drift error* (*ppm*/°C).

$\in_O$ = *offset drift error* (*ppm of FSR*/°C).

$\in_L$ = *linearity error* (*ppm of FSR*/°C).

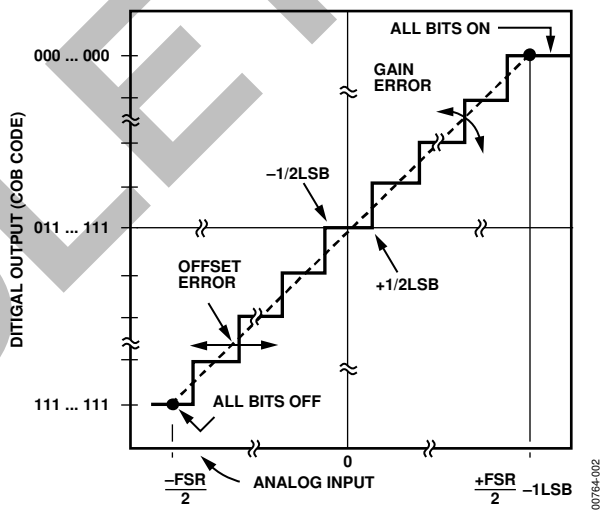


Figure 2. Transfer Characteristics for an Ideal Bipolar ADC

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD1380 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected to both the device bit output pins and the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjustment circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300 kΩ resistor to Pin 3 (GAIN ADJ) as shown in Figure 3.

If no external trim adjustment is desired, Pin 5 (COMPARATOR IN) and Pin 3 may be left open.

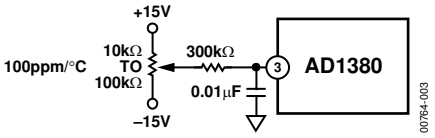


Figure 3. Gain Adjustment Circuit (±0.2% FSR)

ZERO OFFSET ADJUSTMENT

The zero offset adjustment circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8 MΩ resistor to Pin 5 for all ranges. As shown in Figure 4, the tolerance of this fixed resistor is not critical; a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200 ppm/°C temperature coefficient contributes a worst-case offset temperature coefficient of 32 $LSB_{14} \times 61$ ppm/$LSB_{14} \times 1200$ ppm/°C = 2.3 ppm/°C of FSR, if the offset adjustment potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±16 LSB_{14}, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset temperature coefficient.

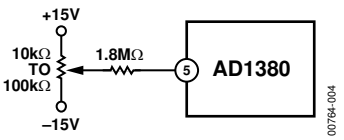


Figure 4. Zero Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjustment circuit, which contributes a negligible offset temperature coefficient if metal film resistors (temperature coefficient <100 ppm/°C) are used, is shown in Figure 5.

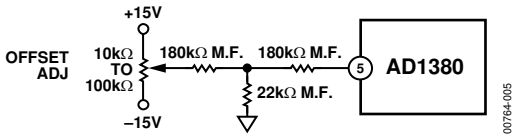


Figure 5. Low Temperature Coefficient Zero Adjustment Circuit

In either adjustment circuit, the fixed resistor connected to Pin 5 should be located close to this pin to keep the pin connection runs short. Pin 5 is quite sensitive to external noise pickup and should be guarded by ANALOG COMMON.

TIMING

The timing diagram is shown in Figure 6. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 to B_{16} are set unconditionally. At t_1, the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic 0 state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

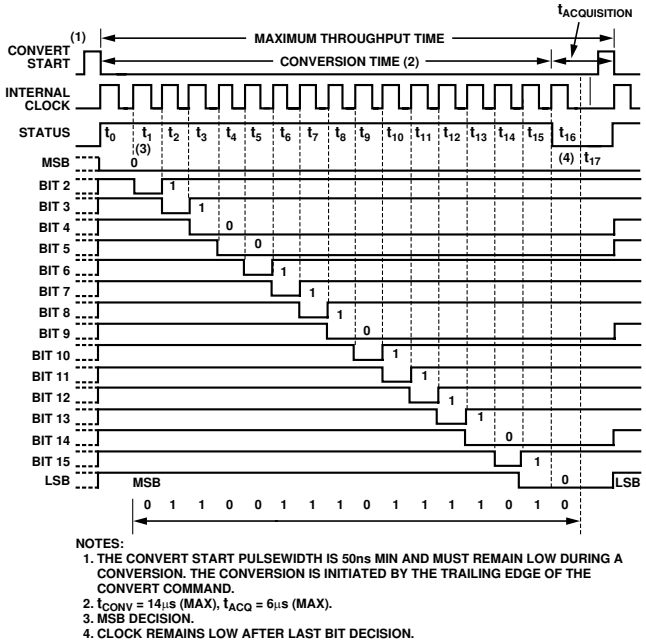


Figure 6. Timing Diagram (Binary Code 0110011101 111010)

DIGITAL OUTPUT DATA

Parallel data from TTL storage registers is in negative true form (Logic 1 = 0 V and Logic 0 = 2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20 ns before the STATUS flag returns to Logic 0, permitting parallel data transfer to be clocked on the 1 to 0 transition of the STATUS flag (see Figure 7). Parallel data output changes state on positive going clock edges.

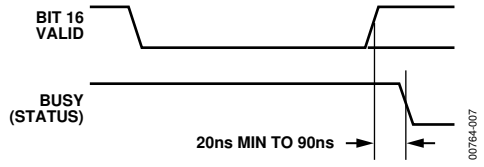


Figure 7. LSB Valid to Status Low

INPUT SCALING

The AD1380 inputs should be scaled as close to the maximum input signal range as possible to use the maximum signal resolution of the ADC. Connect the input signal as shown in Table 3. See Figure 8 for circuit details.

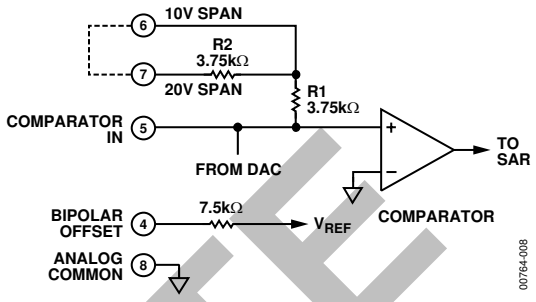


Figure 8. Input Scaling Circuit

Table 3. Input Scaling Connections

Input Signal Line	Output Code	Connect Pin 4 to	Connect Pin 7 to	Connect Input Signal to	Connect Pin 32 to
±10 V	COB	Pin 5[1]	Pin 32	Pin 31	Pin 7
±5 V	COB	Pin 5[1]	Open	Pin 31	Pin 6
±2.5 V	COB	Pin 5[1]	Pin 5[1]	Pin 31	Pin 6
0 V to +5 V	CSB	Open	Pin 5[1]	Pin 31	Pin 6
0 V to +10 V	CSB	Open	Open	Pin 31	Pin 6

[1] Pin 5 is extremely sensitive to noise and should be guarded by ANALOG COMMON.

Table 4. Transition Values vs. Calibration Codes

Output Code MSB LSB[1]	Range	±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
000. . . .000[2]	+Full Scale	+10 V −3/2 LSB	+5 V −3/2 LSB	+2.5 V −3/2 LSB	+10 V −3/2 LSB	+5 V −3/2 LSB
011 . . . 111	Midscale	0 V −1/2 LSB	0 V −1/2 LSB	0 V −1/2 LSB	+5 V −1/2 LSB	+2.5 V −1/2 LSB
111 . . . 110	−Full Scale	−10 V +1/2 LSB	−5 V +1/2 LSB	−2.5 V +1/2 LSB	0 V +1/2 LSB	0 V +1/2 LSB

[1] For LSB value for range and resolution used, see Table 5.
[2] Voltages given are the nominal value for transition to the code specified.

Table 5. Input Voltage Range and LSB Values

Analog Input Voltage Range		±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
Code Designation		COB[1] or CTC[2]	COB[1]or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV
	n = 13	2.44 mV	1.22 mV	0.61 mV	1.22 mV	0.61 mV
	n = 14	1.22 mV	0.61 mV	0.31 mV	0.61 mV	0.31 mV
	n = 15	0.61 mV	0.31 mV	0.15 mV	0.31 mV	0.15 mV

[1] COB = complementary offset binary.
[2] CTC = complementary twos complement—achieved by using an inverter to complement the most significant bit to produce $\overline{MSB}$.
[3] CSB = complementary straight binary.

CALIBRATION (14-BIT RESOLUTION EXAMPLES)

External zero adjustment and gain adjustment potentiometers, connected as shown in Figure 3 and Figure 4, are used for device calibration. To prevent interaction of these two adjustments, zero is always adjusted first and then gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and minus full scale for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 V to +10 V Range

Set analog input to +1 LSB_{14} = 0.00061 V; adjust zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2 LSB = +9.99878 V; adjust gain for 00000000000001 digital output code; full scale (gain) is now calibrated. Half-scale calibration check: set analog input to 5.00000 V; digital output code should be 01111111111111.

−10 V to +10 V Range

Set analog input to −9.99878 V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756 V; adjust gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000 V; digital output (complementary offset binary) code should be 01111111111111.

Other Ranges

Representative digital coding for 0 V to +10 V and −10 V to +10 V ranges is given in the 0 V to +10 V Range section and −10 V to +10 V Range section. Coding relationships and calibration points for 0 V to +5 V, −2.5 V to +2.5 V and −5 V to +5 V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 V to +10 V and −10 V to +10 V ranges, respectively, as indicated in Table 4.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2 LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data acquisition components have two or more ground pins that are not connected together within the device. These grounds are usually referred to as the DIGITAL COMMON (logic power return), ANALOG COMMON (analog power return), or analog signal ground. These grounds (Pin 8 and Pin 30) must be tied together at one point as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes on the circuit cards and, since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD1380. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way, AD1380 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD1380 supply terminals should be capacitively decoupled as close to the AD1380 as possible. A large value (such as 1 µF) capacitor in parallel with a 0.1 µF capacitor is usually sufficient. Analog supplies are to be bypassed to the ANALOG COMMON (analog power return) Pin 30 and the logic supply is bypassed to DIGITAL COMMON (logic power return) Pin 8.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

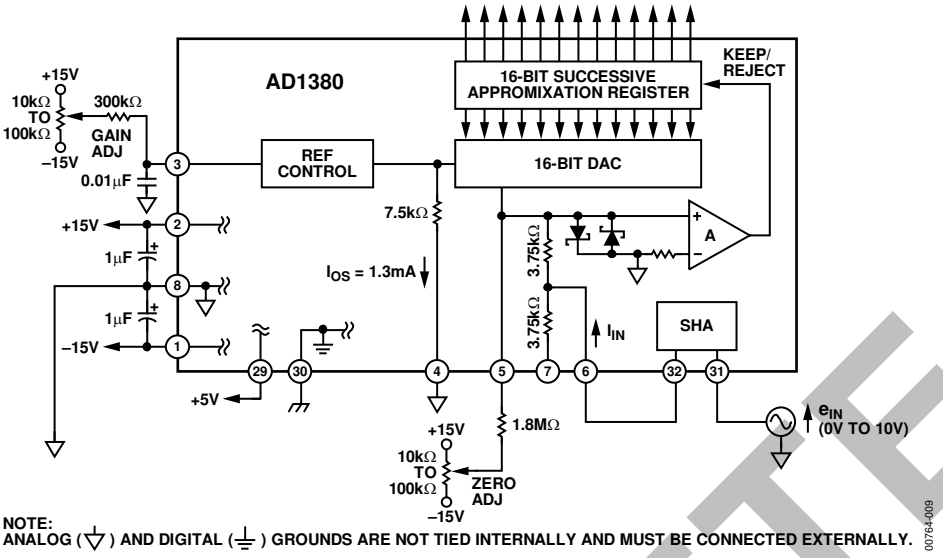


Figure 9. Analog and Power Connections for Unipolar 0 V to 10 V Input Range

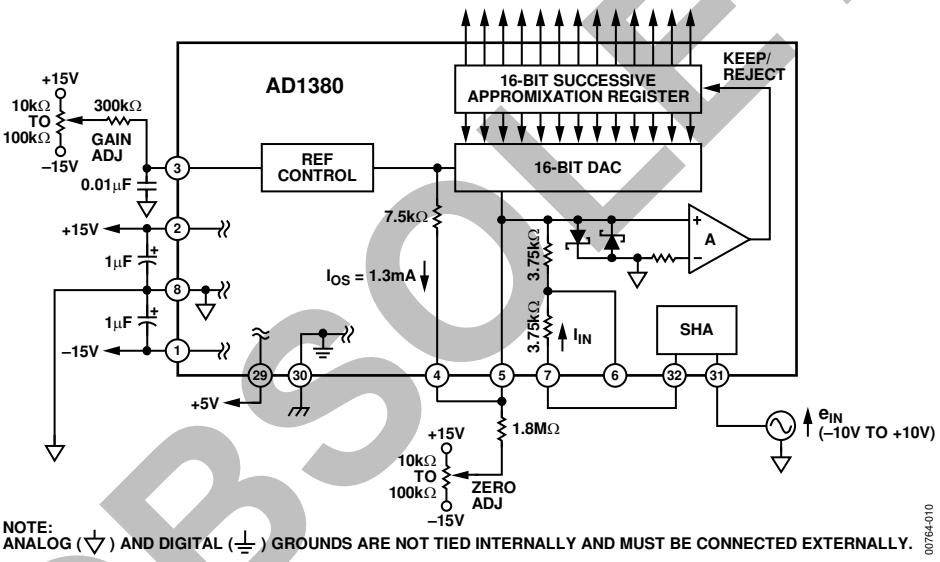


Figure 10. Analog and Power Connections for Bipolar –10 V to +10 V Input Range

APPLICATIONS

High performance sampling analog-to-digital converters like the AD1380 require dynamic characterization to ensure that they meet or exceed their desired performance parameters for signal processing applications. Key dynamic parameters include signal-to-noise ratio (SNR) and total harmonic distortion (THD), which are characterized using Fast Fourier Transform (FFT) analysis techniques.

The results of that characterization are shown in Figure 11. In the test, a 13.2 kHz sine wave is applied as the analog input (f_O) at a level of 10 dB below full scale; the AD1380 is operated at a word rate of 50 kHz (its maximum sampling frequency). The results of a 1024-point FFT demonstrate the exceptional performance of the converter, particularly in terms of low noise and harmonic distortion.

In Figure 11, the vertical scale is based on a full-scale input referenced as 0 dB. In this way, all (frequency) energy cells can be calculated with respect to full-scale rms inputs. The resulting signal-to-noise ratio is 83.2 dB, which corresponds to a noise floor of –93.2 dB. Total harmonic distortion is calculated by adding the rms energy of the first four harmonics and equals –97.5 dB.

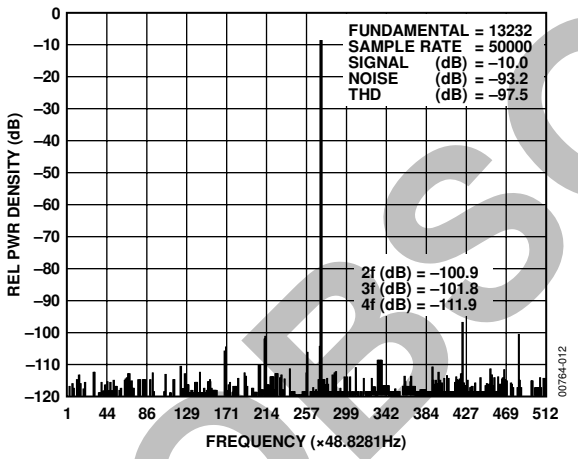


Figure 11. FFT of 13.2 kHz Input Signal at –10 dB with a 50 kHz Sample Rate

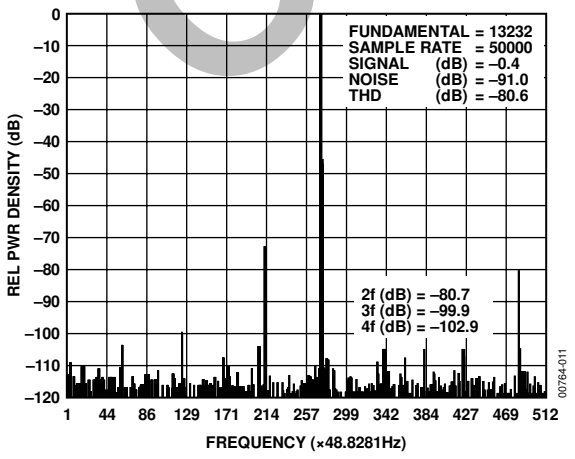


Figure 12. FFT of 13.2 kHz Input Signal at –0.4 dB with a 50 kHz Sample Rate

Increasing the input signal amplitude to –0.4 dB of full scale causes THD to increase to –80.6 dB as shown in Figure 12.

At lower input frequencies, however, THD performance is improved. Figure 13 shows a full-scale (–0.3 dB) input signal at 1.41 kHz. THD is now –96.0 dB.

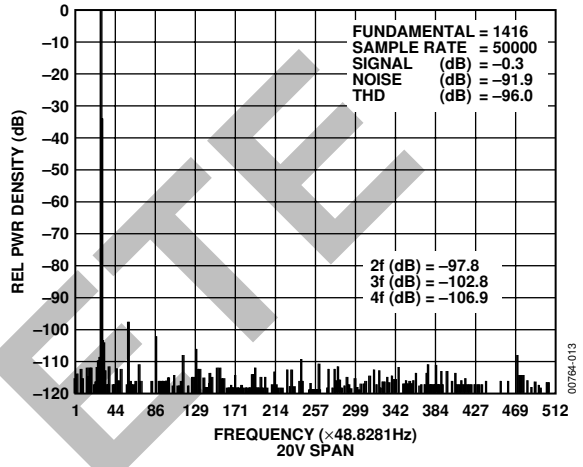


Figure 13. FFT of 1.4 kHz Input Signal at –0.3 dB with a 50 kHz Sample Rate

The ultimate noise floor can be seen with low level input signals of any frequency. In Figure 14, the noise floor is at –94 dB, as demonstrated with an input signal of 24 kHz at –39.8 dB.

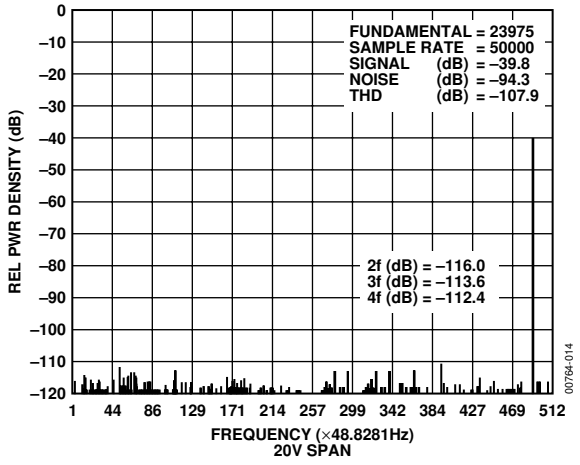
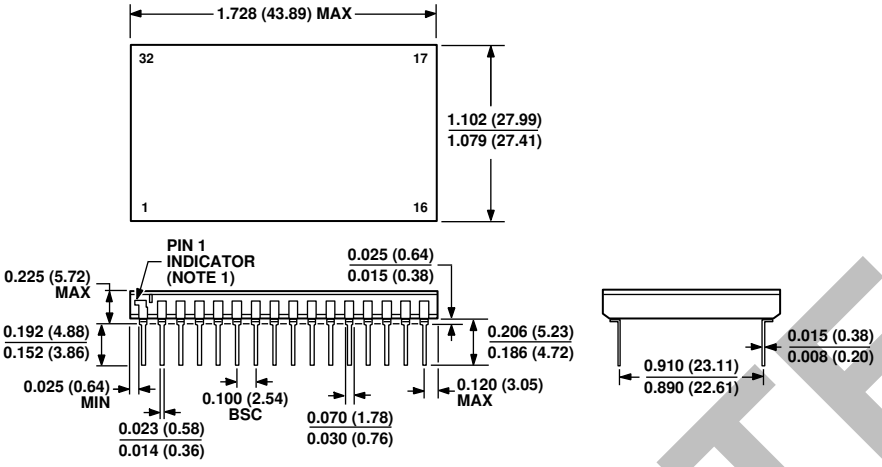


Figure 14. FFT of 24 kHz Input Signal at –39.8 dB with a 50 kHz Sample Rate

OUTLINE DIMENSIONS



NOTES:
1. INDEX AREA IS INDICATED BY A NOTCH OR LEAD ONE IDENTIFICATION MARK LOCATED ADJACENT TO LEAD ONE.
2. CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 15. 32-Lead Bottom-Brazed Ceramic DIP for Hybrid [BBDIP_H] (DH-32E)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option
AD1380JD	0.006% FSR	0°C to 70°C	Ceramic (DH-32E)
AD1380KD	0.003% FSR	0°C to 70°C	Ceramic (DH-32E)

C00764–0–6/05(D)