PCA9519

4-channel level translating I²C-bus/SMBus repeater

Rev. 3 — 10 January 2013 Product data sheet

1. General description

The PCA9519 is a 4-channel level translating I²C-bus/SMBus repeater that enables the processor low voltage 2-wire serial bus to interface with standard I²C-bus or SMBus I/O. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling the I²C-bus or SMBus maximum capacitance of 400 pF on the higher voltage side. The SDA and SCL pins are over-voltage tolerant and are high-impedance when the PCA9519 is unpowered.

The port B drivers are compliant with SMBus I/O levels, while port A uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. The port A uses a 1 mA current source for pull-up and a 200 Ω pull-down driver. This results in a LOW on port A accommodating smaller voltage swings. The output pull-down on the port A internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port B drives a hard LOW and the input level is set at 0.3 of SMBus or I²C-bus voltage level which enables port B to connect to any other I²C-bus device or buffer.

The PCA9519 drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

2. Features and benefits

- 4-channel (4 SCL/SDA pairs), bidirectional buffer isolates capacitance and allows 400 pF on port B of the device
- Voltage level translation from port A (1 V to $V_{CC(B)}$ − 1.5 V) to port B (3.0 V to 5.5 V)
- Requires no external pull-up resistors on lower voltage port A
- Active HIGH repeater enable input
- Open-drain inputs/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins
- Operating supply voltage range of 1.0 V to $V_{CC(B)}$ − 1.5 V on port A, 3.0 V to 5.5 V on port B
- 5 V tolerant B-side SCL and SDA and enable pins
- 50 ns glitch filter on B-side input

- 0 Hz to 400 kHz clock frequency

  Remark: The maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP20, HVQFN24

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9519PW	PA9519	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
PCA9519BS	9519	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9519PW	PCA9519PW,118	TSSOP20	Reel pack, SMD, 13-inch	2500	T_{amb} = −40 °C to +85 °C
PCA9519BS	PCA9519BS,118	HVQFN24	Reel pack, SMD, 13-inch	6000	T_{amb} = −40 °C to +85 °C

4. Functional diagram

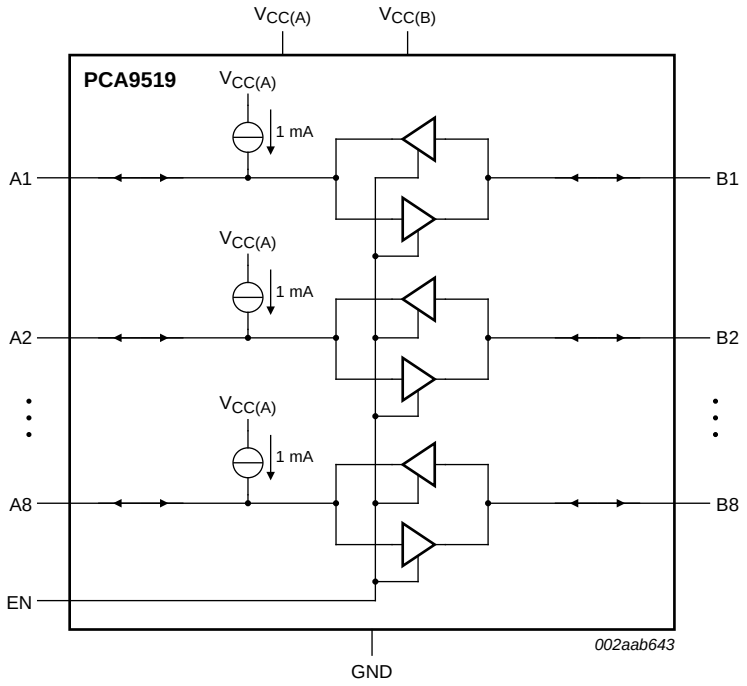


Fig 1. Functional diagram of PCA9519

5. Pinning information

5.1 Pinning

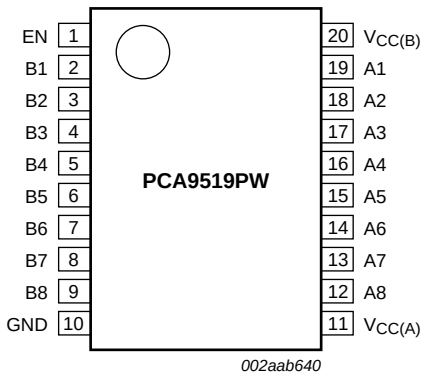


Fig 2. Pin configuration for TSSOP20

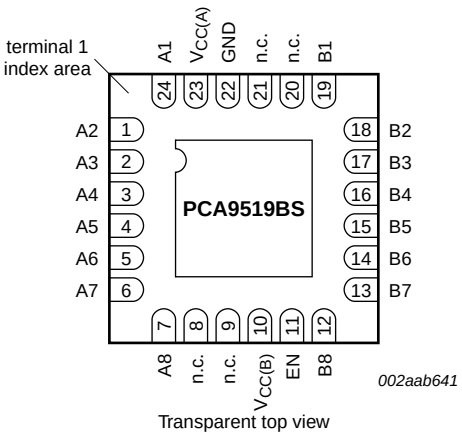


Fig 3. Pin configuration for HVQFN24

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP20	HVQFN24	
EN	1	11	enable input (active HIGH)
GND	10	22[1]	ground (0 V)
$V_{CC(A)}$	11	23	port A power supply
A1	19	24	A1 port (low voltage side)[2]
A2	18	1	A2 port (low voltage side)[2]
A3	17	2	A3 port (low voltage side)[2]
A4	16	3	A4 port (low voltage side)[2]
A5	15	4	A5 port (low voltage side)[2]
A6	14	5	A6 port (low voltage side)[2]
A7	13	6	A7 port (low voltage side)[2]
A8	12	7	A8 port (low voltage side)[2]
$V_{CC(B)}$	20	10	port B power supply
B8	9	12	B8 port (SMBus/I²C-bus side)[2]
B7	8	13	B7 port (SMBus/I²C-bus side)[2]
B6	7	14	B6 port (SMBus/I²C-bus side)[2]
B5	6	15	B5 port (SMBus/I²C-bus side)[2]
B4	5	16	B4 port (SMBus/I²C-bus side)[2]
B3	4	17	B3 port (SMBus/I²C-bus side)[2]
B2	3	18	B2 port (SMBus/I²C-bus side)[2]
B1	2	19	B1 port (SMBus/I²C-bus side)[2]
n.c.	-	8, 9, 20, 21	

[1] HVQFN24 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

[2] Port A and port B can be used for either SCL or SDA.

6. Functional description

Refer to Figure 1 “Functional diagram of PCA9519”.

The PCA9519 enables I²C-bus or SMBus translation down to $V_{CC(A)}$ as low as 1.0 V without degradation of system performance. The PCA9519 contains 8 bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage and 3.3 V SMBus or 5 V I²C-bus. Port B I/Os are over-voltage tolerant to 5.5 V even when the device is unpowered.

The PCA9519 includes a power-up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.5 V and the $V_{CC(A)}$ is above 0.8 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power-up. After power-up and with the EN pin HIGH, a LOW level on the port A (below approximately 0.15 V) turns the corresponding port B driver (either SDA or SCL) on and drives the port B down to about 0 V. When port A rises above approximately 0.15 V, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When the port B falls first and goes below $0.3V_{CC(B)}$, the port A driver is turned on and the port A pulls down to 0.2 V (typical). The port B pull-down is not enabled unless the port A voltage goes below V_{ILc}. If the port A low voltage goes below V_{ILc}, the port B pull-down driver is enabled until the port A rises above approximately 0.15 V (V_{ILc}), then the port B, if not externally driven LOW, will continue to rise being pulled up by the external pull-up resistor.

Remark: Ground offset between the PCA9519 ground and the ground of devices on port A of the PCA9519 must be avoided.

The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133 Ω or less (R = E / I). Such a driver will share enough current with the port A output pull-down of the PCA9519 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{ILc} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV.

Bus repeaters that use an output offset are not interoperable with port A of the PCA9519 as their output LOW levels will not be recognized by the PCA9519 as a LOW. If the PCA9519 is placed in an application where the V_{IL} of the port A of the PCA9519 does not go below its V_{ILc} it will pull the port B LOW initially when the port A input transitions LOW but port B will return HIGH, so it will not reproduce the port A input on port B. Such applications should be avoided.

Port B is interoperable with all I²C-bus slaves, masters, and repeaters and includes the 50 ns glitch filter.

6.1 Enable

The EN pin is active HIGH and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled.

The enable pin should only change state when the bus and the repeater port are in an idle state to prevent system failures.

6.2 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system. Each of the port A I/Os has an internal pull-up current source and does not require the external pull-up resistor. The port B is designed to work with Standard mode and Fast mode I²C-bus devices in addition to SMBus devices. Standard mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

7. Application design-in information

A typical application is shown in Figure 4. In this example, the CPU is running on a 1.1 V I²C-bus while the master is connected to a 3.3 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

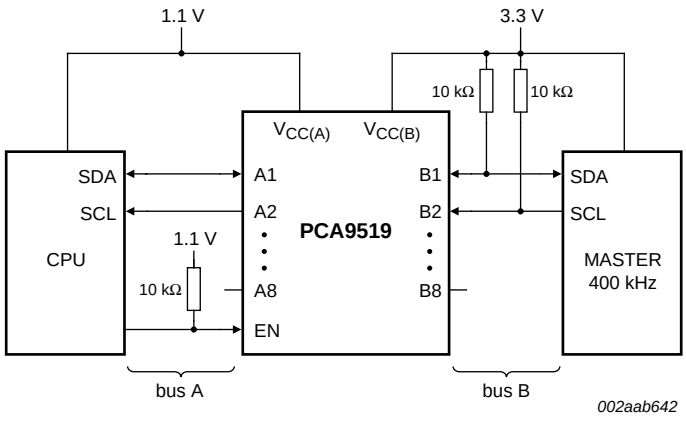


Fig 4. Typical application

When port B of the PCA9519 is pulled LOW by a driver on the I²C-bus, a CMOS hysteresis detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about 0.2 V. When port A of the PCA9519 falls, first a comparator detects the falling edge and causes the internal driver on port B to turn on and pull the port B pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 5 and Figure 6. If the bus master in Figure 4 were to write to the slave through the PCA9519, waveforms shown in Figure 5 would be observed on the B bus. This looks like a normal I²C-bus transmission.

On the port A bus of the PCA9519, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9519. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the master device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9519 for a short delay while the port B bus rises above $0.5V_{CC(B)}$, then it continues

HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the port A bus at the input of the PCA9519 (V_{IL}) is below V_{ILc} to be recognized by the PCA9519 and then transmitted to the port B bus.

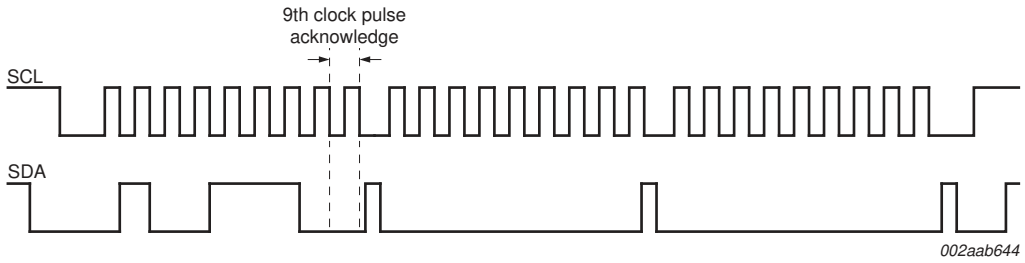


Fig 5. Bus B SMBus/I²C-bus waveform

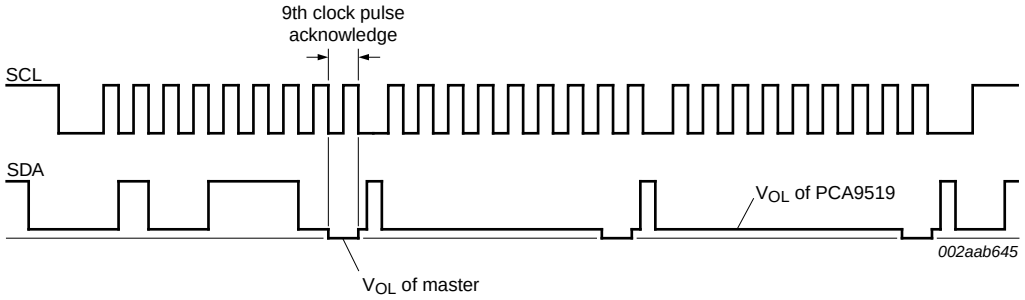


Fig 6. Bus A lower voltage waveform

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(B)}$	supply voltage port B		−0.5	+6	V
$V_{CC(A)}$	supply voltage port A		−0.5	+6	V
$V_{I/O}$	voltage on an input/output pin	port A	−0.5	+6	V
		port B; enable pin (EN)	−0.5	+6	V
$I_{I/O}$	input/output current		-	±20	mA
I_I	input current		-	±20	mA
P_{tot}	total power dissipation		-	100	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating in free air	−40	+85	°C
T_j	junction temperature		-	125	°C
T_{sp}	solder point temperature	10 s max.	-	300	°C

9. Static characteristics

Table 5. Static characteristics

GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supplies							
$V_{CC(B)}$	supply voltage port B			3.0	-	5.5	V
$V_{CC(A)}$	supply voltage port A			1.0	-	$V_{CC(B)}$ − 1.5	V
$I_{CC(A)}$	supply current port A	all port A static HIGH		1	2.1	3.6	mA
		all port A static LOW		5	11.6	20	mA
$I_{CC(B)}$	supply current port B	all port B static HIGH		2	3.3	4.5	mA
Input and output of port A (A1 to A8)							
V_{IH}	HIGH-level input voltage	port A		$0.7V_{CC(A)}$	-	$V_{CC(A)}$	V
V_{IL}	LOW-level input voltage	port A	[2]	−0.5	-	+0.3	V
V_{ILc}	contention LOW-level input voltage		[2]	−0.5	+0.15	-	V
V_{IK}	input clamping voltage	I_L = −18 mA		−1.5	-	−0.5	V
I_{LI}	input leakage current	$V_I = V_{CC(A)}$		-	-	±1	µA
I_{IL}	LOW-level input current		[3]	−1.5	−1	−0.45	mA
V_{OL}	LOW-level output voltage		[4]	-	0.2	0.35	V
V_{OL}−V_{ILc}	difference between LOW-level output and LOW-level input voltage contention	port A	[5]	-	50	-	mV
I_{LOH}	HIGH-level output leakage current	V_O = 1.1 V		-	-	10	µA
C_{io}	input/output capacitance			-	6	7	pF
Input and output of port B (B1 to B8)							
V_{IH}	HIGH-level input voltage			$0.7V_{CC(B)}$	-	$V_{CC(B)}$	V
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{CC(B)}$	V
V_{IK}	input clamping voltage	I_L = −18 mA		−1.5	-	−0.5	V
I_{LI}	input leakage current	V_I = 3.6 V		−1.0	-	+1.0	µA
I_{IL}	LOW-level input current	V_I = 0.2 V		-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	0.1	0.2	V
I_{LOH}	HIGH-level output leakage current	V_O = 3.6 V		-	-	10	µA
C_{io}	input/output capacitance			-	6	7	pF
Enable							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.1V_{CC(A)}$	V
V_{IH}	HIGH-level input voltage			$0.9V_{CC(A)}$	-	$V_{CC(B)}$	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V, EN; V_{CC} = 3.6 V		−1	-	+1	µA
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance	V_I = 3.0 V or 0 V		-	2	3	pF

[1] Typical values with $V_{CC(A)}$ = 1.1 V, $V_{CC(B)}$ = 5.0 V.

[2] V_{IL} specification is for the falling edge seen by the port A input. V_{ILc} is for the static LOW levels seen by the port A input resulting in port B output staying LOW.

[3] The port A current source has a typical value of about 1 mA, but varies with both $V_{CC(A)}$ and $V_{CC(B)}$. Below $V_{CC(A)}$ of about 0.7 V the port A current source current drops to 0 mA. The current source current dropping across the internal pull-down driver resistance of about 200 Ω defines the V_{OL}.

[4] As long as the chip ground is common with the input ground reference the driver resistance may be as large as 120 Ω. However, ground offset will rapidly decrease the maximum allowed driver resistance.

[5] Guaranteed by design.

10. Dynamic characteristics

Table 6. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V							
t_{PLH}	LOW to HIGH propagation delay	port B to port A	[1]	69	109	216	ns
t_{PHL}	HIGH to LOW propagation delay	port B to port A	[1]	63	86	140	ns
t_{TLH}	LOW to HIGH output transition time	port A	[1]	14	22	96	ns
t_{THL}	HIGH to LOW output transition time	port A	[1]	5	8.1	16	ns
t_{PLH}	LOW to HIGH propagation delay	port A to port B	[1]	−69	−91	−139	ns
t_{PLH2}	LOW to HIGH propagation delay 2	port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	[1]	91	153	226	ns
t_{PHL}	HIGH to LOW propagation delay	port A to port B	[1]	73	122	183	ns
t_{TLH}	LOW to HIGH output transition time	port B	[1][2]	-	61	-	ns
t_{THL}	HIGH to LOW output transition time	port B	[1]	15	24	40	ns
t_{su}	set-up time	EN HIGH before START condition		100	-	-	ns
t_h	hold time	EN HIGH after STOP condition		100	-	-	ns
$V_{CC(A)}$ = 1.9 V; $V_{CC(B)}$ = 5.0 V							
t_{PLH}	LOW to HIGH propagation delay	port B to port A	[1]	69	105	216	ns
t_{PHL}	HIGH to LOW propagation delay	port B to port A	[1]	63	86	140	ns
t_{TLH}	LOW to HIGH output transition time	port A	[1]	14	27	96	ns
t_{THL}	HIGH to LOW output transition time	port A	[1]	5	8	35	ns
t_{PLH}	LOW to HIGH propagation delay	port A to port B	[1]	−69	−89	−139	ns
t_{PLH2}	LOW to HIGH propagation delay 2	port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	[1]	91	131	226	ns
t_{PHL}	HIGH to LOW propagation delay	port A to port B	[1]	73	99	183	ns
t_{TLH}	LOW to HIGH output transition time	port B	[1][2]	-	65	-	ns
t_{THL}	HIGH to LOW output transition time	port B	[1]	15	31	40	ns
t_{su}	set-up time	EN HIGH before START condition		100	-	-	ns
t_h	hold time	EN HIGH after STOP condition		100	-	-	ns

[1] Load capacitance = 50 pF; load resistance on port B = 1.35 kΩ.

[2] Value is determined by RC time constant of bus line.

10.1 AC waveforms

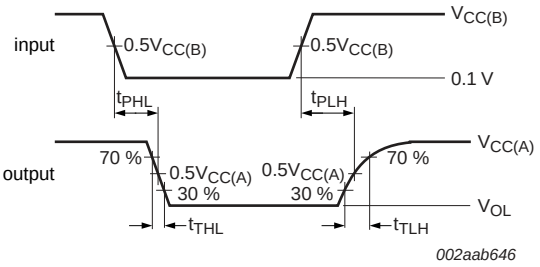


Fig 7. Propagation delay and transition times; port B to port A

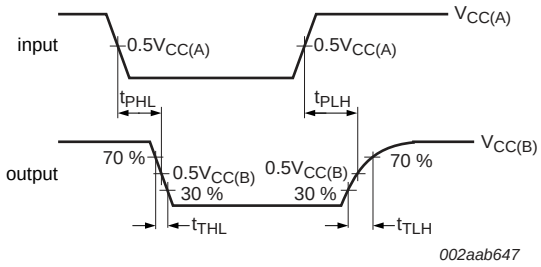


Fig 8. Propagation delay and transition times; port A to port B

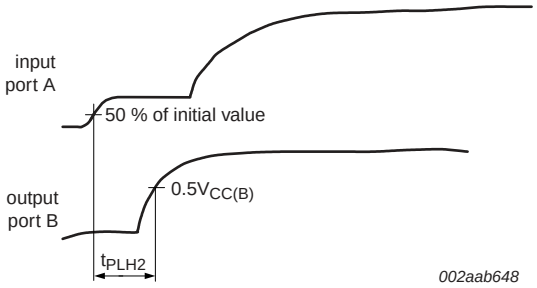
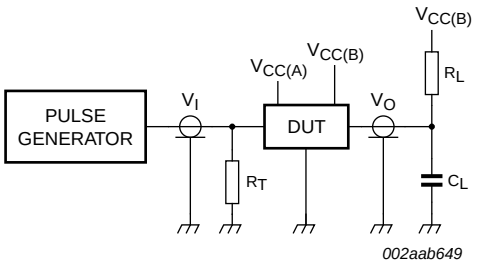


Fig 9. Propagation delay from port A's external driver switching off to the port B LOW-to-HIGH transition; port A to port B

11. Test information



R_L = load resistor; 1.35 kΩ on port B

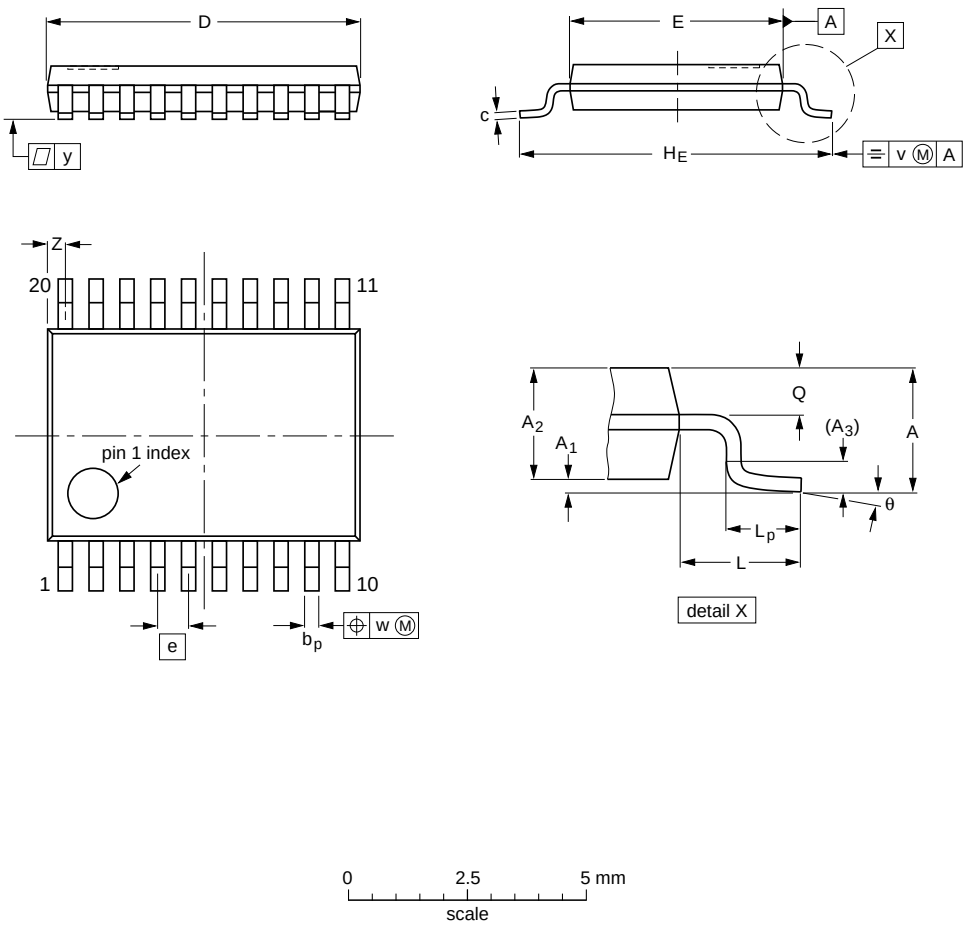
C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Fig 10. Test circuit for open-drain outputs

12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

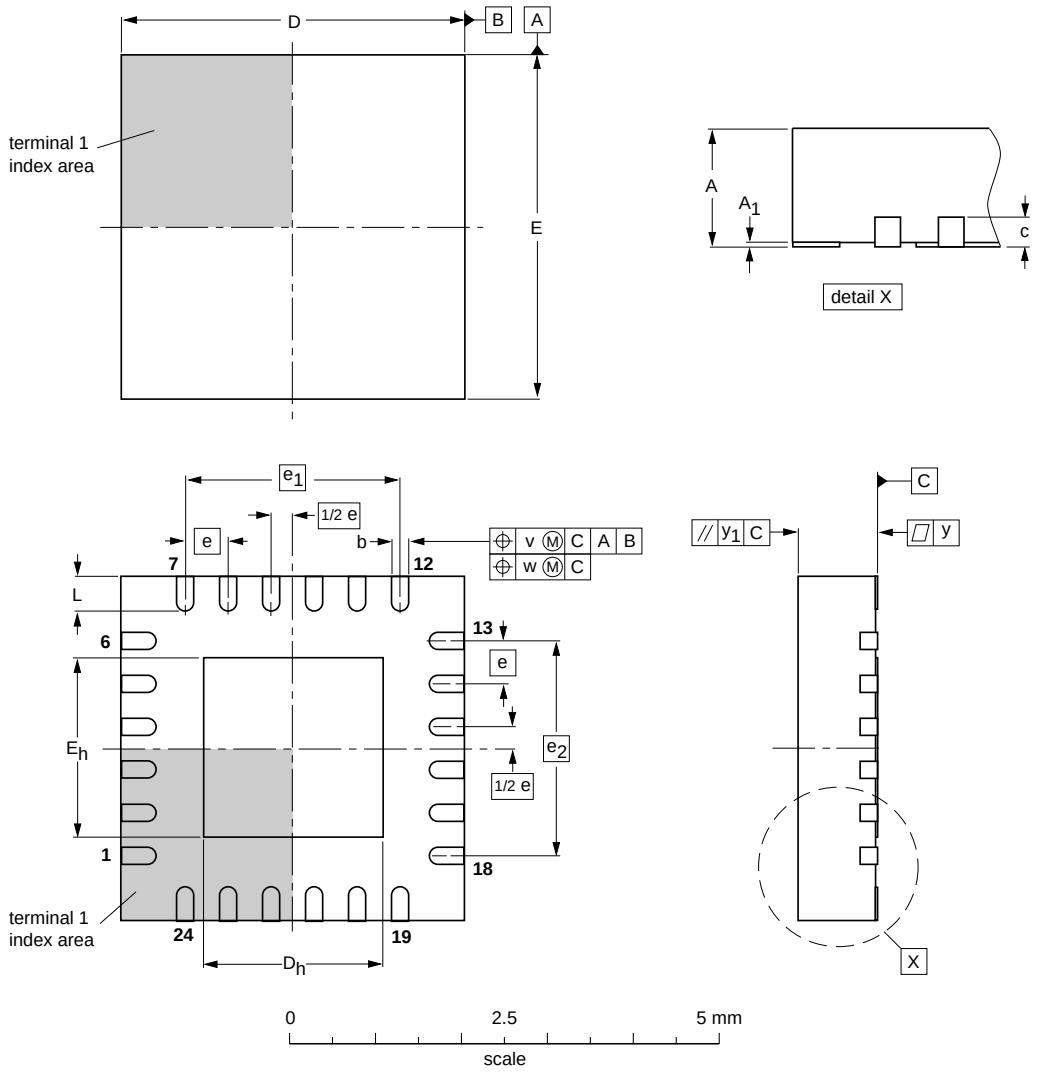
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT360-1 (TSSOP20)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 12. Package outline SOT616-1 (HVQFN24)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020C)

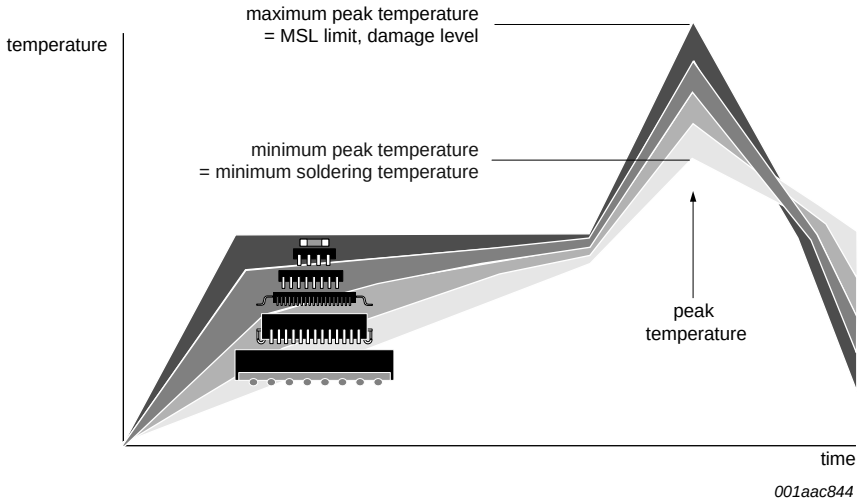
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



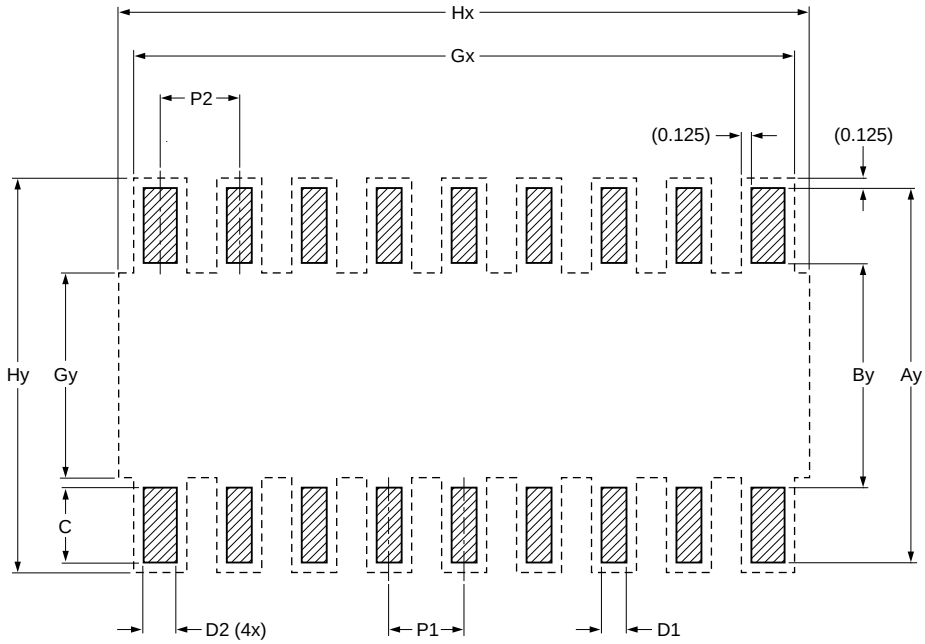
MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

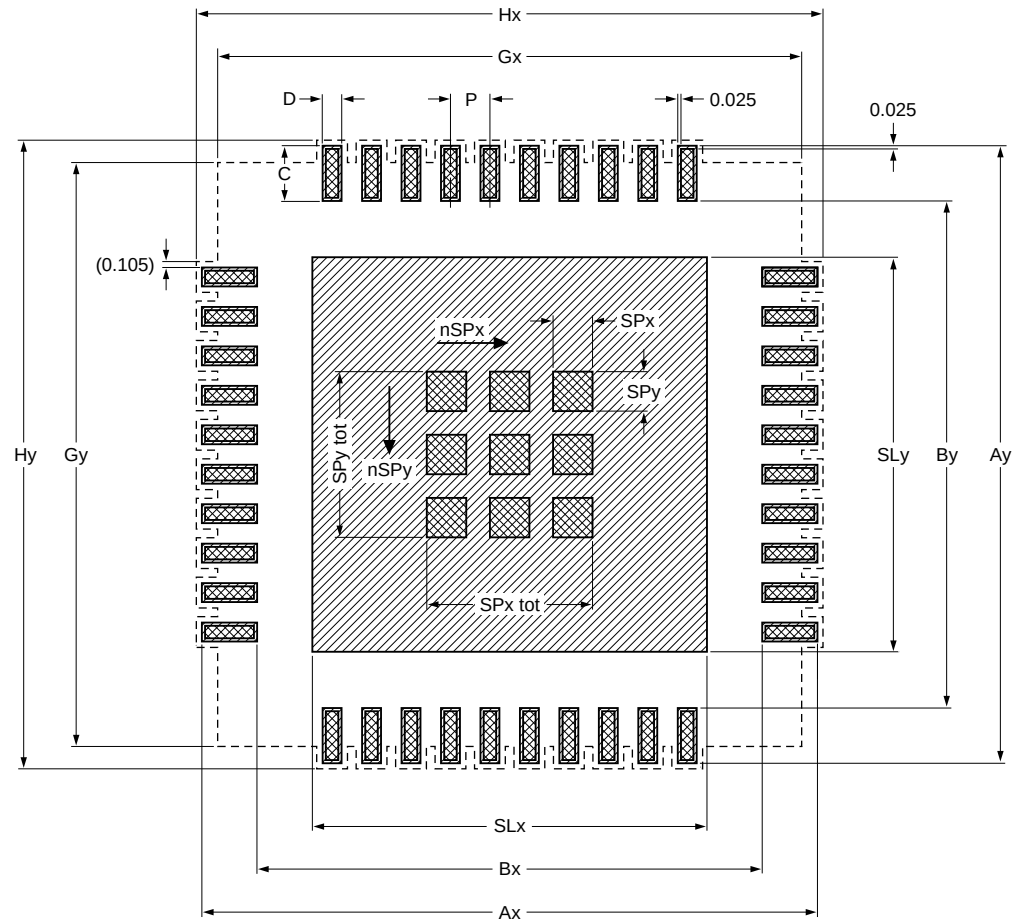
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Fig 14. PCB footprint for SOT360-1 (TSSOP20); reflow soldering

Footprint information for reflow soldering of HVQFN24 package **SOT616-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	5.000	5.000	3.200	3.200	0.900	0.240	2.100	2.100	1.200	1.200	0.450	0.450	4.300	4.300	5.250	5.250

Issue date ~~07-05-07~~ 09-06-15 *sot616-1_fr*

Fig 15. PCB footprint for SOT616-1 (HVQFN24); reflow soldering

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit Bus
NMOS	Negative-channel Metal-Oxide Semiconductor
PCB	Printed-Circuit Board
RC	Resistor Capacitor network
SMBus	System Management Bus

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9519 v.3	20130110	Product data sheet	-	PCA9519 v.2
Modifications:	• Section 2 “Features and benefits”, 14th bullet item: deleted phrase “200 V MM per JESD22-A115” • Table 1 “Ordering information”: Type number PCA9519PW’s topside mark is corrected from “PCA9519” to “PA9519” to reflect manufacturing. • Added Section 3.1 “Ordering options” • Added Section 14 “Soldering: PCB footprints”			
PCA9519 v.2	20070813	Product data sheet	-	PCA9519 v.1
PCA9519 v.1	20060622	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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