BCW70LT1

General Purpose Transistors

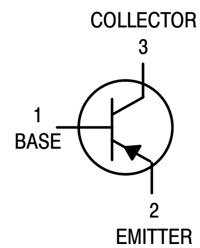
PNP Silicon

ON Semiconductor®

http://onsemi.com

Features

- Pb−Free Package is Available



MAXIMUM RATINGS

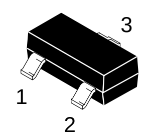
Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	−45	Vdc
Emitter−Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) @T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

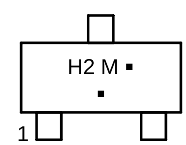
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina



SOT−23 (TO−236AB)
CASE 318
STYLE 6

MARKING DIAGRAM



H2 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
BCW70LT1	SOT−23	3000 / Tape & Reel
BCW70LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = −2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−45	−	Vdc
Collector−Emitter Breakdown Voltage (I_C = −100 μAdc, V_{EB} = 0)	$V_{(BR)CES}$	−50	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −10 μAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−	Vdc
Collector Cutoff Current (V_{CB} = −20 Vdc, I_E = 0) (V_{CB} = −20 Vdc, I_E = 0, T_A = 100°C)	I_{CBO}	 − −	 −100 −10	 nAdc μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = −2.0 mAdc, V_{CE} = −5.0 Vdc)	h_{FE}	215	500	−
Collector−Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −0.5 mAdc)	$V_{CE(sat)}$	−	−0.3	Vdc
Base−Emitter On Voltage (I_C = −2.0 mAdc, V_{CE} = −5.0 Vdc)	$V_{BE(on)}$	−0.6	−0.75	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Output Capacitance (I_E = 0, V_{CB} = −10 Vdc, f = 1.0 MHz)	C_{obo}	−	7.0	pF
Noise Figure (I_C = −0.2 mAdc, V_{CE} = −5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)	N_F	−	10	dB

TYPICAL NOISE CHARACTERISTICS

(V_{CE} = −5.0 Vdc, T_A = 25°C)

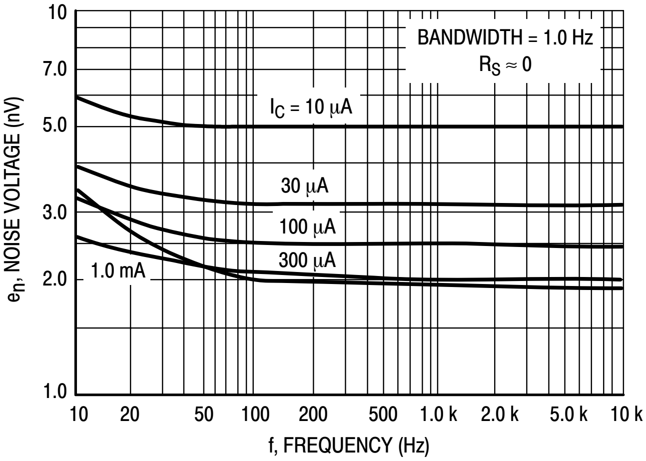


Figure 1. Noise Voltage

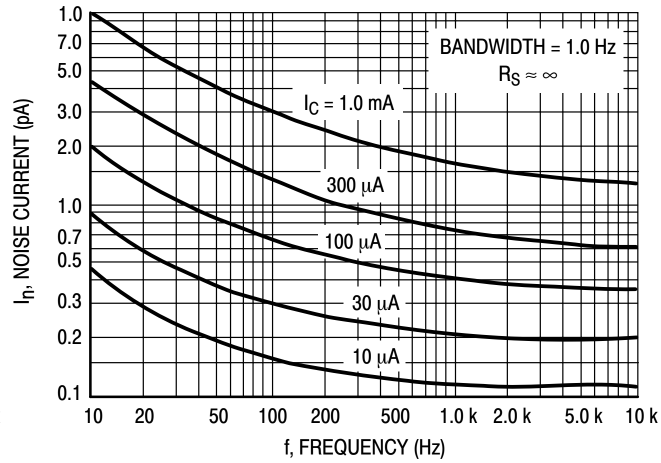


Figure 2. Noise Current

NOISE FIGURE CONTOURS

(V_{CE} = −5.0 Vdc, T_A = 25°C)

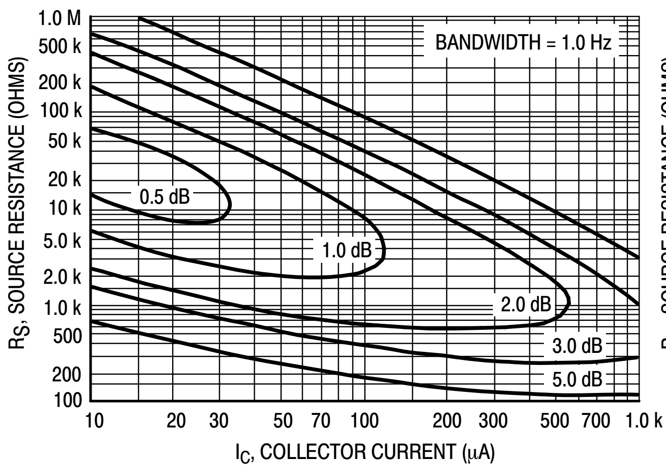


Figure 3. Narrow Band, 100 Hz

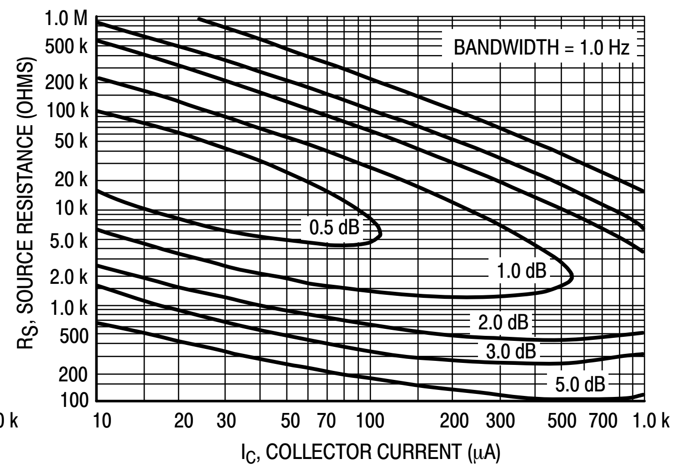


Figure 4. Narrow Band, 1.0 kHz

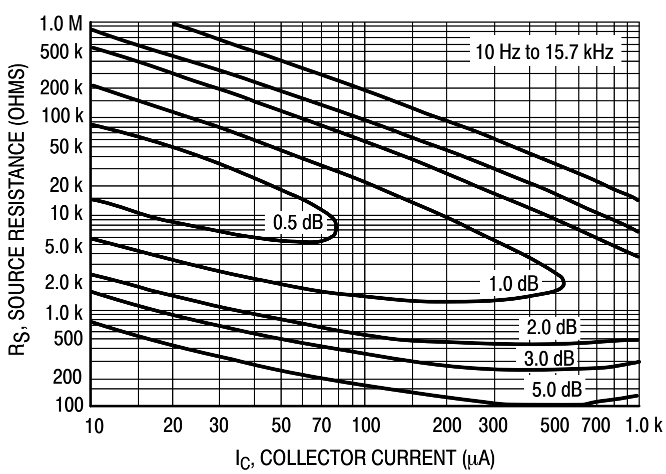


Figure 5. Wideband

Noise Figure is Defined as:

$$NF = 20 \log_{10}\left[\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S}\right]^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)
I_n = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant (1.38 x 10^{-23} j/°K)
T = Temperature of the Source Resistance (°K)
R_S = Source Resistance (Ohms)

TYPICAL STATIC CHARACTERISTICS

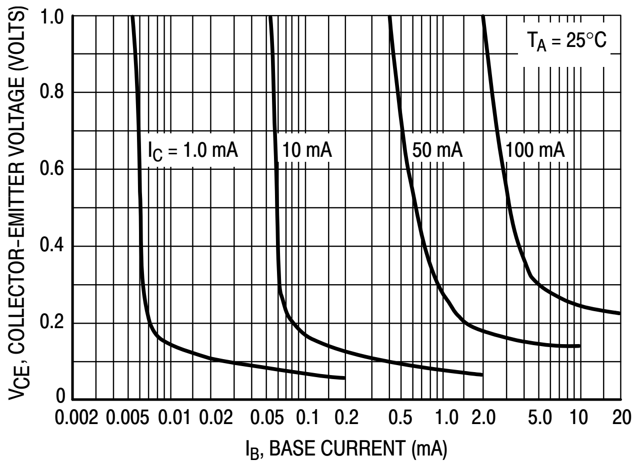


Figure 6. Collector Saturation Region

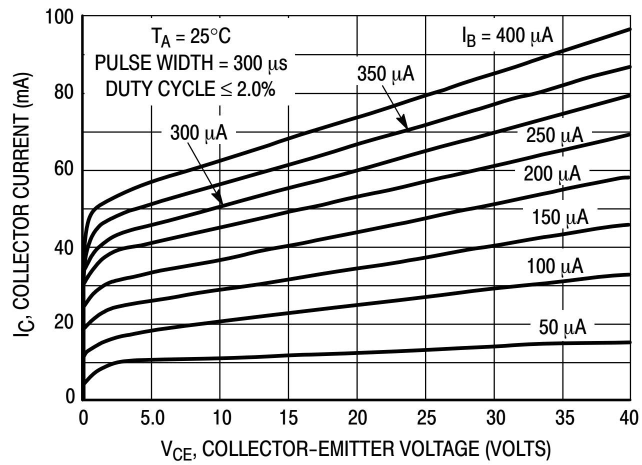


Figure 7. Collector Characteristics

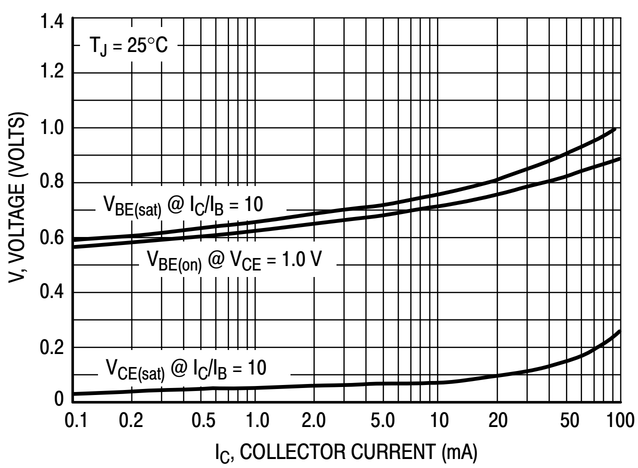


Figure 8. "On" Voltages

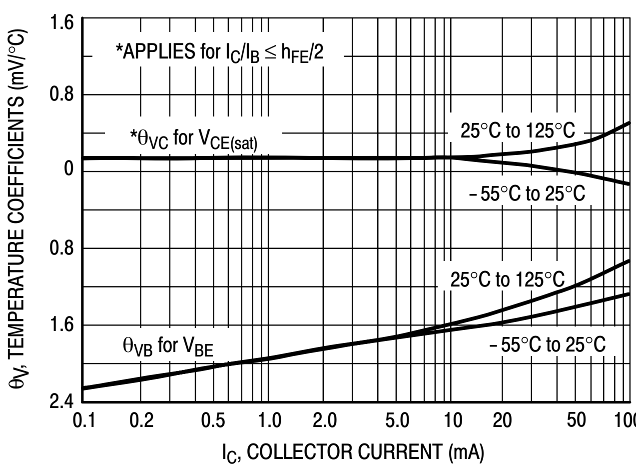


Figure 9. Temperature Coefficients

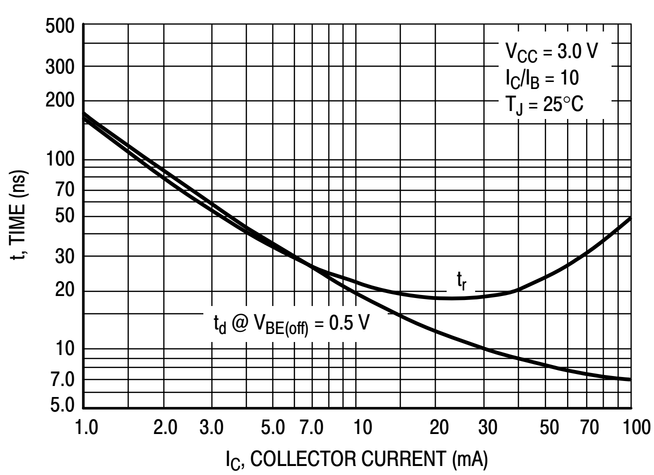


Figure 10. Turn−On Time

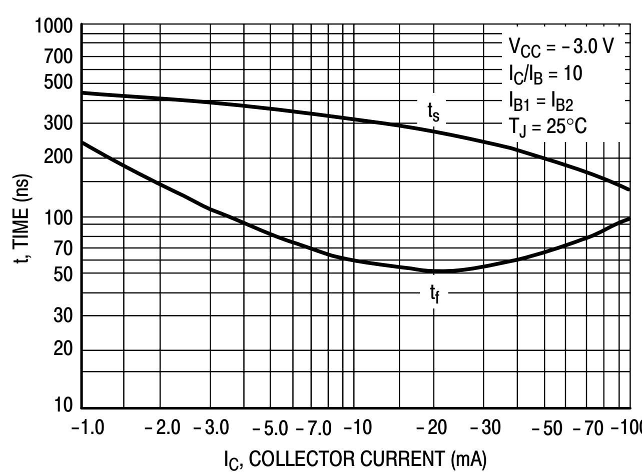


Figure 11. Turn−Off Time

TYPICAL DYNAMIC CHARACTERISTICS

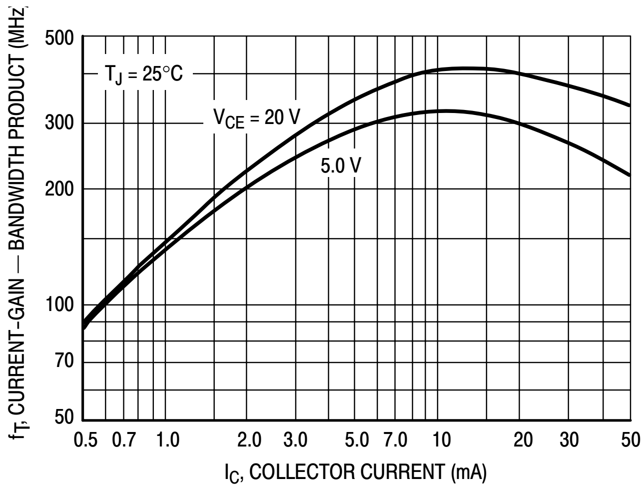


Figure 12. Current−Gain — Bandwidth Product

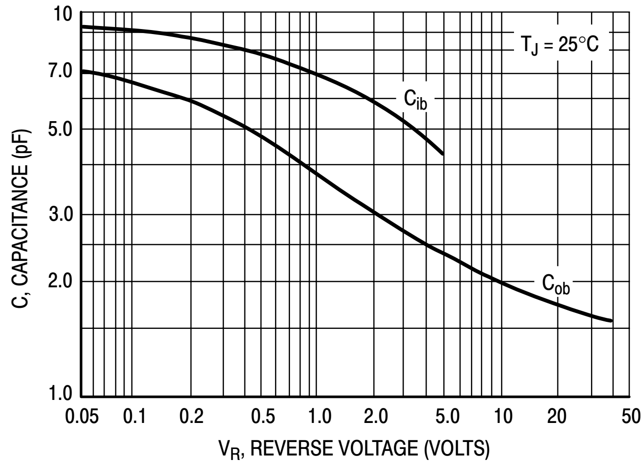


Figure 13. Capacitance

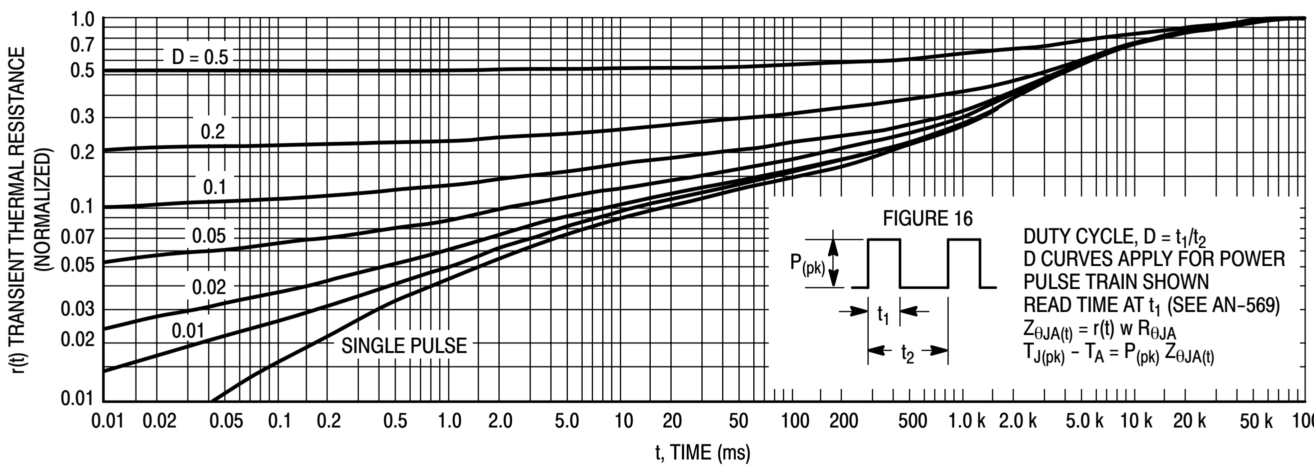


Figure 14. Thermal Response

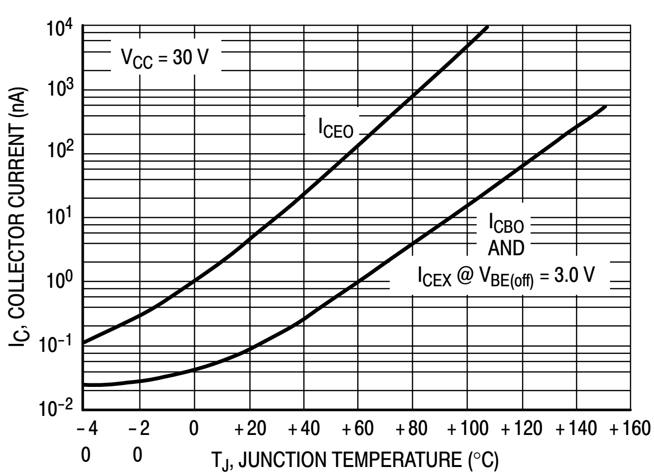


Figure 15. Typical Collector Leakage Current

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 16. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 14 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 14 by the steady state value $R_{\theta JA}$.

Example:

Dissipating 2.0 watts peak under the following conditions:

t_1 = 1.0 ms, t_2 = 5.0 ms (D = 0.2)

Using Figure 14 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

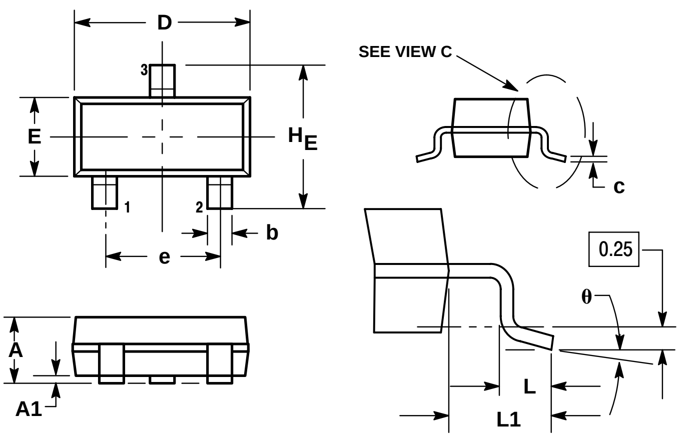
The peak rise in junction temperature is therefore

$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.

For more information, see AN−569.

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN



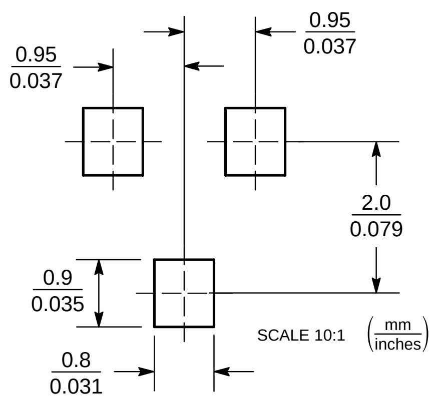
VIEW C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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