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NTE4069 and NTE4069T Integrated Circuit CMOS, Hex Inverter, High Voltage Type

Description:

The NTE4069 (14-Lead DIP) and NTE4069T (SOIC-14) are hex inverters constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

Features:

- Quiescent Current = 0.5nA Typ/Pkg at 5 Vdc
- Noise Immunity = 45% of V_{DD} (Typ)
- Supply Voltage Range = 3Vdc to 18Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs

Absolute Maximum Ratings: (Voltages Referenced to V_{SS} , Note 1)

DC Supply Voltage, V_{DD}	-0.5 to +18.0V
Input Voltage (All Inputs), V_{in}	-0.5 to $V_{DD} + 0.5V$
DC Current Drain (Per Pin), I	10mA
Operating Temperature Range, T_{sA}	-55 to +125°C
Storage Temperature Range, T_{stg}	-65 to +150°C
Lead Temperature (8-Seconds Soldering), T_L	260°C

Note 1. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS} , Note 2)

Parameter	Symbol	V_{DD} Vdc	-55°C		+25°C			+125°C		Unit	
			Min	Max	Min	Typ	Max	Min	Max		
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05	Vdc	
		15	-	0.05	-	0	0.05	-	0.05	Vdc	
	"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	Vdc
			15	14.95	-	14.95	15	-	14.95	-	Vdc
Input Voltage "0" Level ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	-	1.0	-	2.25	1.0	-	1.0	Vdc	
		10	-	2.0	-	4.50	2.0	-	2.0	Vdc	
		15	-	2.5	-	6.75	2.5	-	2.5	Vdc	
	"1" Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IH}	5.0	4.0	-	4.0	2.75	-	4.0	-	Vdc
			10	8.0	-	8.0	5.50	-	8.0	-	Vdc
			15	12.5	-	12.5	8.25	-	12.5	-	Vdc
Output Drive Current Source ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	I_{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc	
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	mAdc	
		10	-1.6	-	-1.3	-2.25	-	-0.9	-	mAdc	
		15	-4.2	-	-3.4	-8.8	-	-2.4	-	mAdc	
	Sink ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	I_{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
			10	1.6	-	1.3	2.25	-	0.9	-	mAdc
15			4.2	-	3.4	8.8	-	2.4	-	mAdc	
Input Current	I_{in}	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 0.1	μ Adc	
Input Capacitance ($V_{IN} = 0$)	C_{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I_{DD}	5.0	-	0.25	-	0.0005	0.25	-	7.5	μ Adc	
		10	-	0.5	-	0.0010	0.5	-	15	μ Adc	
		15	-	1.0	-	0.0015	1.0	-	30	μ Adc	
Total Supply Current (Dynamic plus Quiescent, Per Gate, $C_L = 50$ pF, Note 3, Note 4)	I_T	5.0	$I_T = (0.3\mu A/kHz) f + I_{DD}/6$							μ Adc	
		10	$I_T = (0.6\mu A/kHz) f + I_{DD}/6$							μ Adc	
		15	$I_T = (0.8\mu A/kHz) f + I_{DD}/6$							μ Adc	

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 6 \times 10^{-3}(C_L - 50) V_{DD}f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

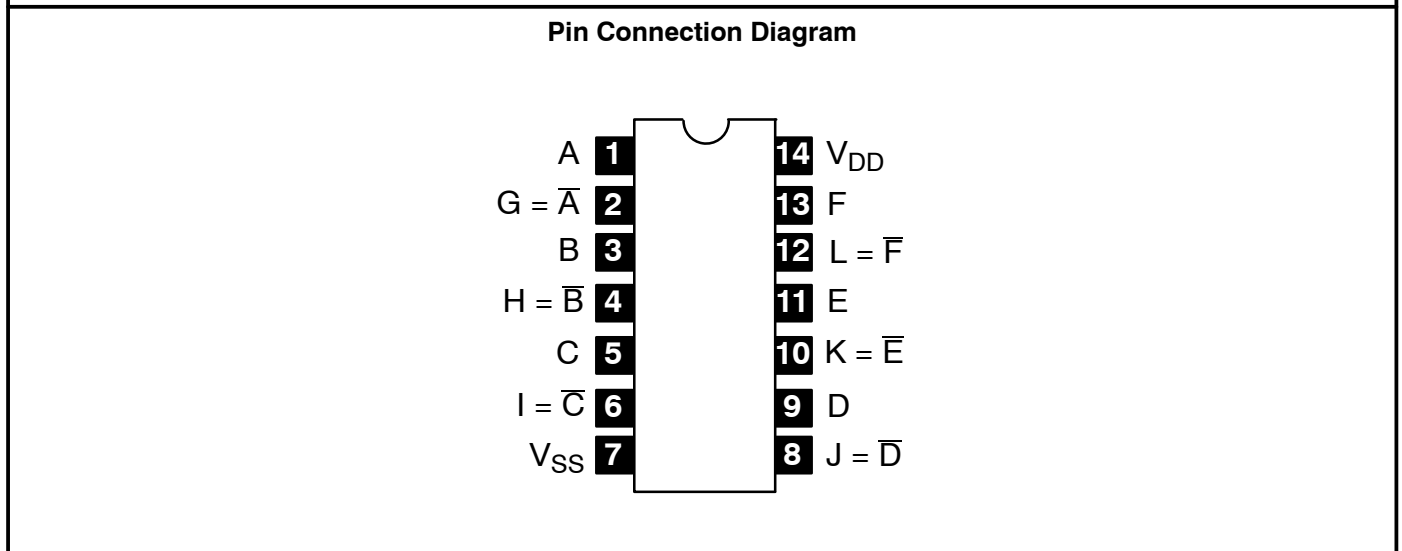
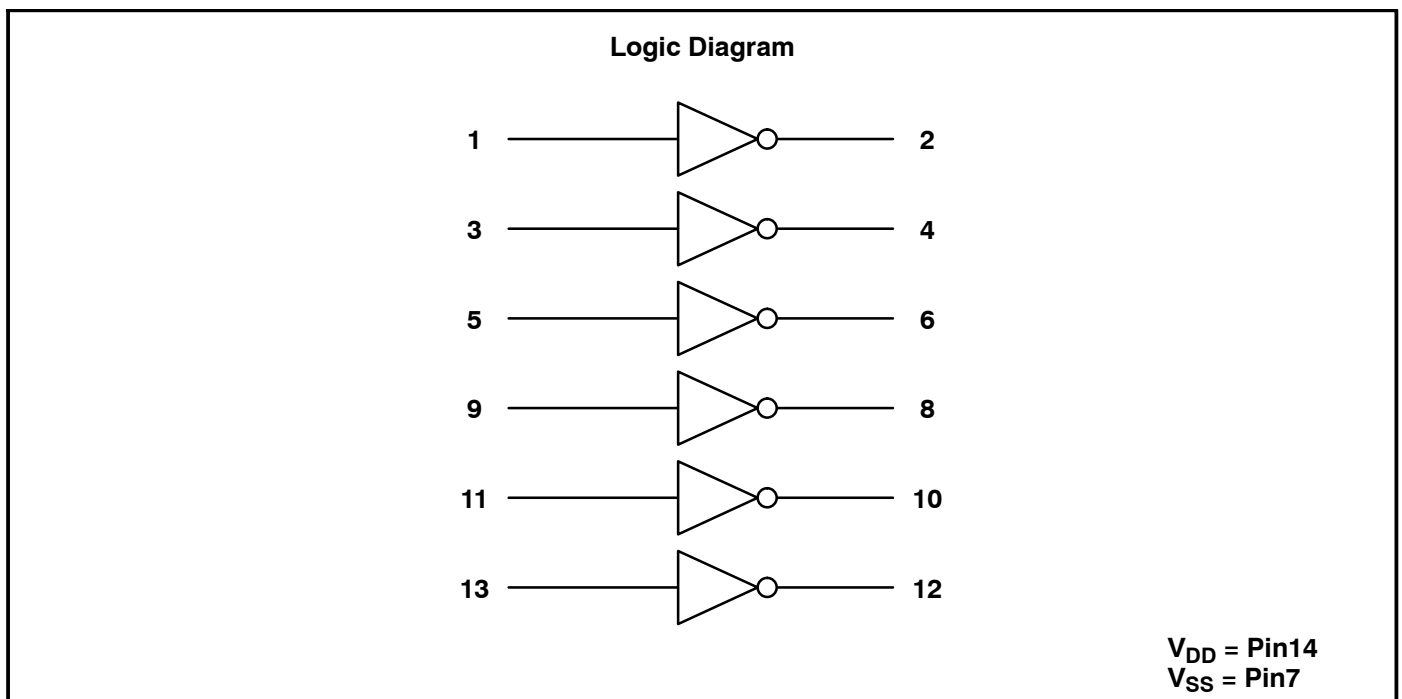
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Switching Characteristics: ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 2)

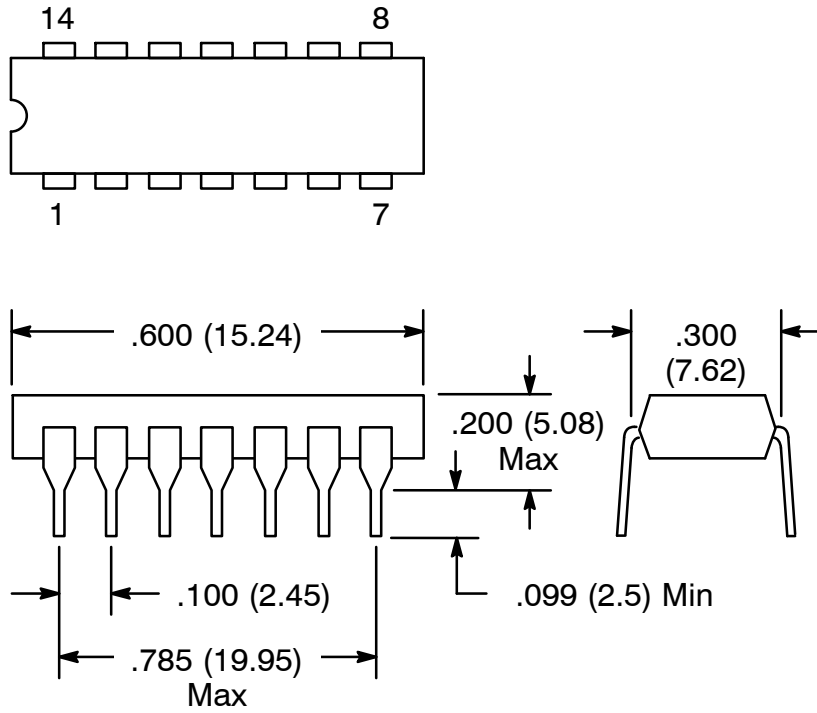
Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Times $t_{TLH}, t_{THL} = (1.35\text{ns/pf}) C_L + 33\text{ns}$ $t_{TLH}, t_{THL} = (0.60\text{ns/pf}) C_L + 20\text{ns}$ $t_{TLH}, t_{THL} = (0.40\text{ns/pf}) C_L + 20\text{ns}$	t_{TLH}, t_{THL}	5.0	-	100	200	ns
		10	-	50	100	ns
		15	-	40	80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (0.90\text{ns/pf}) C_L + 20\text{ns}$ $t_{PLH}, t_{PHL} = (0.36\text{ns/pf}) C_L + 22\text{ns}$ $t_{PLH}, t_{PHL} = (0.26\text{ns/pf}) C_L + 17\text{ns}$	t_{PLH}, t_{PHL}	5.0	-	65	125	ns
		10	-	40	75	ns
		15	-	30	55	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

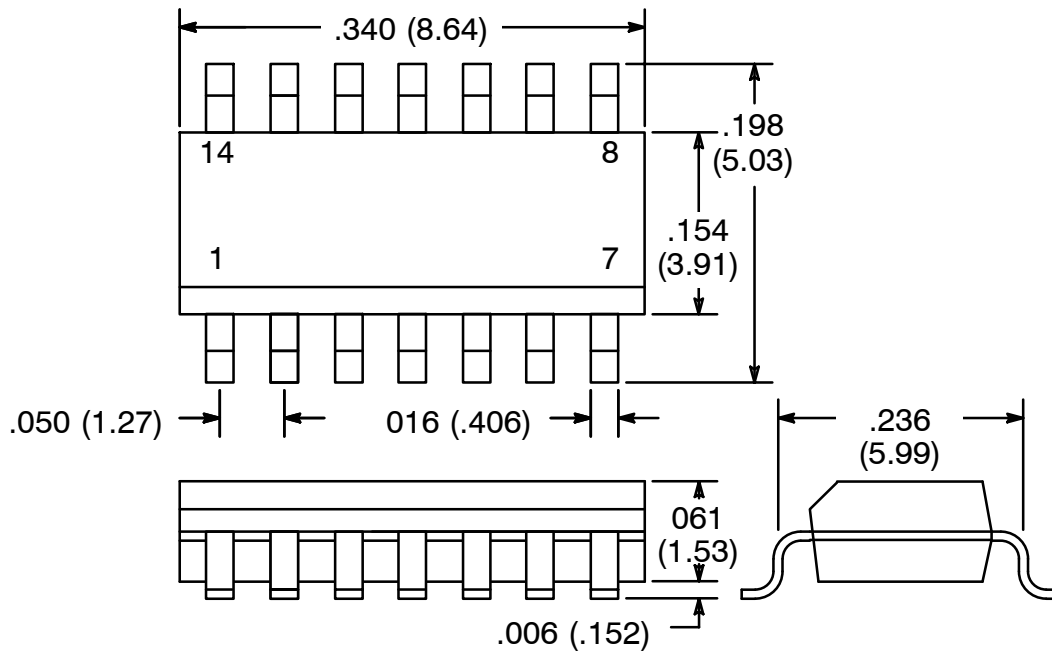
Note 3. The formulas given are for the typical characteristics only at $+25^\circ\text{C}$.



NTE4069



NTE4069T



NOTE: Pin1 on Beveled Edge