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November 2013

FQD30N06

N-Channel QFET® MOSFET

60 V, 22.7 A, $45~\text{m}\Omega$

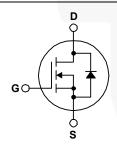
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 22.7 A, 60 V, $R_{DS(on)}$ = 45 m Ω (Max.) @ V_{GS} = 10V, ID = 11.4 A
- Low Gate Charge (Typ. 19 nC)
- Low Crss (Typ. 40 pF)
- · 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

| Symbol | Parameter | | | FQD30N06TM | Unit |
|-----------------------------------|---|-----------------------------------|----------|-------------|------|
| V_{DSS} | Drain-Source Voltage | | | 60 | V |
| I _D | Drain Current - Continuous (T _C = 25°C) | | °C) | 22.7 | А |
| | | - Continuous (T _C = 10 | 0°C) | 14.3 | Α |
| I _{DM} | Drain Current | - Pulsed | (Note 1) | 90.8 | Α |
| V _{GSS} | Gate-Source Vo | Gate-Source Voltage | | ± 25 | V |
| E _{AS} | Single Pulsed A | ngle Pulsed Avalanche Energy | | 280 | mJ |
| I _{AR} | Avalanche Current | | (Note 1) | 22.7 | Α |
| E _{AR} | Repetitive Avalanche Energy | | (Note 1) | 4.4 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | | (Note 3) | 7.0 | V/ns |
| P_{D} | Power Dissipation (T _A = 25°C) * | | | 2.5 | W |
| | Power Dissipation (T _C = 25°C) | | | 44 | W |
| - Derate above | | - Derate above 25°C | | 0.35 | W/°C |
| T _J , T _{STG} | Operating and Storage Temperature Range | | nge | -55 to +150 | °C |
| T _L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | | 300 | °C |

Thermal Characteristics

| Symbol | Parameter | FQD30N06TM | Unit |
|-----------------|---|------------|------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Max. | 2.85 | |
| В | Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max. | 110 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max. | 50 | |

Package Marking and Ordering Information

| Part Number | Top Mark | Package | Packing Method | Reel Size | Tape Width | Quantity |
|-------------|----------|---------|----------------|-----------|------------|------------|
| FQD30N06TM | FQD30N06 | D-PAK | Tape and Reel | 330 mm | 16 mm | 2500 units |

Electrical Characteristics T_C = 25°C unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Тур. | Max. | Unit |
|---|--|--|------|-------|-------|------|
| Off Cha | aracteristics | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$ | 60 | | | V |
| ΔBV _{DSS} / ΔT _J | Breakdown Voltage Temperature Coefficient | I _D = 250 μA, Referenced to 25°C | | 0.06 | | V/°C |
| I _{DSS} | Zana Oata Valtana Basin Ourset | V _{DS} = 60 V, V _{GS} = 0 V | | | 1 | μΑ |
| Zero Gate Vol | Zero Gate Voltage Drain Current | V _{DS} = 48 V, T _C = 125°C | | | 10 | μА |
| I _{GSSF} | Gate-Body Leakage Current, Forward | V _{GS} = 25 V, V _{DS} = 0 V | | | 100 | nA |
| I _{GSSR} | Gate-Body Leakage Current, Reverse | $V_{GS} = -25 \text{ V}, V_{DS} = 0 \text{ V}$ | | | -100 | nA |
| On Cha | racteristics | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_{D} = 250 \mu A$ | 2.0 | | 4.0 | V |
| R _{DS(on)} | Static Drain-Source On-Resistance | V _{GS} = 10 V, I _D = 11.4 A | | 0.036 | 0.045 | Ω |
| 9 _{FS} | Forward Transconductance | V _{DS} = 25 V, I _D = 11.4 A | \ | 15 | | S |
| | ic Characteristics | | | | | |
| C _{iss} | Input Capacitance $V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ | | | 725 | 945 | pF |
| C _{oss} | Output Capacitance | f = 1.0 MHz | | 270 | 350 | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 40 | 52 | pF |
| Switchi | ing Characteristics | | | | | |
| t _{d(on)} | Turn-On Delay Time | $V_{DD} = 30 \text{ V}, I_{D} = 15 \text{ A},$ $R_{G} = 25 \Omega$ | | 10 | 30 | ns |
| t _r | Turn-On Rise Time | | | 85 | 180 | ns |
| t _{d(off)} | Turn-Off Delay Time | 1.6 2022 | | 35 | 80 | ns |
| t _f | Turn-Off Fall Time | (Note 4) | | 40 | 90 | ns |
| Qg | Total Gate Charge | V _{DS} = 48 V, I _D = 30 A, | | 19 | 25 | nC |
| Q _{gs} | Gate-Source Charge | V _{GS} = 10 V | | 5.4 | | nC |
| Q _{gd} | Gate-Drain Charge | (Note 4) | / | 8.5 | | nC |
| Drain-S | ource Diode Characteristics a | nd Maximum Ratings | | | | |
| I _S | Maximum Continuous Drain-Source Diode Forward Current | | | | 22.7 | Α |
| I _{SM} | Maximum Pulsed Drain-Source Diode F | Forward Current | | | 90.8 | Α |
| V _{SD} | Drain-Source Diode Forward Voltage | V _{GS} = 0 V, I _S = 22.7 A | | | 1.5 | V |
| t _{rr} | Reverse Recovery Time | V _{GS} = 0 V, I _F = 30 A, | | 45 | | ns |
| Q _{rr} | Reverse Recovery Charge | dI _F / dt = 100 A/μs | | 65 | // | nC |

Notes: 1. Repetitive rating : pulse-width limited by maximum junction temperature. 2. L = 630 μ H, I_{AS} = 22.7 A, V_{DD} = 25 V, R_G = 25 Ω , starting T_J = 25°C. 3. I_{SD} ≤ 30 A, di/dt ≤ 300 A/ μ s, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C. 4. Essentially independent of operating temperature.

Typical Characteristics

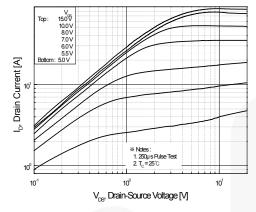


Figure 1. On-Region Characteristics

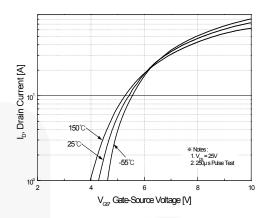


Figure 2. Transfer Characteristics

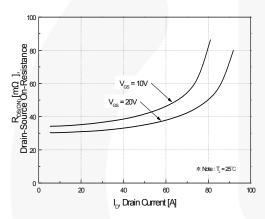


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

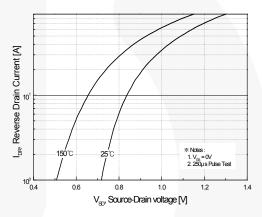


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

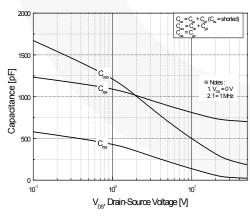


Figure 5. Capacitance Characteristics

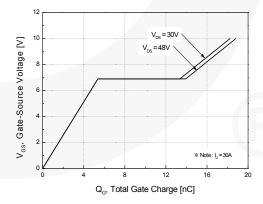


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

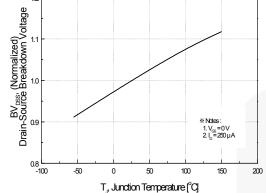


Figure 7. Breakdown Voltage Variation vs. Temperature

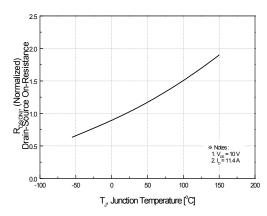


Figure 8. On-Resistance Variation vs. Temperature

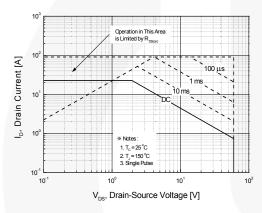


Figure 9. Maximum Safe Operating Area

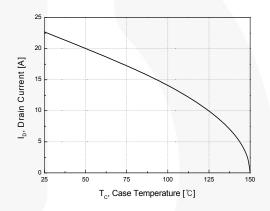


Figure 10. Maximum Drain Current vs. Case Temperature

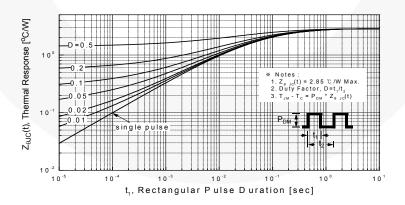


Figure 11. Transient Thermal Response Curve

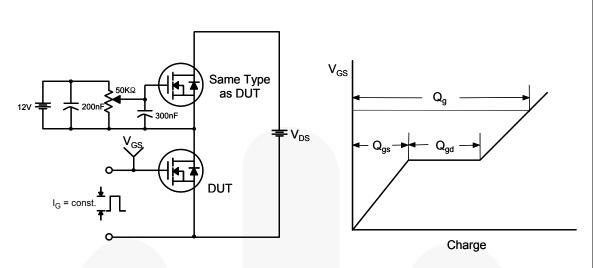


Figure 12. Gate Charge Test Circuit & Waveform

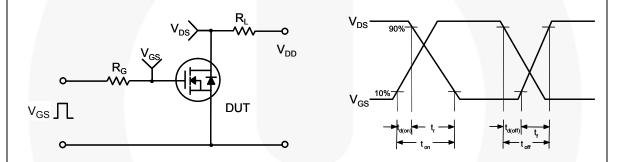


Figure 13. Resistive Switching Test Circuit & Waveforms

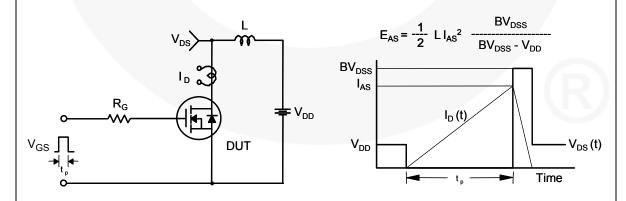
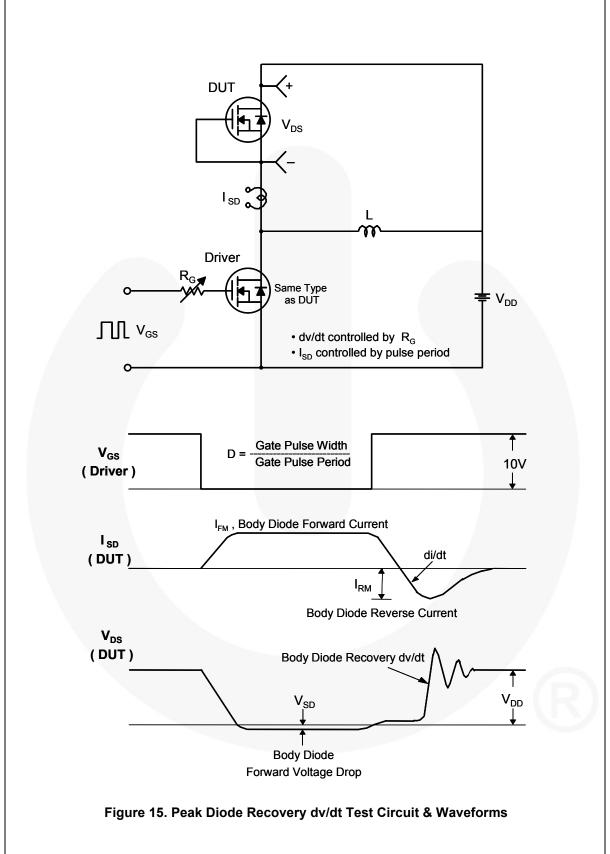


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions

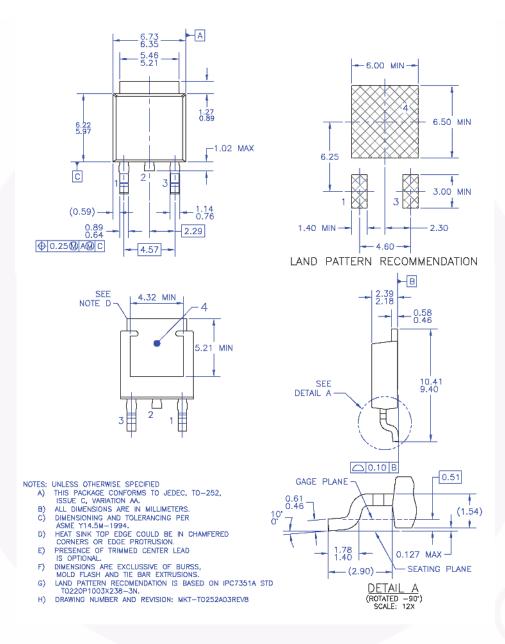


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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