FAIRCHILD
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FSDM311
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged SenseFET
- Precision Fixed Operating Frequency (67KHz)
- Advanced Burst-Mode Operation (power consumption < 0.1W at 265VAC, no-load condition)
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limit
- Over-Voltage Protection (OVP)
- Over-Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO) with Hysteresis
- Built-in Soft-Start

Applications

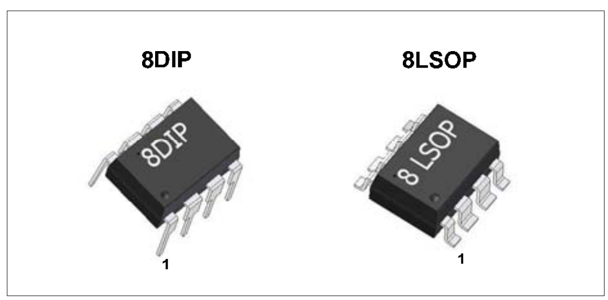
- Charger & Adapter for Mobile Phone, PDA & MP3
- Auxiliary Power for White Goods, PC, C-TV & Monitor

Related Application Notes

- AN-4137, AN-4141, AN-4147 (Flyback)
- AN-4134 (Forward)
- AN-4138 (Charger)

Description

The FSDM311, consisting of integrated Pulse-Width Modulator (PWM) and SenseFET, is specifically designed for high-performance, off-line Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high-voltage, power-switching regulator which combines a VDMOS SenseFET with a voltage mode PWM control block. The integrated PWM controller features include: a fixed oscillator, Under-Voltage Lockout (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature-compensated, precision-current sources for loop-compensation and fault-protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDM311 device reduces total component count and design size and weight; while increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for the design of cost-effective flyback converters.



Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$
FSDM311	8DIP	DM311	650V	67KHz	14Ω
FSDM311L	8LSOP	DM311	650V	67KHz	14Ω

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Typical Application & Output Power Table

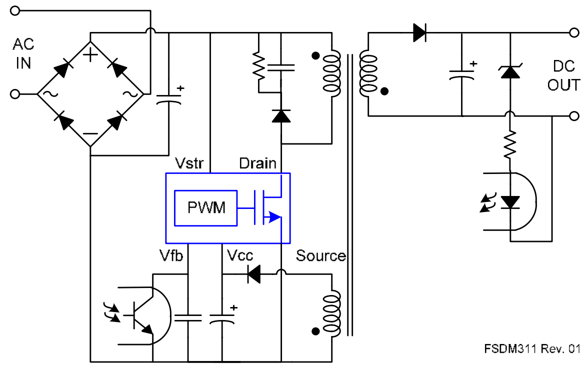


Figure 1 Typical Flyback Application

OUTPUT POWER TABLE		
Product	**Open Frame**(1)	
	230VAC± 15%(2)	**85~265VAC**
FSDM311	13W	8W
FSDM311L	13W	8W

Notes:
1. Maximum practical continuous power in open-frame design with sufficient drain pattern as a heat sink, at 50°C ambient.
2. 230VAC or 100/115VAC with doubler.

Internal Block Diagram

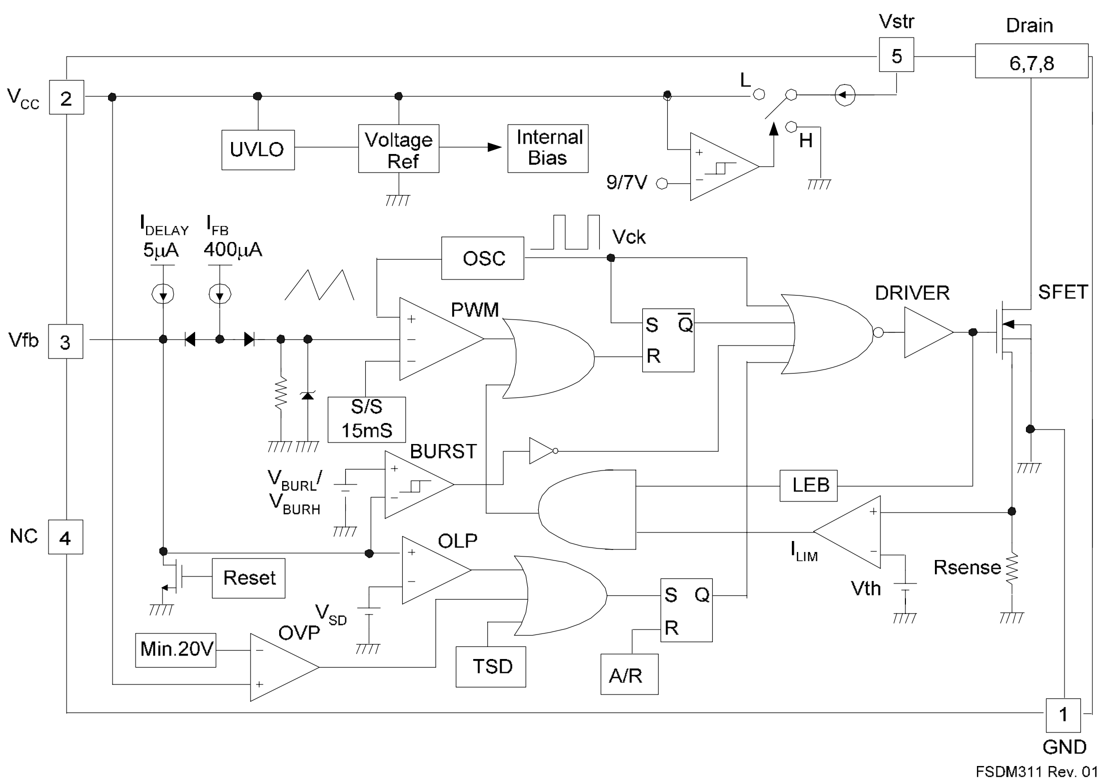


Figure 2 Functional Block Diagram of FSDM311

Pin Assignments

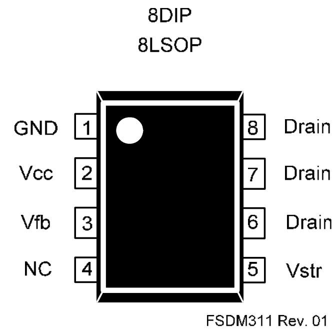


Figure 3 Pin Configuration (Top View)

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	**Ground.** SenseFET source terminal on primary side and internal control ground.
2	V_{CC}	**Positive supply voltage input.** Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during start-up (see Internal Block Diagram section). When V_{CC} reaches the UVLO upper threshold (9V), the internal start-up switch opens and device power is supplied by the auxiliary transformer winding.
3	Vfb	**Feedback.** Inverting input to the PWM comparator with its normal input level between 0.5V and 2.5V. It has a 0.4mA current source connected internally, while a capacitor and opto-coupler are typically connected externally. A feedback voltage of 4.5V triggers overload protection (OLP). There is a time delay while charging the external capacitor Cfb from 3V to 4.5V using an internal 5µA current source. This time delay prevents false triggering under transient conditions, but allows the protection mechanism to operate under true overload conditions.
4	NC	**No Connection**.
5	Vstr	**Start-up.** This pin connects directly to the rectified AC line voltage source. At start-up, the internal switch supplies internal bias and charges an external storage capacitor placed between the V_{CC} pin and ground. Once the V_{CC} reaches 9V, the internal switch stops charging the capacitor.
6,7,8	Drain	**SenseFET Drain.** The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer is recommended to decrease leakage inductance.

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

T_A=25°C, unless otherwise specified.

Symbol	Parameter	Value	Unit
V_{DRAIN}	Drain Pin Voltage	650	V
V_{STR}	Vstr Pin Voltage	650	V
V_{DG}	Drain-Gate Voltage	650	V
V_{GS}	Gate-Source Voltage	±20	V
I_{DM}	Drain Current Pulsed(3)	1.5	A
I_D	Continuous Drain Current (Tc=25°C)	0.5	A
I_D	Continuous Drain Current (Tc=100°C)	0.32	A
E_{AS}	Single Pulsed Avalanche Energy(4)	10	mJ
V_{CC}	Supply Voltage	20	V
V_{FB}	Feedback Voltage Range	-0.3 to V_{STOP}	V
P_D	Total Power Dissipation	1.40	W
T_J	Operating Junction Temperature	Internally limited	°C
T_A	Operating Ambient Temperature	-25 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C

Notes:
3. Repetitive rating: Pulse width is limited by maximum junction temperature.
4. L = 24mH, starting TJ = 25°C.

Thermal Impedance

FSDM311 8DIP. T_A=25°C, unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance(5)	88.84	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance(6)	13.94	°C/W

Notes:
5. Free standing with no heat sink, without copper clad. (Measurement Condition – Just before junction temperature T_J enters into OTP.)
6. Measured on the DRAIN pin close to plastic interface.

All items are tested with the standards JESD 51-2 and 51-10 (DIP).

Electrical Characteristics

T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET SECTION						
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS}=650V, V_{GS}=0V	-	-	25	μA
		V_{DS}=520V, V_{GS}=0V, T_C=125°C	-	-	200	
$R_{DS(ON)}$	Drain-Source On-State Resistance(7)	V_{GS}=10V, I_D=0.5A	-	14	19	Ω
g_{fs}	Forward Trans-Conductance	V_{DS}=50V, I_D=0.5A	1.0	1.3	-	S
C_{ISS}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	162	-	pF
C_{OSS}	Output Capacitance		-	18	-	
C_{RSS}	Reverse Transfer Capacitance		-	3.8	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=325V, I_D=1.0A	-	9.5	-	ns
t_r	Rise Time		-	19	-	
$t_{d(off)}$	Turn-Off Delay Time		-	33	-	
t_f	Fall Time		-	42	-	
Q_g	Total Gate Charge	V_{GS}=10V, I_D=1.0A, V_{DS}=325V	-	7.0	-	nC
Q_{gs}	Gate-Source Charge		-	3.1	-	
Q_{gd}	Gate-Drain (Miller) Charge		-	0.4	-	
CONTROL SECTION						
f_{OSC}	Switching Frequency		61	67	73	KHz
Δf_{OSC}	Switching Frequency Variation(8)	-25°C ≤ T_A ≤ 85°C	-	±5	±10	%
D_{MAX}	Maximum Duty Cycle		60	67	74	%
V_{START}	UVLO Threshold Voltage	V_{FB}=GND	8	9	10	V
V_{STOP}		V_{FB}=GND	6	7	8	V
I_{FB}	Feedback Source Current	0V ≤ V_{FB} ≤ 3V	0.35	0.40	0.45	mA
$t_{S/S}$	Internal Soft-Start Time		10	15	20	ms
V_{REF}	Reference Voltage(9)		4.2	4.5	4.8	V
$\Delta V_{REF}/\Delta T$	Reference Voltage Variation with Temperature(8)(9)	-25°C ≤ T_A ≤ 85°C	-	0.3	0.6	mV/°C
BURST-MODE SECTION						
V_{BURH}	Burst-Mode Voltage	T_J=25°C	0.6	0.7	0.8	V
V_{BURL}			0.45	0.55	0.65	V
$V_{BUR(HYS)}$		Hysteresis	-	150	-	mV
PROTECTION SECTION						
I_{LIM}	Peak Current Limit		0.475	0.55	0.625	A
T_{SD}	Thermal Shutdown Temperature(9)		125	145	-	°C
V_{SD}	Shutdown Feedback Voltage		4.0	4.5	5.0	V
V_{OVP}	Over-Voltage Protection		20	-	-	V
I_{DELAY}	Shutdown Delay Current	3V ≤ V_{FB} ≤ V_{SD}	4	5	6	μA
TOTAL DEVICE SECTION						
I_{OP}	Operating Supply Current (control part only)	V_{CC} ≤ 16V	-	1.5	3.0	mA
I_{CH}	Start-Up Charging Current	V_{CC}=0V , V_{STR}=50V	450	550	650	μA

Notes:

7. Pulse test: Pulse width ≤ 300μs, duty ≤ 2%.
8. These parameters, although guaranteed, are tested in EDS (wafer test) process.
9. These parameters, although guaranteed, are not 100% tested in production.

Temperature Characteristics

These characteristic graphs are normalized at T_A = 25°C.

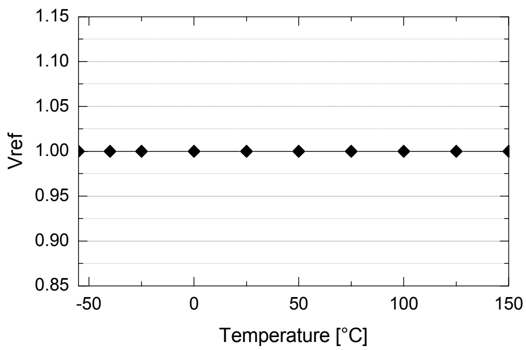


Figure 4 Reference Voltage (V_{REF}) vs. T_A

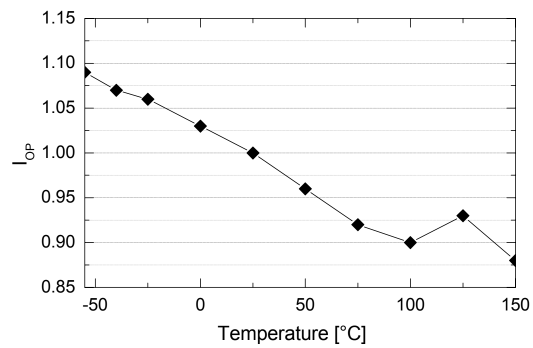


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

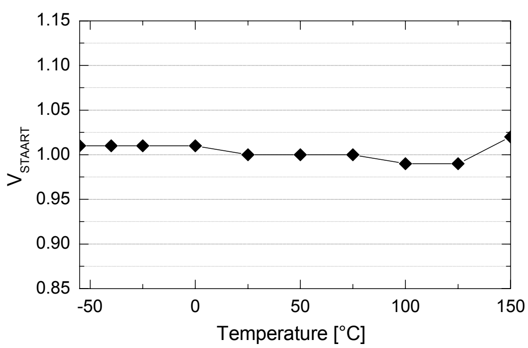


Figure 6. Start Threshold Voltage (V_{START}) vs. T_A

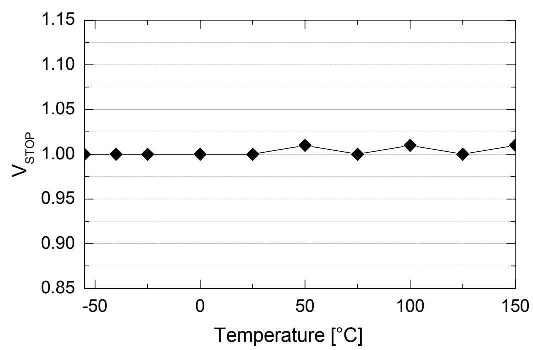


Figure 7. Stop Threshold Voltage (V_{STOP}) vs. T_A

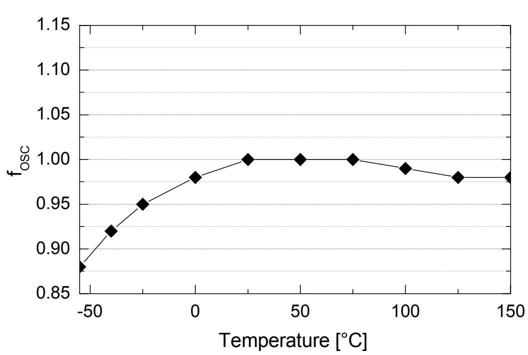


Figure 8. Operating Frequency (f_{OSC}) vs. T_A

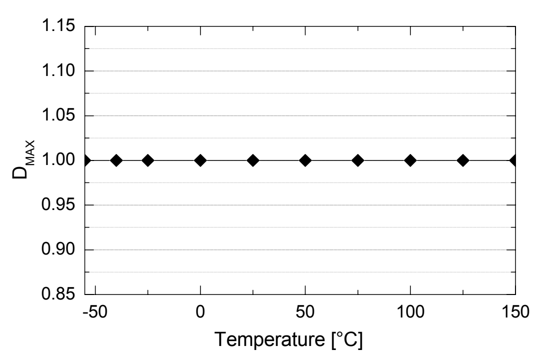


Figure 9. Maximum Duty Cycle (D_{MAX}) vs. T_A

Temperature Characteristics (continued)

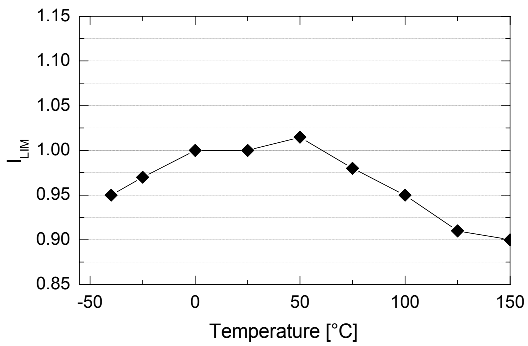


Figure 10. Peak Current Limit (I_{LIM}) vs. T_A

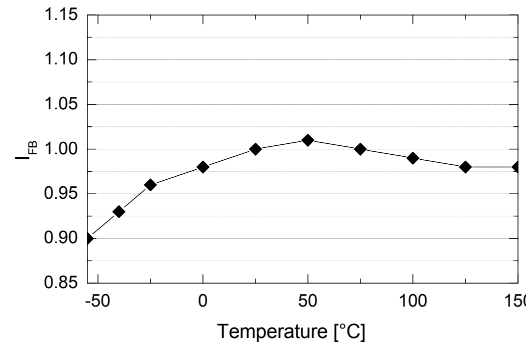


Figure 11. Feedback Source Current (I_{FB}) vs. T_A

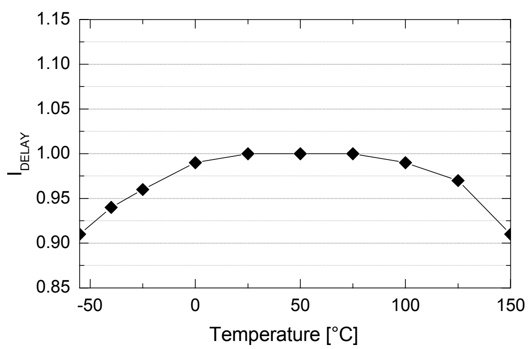


Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

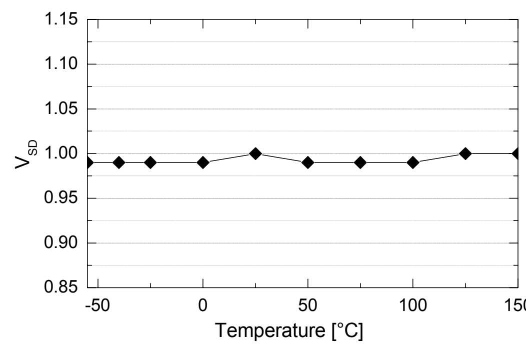


Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

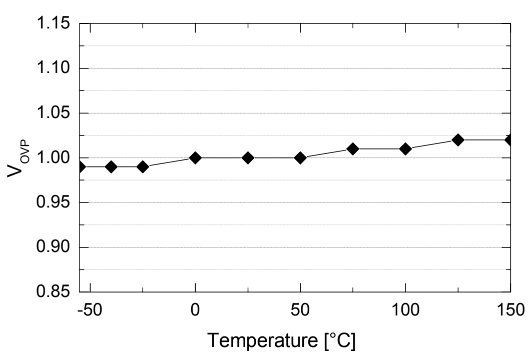


Figure 14. Over-Voltage Protection (V_{OVP}) vs. T_A

Functional Description

1. Start-up: At start-up, the internal high-voltage current source supplies the internal bias and charges the external Vcc capacitor, as shown in Figure 15. In the case of the FSDM311, when Vcc reaches 9V, the device starts switching and the internal high-voltage current source stops charging the capacitor. The device is in normal operation provided that Vcc does not drop below 7V. After start-up, the bias is supplied from the auxiliary transformer winding.

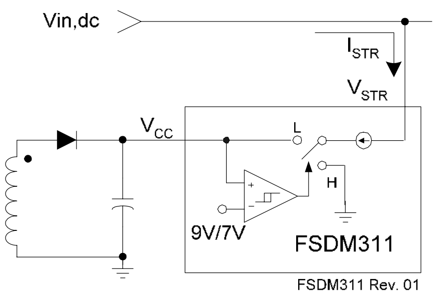


Figure 15. Internal Startup Circuit

Calculating the Vcc capacitor is an important step in design with the FSDM311. At initial start-up in the FSDM311, the maximum value of start operating current I_{START} is about 100µA, which supplies current to UVLO and Vref Blocks. The charging current I_{Vcc} of the Vcc capacitor is equal to I_{STR} - I_{START}. After V_{CC} reaches the UVLO start voltage, only the bias winding supplies Vcc current to the device. When the bias winding voltage is not sufficient, the Vcc level decreases to the UVLO stop voltage and the internal current source is activated again to charge the Vcc capacitor. To prevent this Vcc fluctuation (charging/discharging), a Vcc with a value between 10uF and 47µF should be chosen.

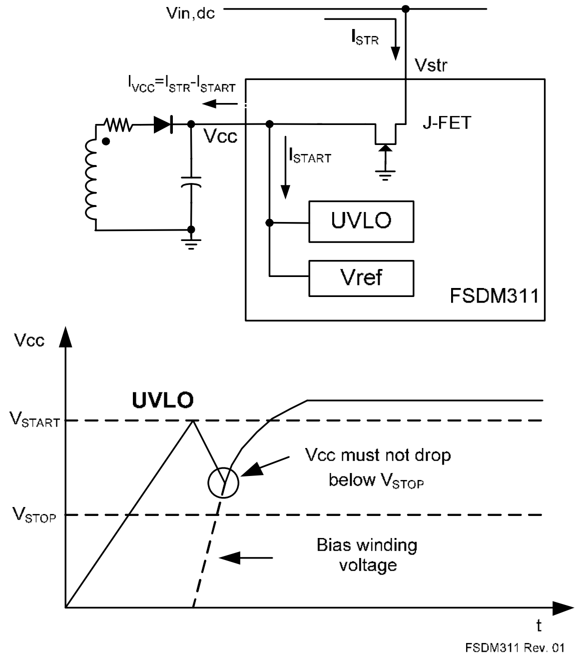


Figure 16. Charging Vcc Capacitor Through Vstr

2. Feedback Control: The FSDM311 is a voltage-mode controlled device, as shown in Figure 17. Usually, an opto-coupler with shunt regulator, like KA431, is used to implement the feedback network. The feedback voltage is compared with an internally generated sawtooth waveform, which directly controls the duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage Vfb is pulled down, and it reduces the duty cycle. This happens when the input voltage increases or the output load decreases.

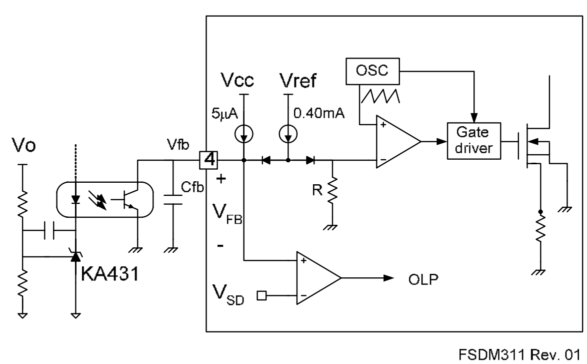
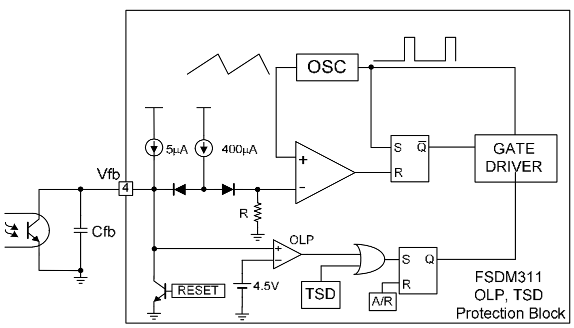


Figure 17. PWM and Feedback Circuit

3. Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high current spike through the SenseFET. Excessive voltage across the R_{sense} resistor leads to incorrect pulse-by-pulse current limit protection. To avoid this, a leading edge blanking (LEB) circuit disables pulse-by-pulse current limit protection block for a fixed time (t_{LEB}) after the SenseFET turns on.

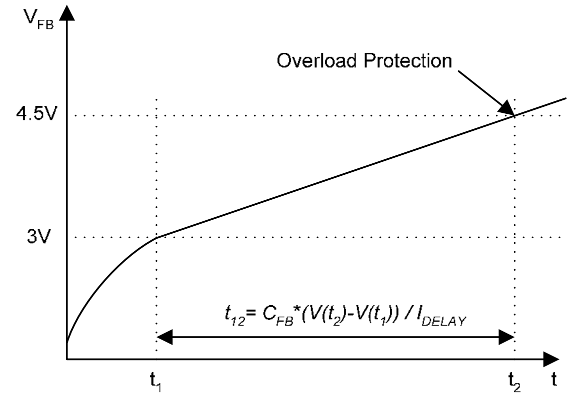
4. Protection Circuit: The FSDM311 has several protective functions, such as overload protection (OLP), over-voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown (TSD). Because these protection circuits are fully integrated in the IC without external components, the reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{cc} to fall. When Vcc reaches the UVLO stop voltage V_{STOP} (7V), the protection is reset and the internal high-voltage current source charges the V_{cc} capacitor via the V_{str} pin. When Vcc reaches the UVLO start voltage V_{START} (9V), the device resumes normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.



FSDM311 Rev. 01

Figure 18. Protection Block

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS is operating normally, the overload protection (OLP) circuit can be activated during the load transition. To avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or true overload situation. If the output consumes more than the maximum power determined by I_{LIM}, the output voltage (V_o) decreases below its rating voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5μA current source (I_{DELAY}) starts to charge C_{fb} slowly up to Vcc. In this condition, V_{FB} increases until it reaches 4.5V, when the switching operation is terminated, as shown in Figure 19. The shutdown delay time is the time required to charge C_{fb} from 3V to 4.5V with a 5μA current source.



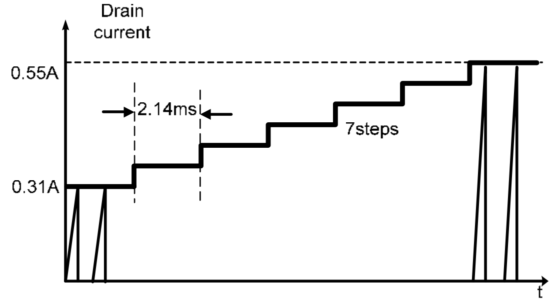
$$t_{12} = C_{FB}\frac{V(t_2) - V(t_1)}{I_{DELAY}}; \quad I_{DELAY} = 5\mu A, V(t_1) = 3V, V(t_2) = 4.5V$$

FSDM311 Rev. 01

Figure 19. Overload Protection (OLP)

4.2 Thermal Shutdown (TSD): The SenseFET and the control IC are integrated, making it easier for the control IC to detect the temperature of the SenseFET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

5. Soft-Start: The FPS has an internal soft-start circuit that slowly increases the feedback voltage, together with the SenseFET current, right after it starts up. The typical soft-start time is 15ms, as shown in Figure 20, where progressive increment of the SenseFET current is allowed during the start-up phase. The soft-start circuit progressively increases current limits to establish proper working conditions for transformers, inductors, capacitors, and switching devices. It also helps to prevent transformer saturation and reduces the stress on the secondary diode.



FSDM311 Rev. 01

Figure 20. Internal Soft-Start

6. Burst Operation: To minimize the power dissipation in standby mode, the FSDM311 enters burst--mode operation. As the load decreases, the feedback voltage decreases. The device automatically enters burst mode when the feedback voltage drops below V_{BURL}(0.55V). At this point, switching stops and the output voltages start to drop. This causes the feedback voltage to rise. Once it passes V_{BURH} (0.70V), switching starts again. The feedback voltage falls and the process repeats. Burst-mode operation alternately enables and disables switching of the power MOSFET to reduce the switching loss in the standby mode.

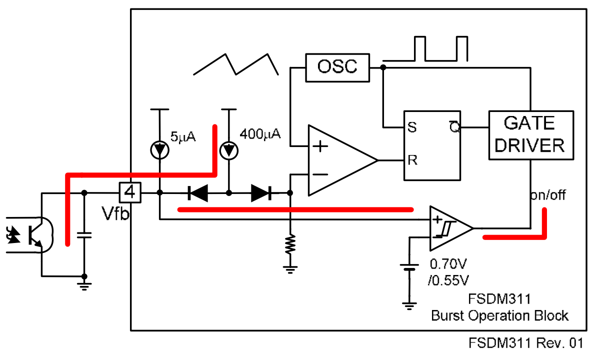


Figure 21. Burst Operation Block

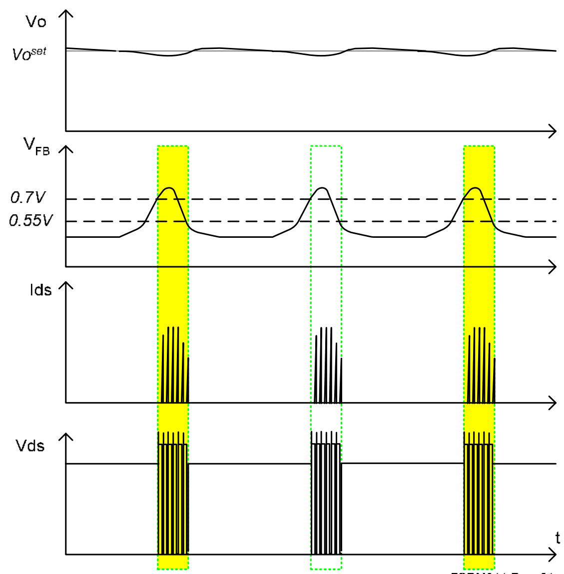


Figure 22. Burst Operation Function

Application Tips

Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components, which generate audible noises when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20KHz, they can make noise in some load conditions. Designers can employ several methods to reduce noise, including:

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil; and the chattering or magnetostriction of core, can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise, but can crack the core because sudden changes in the ambient temperature cause the core and the glue to expand or shrink at different rates.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber is another noise reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. It is possible to use a Zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of the 2~4KHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4KHz. When the fundamental frequency of noise is located in this range, the noise is perceived as louder, although the noise intensity level is identical. Refer to Figure 23 for equal loudness curves.

When FPS acts in burst mode and the burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of burst mode operation lies in the range of 2~4KHz, adjusting the feedback loop can shift the burst operation frequency. To reduce the burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D), and feedback capacitor (C_B); and decrease a feedback gain resistor (R_F), as shown in Figure 24.

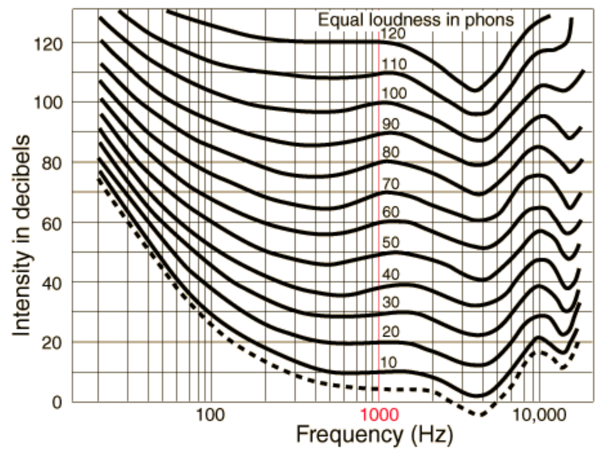


Figure 23. Equal Loudness Curves

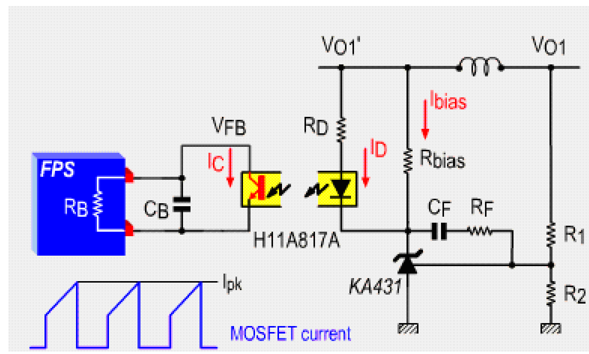


Figure24. Typical Feedback Network of FPS

Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)

AN-4138: Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch (FPS™)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for Fairchild Power Switch (FPS™) Applications

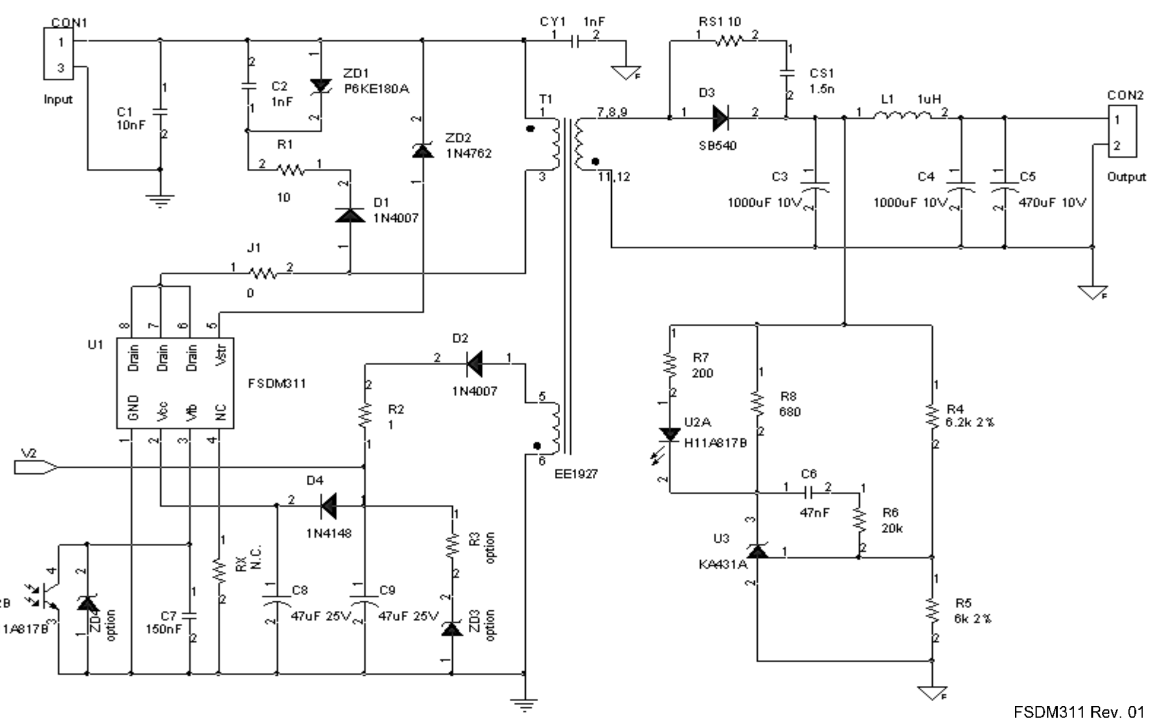
Typical Application Example

Application	Output Power	Input Voltage	Output Voltage (Max. Current)
PC Standby Power (Demo board)	12.5W	DC 275~375V	5.1V (2.5A, isolated) 15V (20mA, non-isolated)
	10W	DC 120~375V	5.1V (2.0A, isolated) 15V (20mA, non-isolated)

Features

- Auxiliary Power for PC Power Supply with Passive PFC
  DC Input Voltage 275V ~ 375V (Voltage Doubler) for 12.5W Output
  DC Input Voltage 120V ~ 375V (Off-Line Universal Input) for 10W Output
- Isolated Secondary Output 5.1V / 2.5A (max), 3.5A (peak) @V_{IN}=275~375VDC
  Isolated Secondary Output 5.1V / 2.0A (max), 2.5A (peak) @V_{IN} =120~375VDC
- Non-Isolated Aux-Output 15V(13~17V) / 10mA (up to 20mA)
- Regulation 5.1V ± 2.5% - Accuracy depends on Reference (e.g. shunt regulator or precision resistors)
- Low No-Load Power Consumption:
  < 100mW @ All Input Voltage
  < 820mW @ All Input Voltage, 0.5W Output
- High Efficiency:
  > 80% @ 375Vdc Input, 12.5W Output
  > 79% @ 160Vdc Input, 10W Output

Schematic



Note: The selection of aux-winding diode D2 affects Aux-Output (Vcc) regulation. If another component should be used, its validity must be verified experimentally.

Figure 25. Schematic of FSDM311 PC Standby Power

Transformer Construction

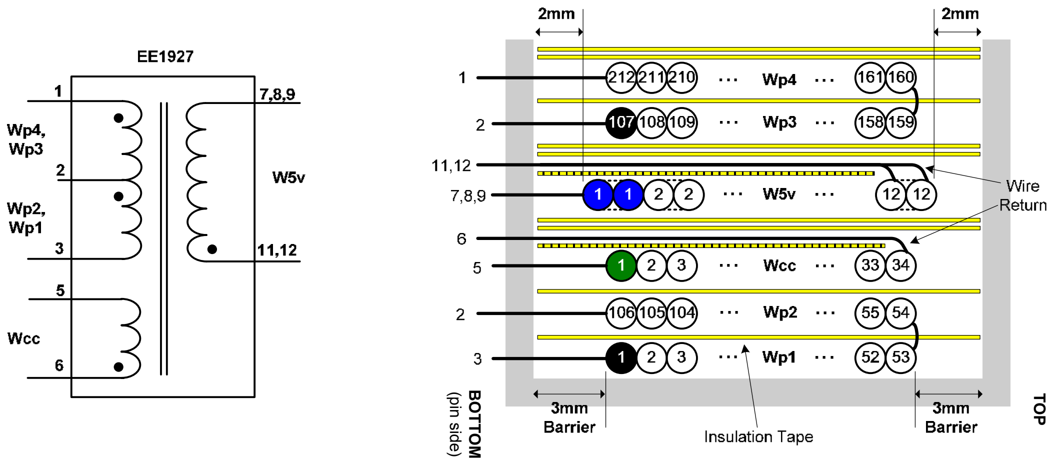


Figure 26. Transformer Construction Diagram

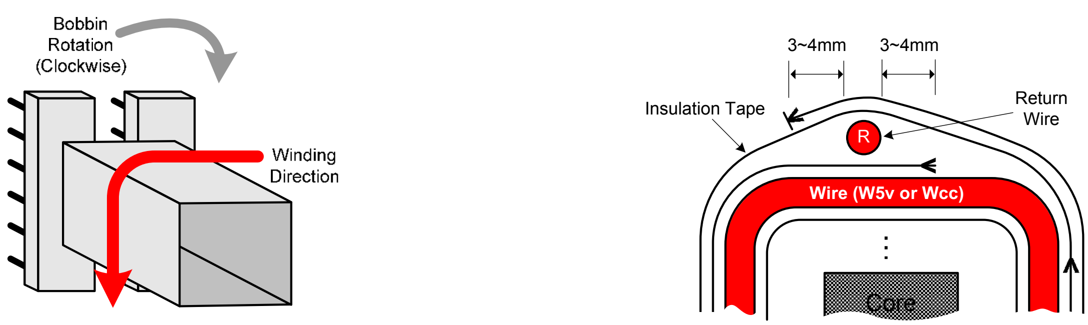


Figure 27. Winding Direction for Each Winding (Left) and Cross-Sectional View for W5v / Wcc Insulation Taping (Right)

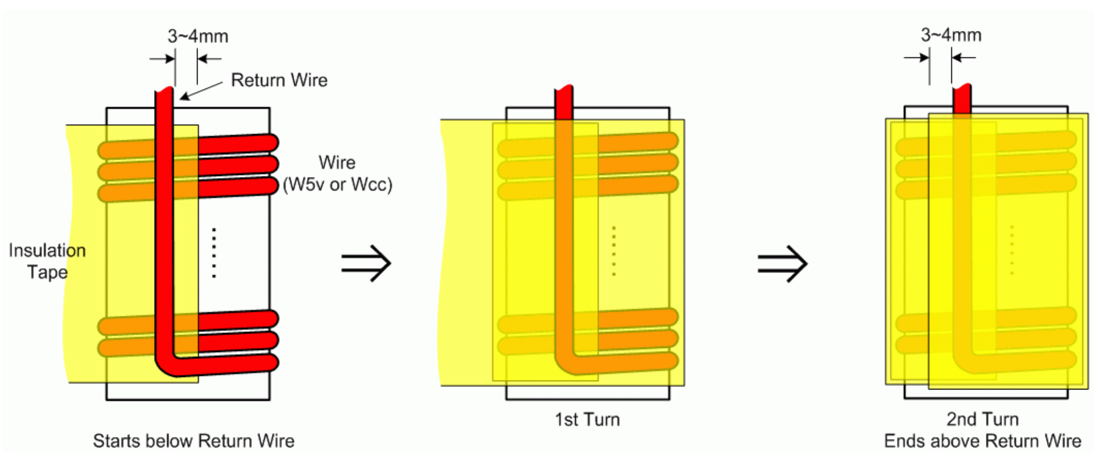


Figure 28. Details on W5v / Wcc Insulation Taping

Winding Specification

All windings should be wound tightly and evenly across the bobbin.

	Winding	Pin(S → F)	Wire (φ:mm)	Turns	Winding Method
Top	Insulation: Polyester Tape t = 0.025mm, 2 Layers[10]				
	Wp4	f_2 → 1	0.22φ ×1	53	Solenoid winding
	Insulation: Polyester Tape t = 0.025mm, 1 Layers[10]				
	Wp3	2 → f_2	0.22φ ×1	53	Solenoid winding
	Insulation: Polyester Tape t = 0.025mm, 2 Layers[11]				
	W5v	7,8,9 → 11,12	0.55φ ×2	12	Bifilar Solenoid winding
	Insulation: Polyester Tape t = 0.025mm, 2 Layers[11]				
	Wcc	5 → 6	0.35φ ×1	34	Solenoid winding
	Insulation: Polyester Tape t = 0.025mm, 1 Layers[10]				
	Wp2	f_1 → 2	0.22φ ×1	53	Solenoid winding
	Insulation: Polyester Tape t = 0.025mm, 1 Layers[10]				
Bottom	Wp1	3 → f_1	0.22φ ×1	53	Solenoid winding

Notes:

10. Overlapped section length between the start and the end of insulation tape is about 3mm – see Figure 29.
11. See Figure 27 (right) and Figure 28 for details.

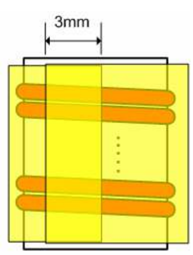


Figure 29. Overlapped Section of Insulation Taping

Electrical Characteristics

	Pin	Specification	Remark
Magnetizing Inductance (Lm)	1 – 3	2.3mH (typical) (2.2mH < Lm ≤ 2.4mH)	67KHz, 1 V All other pins open
Leakage Inductance	1 – 3	< 35µH	67KHz, 1V All other pins shorted
First Resonant Frequency	1 – 3	> 630KHz	All other pins open

Core & Bobbin

- Core: EE1927S (SAMWHA Electronics, PL7 / Ae = $23.4mm^2$)
- Bobbin: Vertical, 12 pins, 6 pins at each side, 20mm width (bobbin wall to wall)

Circuit Part List

Item	Qty.	Reference	Value	Description
1	1	CS1	1.5nF 50V	MLCC X7R, ±10% Tolerance SMD 0805
2	1	CY1	1nF AC250V	Y1 Safety Capacitor
3	1	C1	10nF 1KV	Ceramic
4	1	C2	1nF 1KV	Ceramic
5	2	C3, C4	1000µF 10V	Low ESR (40mΩ) Electrolytic (e.g. Samwha Electric WB series)
6	1	C5	470µF 10V	Low ESR (70mΩ) Electrolytic (e.g. Samwha Electric WB series)
7	1	C6	47nF 50V	Ceramic X7R, ±5% Tolerance
8	1	C7	150nF 50V	Ceramic X7R, ±5% Tolerance
9	2	C8, C9	47µF 25V	Electrolytic
10	2	D1, D2	1N4007	1A, 1000V Diode (Fairchild Semiconductor)
11	1	D3	SB540	5A, 40V Schottky Diode
12	1	D4	1N4148	200mA, 100V Fast Switching Diode (Fairchild Semiconductor)
13	1	J1	(Wire)	Jumper (Test Point)
14	1	L1	1µH	3.5A Inductor
15	1	RS1	10Ω	Resistor 1/4W SMD 1206
16	1	R1	10Ω	Resistor 1/4W
17	1	R2	1Ω	Resistor 1/4W
		(R3)		Option for V2 Voltage Clamping
18	1	R4	6.2kΩ 2%	2% Precision Resistor 1/4W
19	1	R5	6kΩ 2%	2% Precision Resistor 1/4W
20	1	R6	20kΩ	Resistor 1/4W
21	1	R7	200Ω	Resistor 1/4W
22	1	R8	680Ω	Resistor 1/4W
23	1	T1	EE1927S	Transformer (Core: EE1927S Samwha Electronics)
24	1	U1	FSDM311	Fairchild Power Switch (Fairchild Semiconductor FPS)
25	1	U2	H11A817B	Opto-coupler (Fairchild Semiconductor)
26	1	U3	KA431A	Shunt Regulator (Fairchild Semiconductor)
27	1	ZD1	P6KE180A	180V TVS
28	1	ZD2	1N4763A	91V 1W Zener Diode
		(ZD3)		Option for V2 Voltage Clamping
		(ZD4)		Option for Protecting VFB Pin

Layout Information

Single layer, size 59 x 40mm

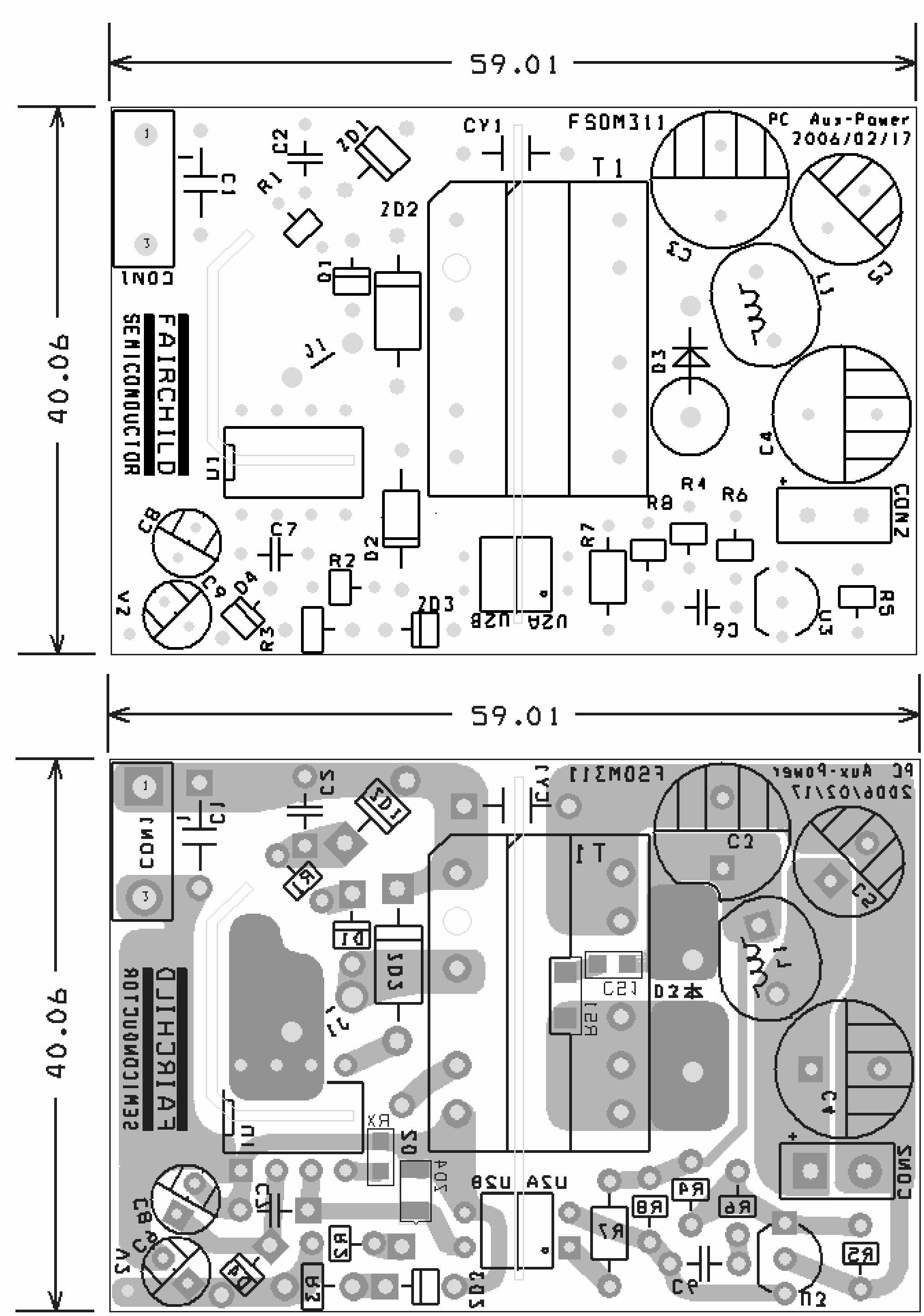
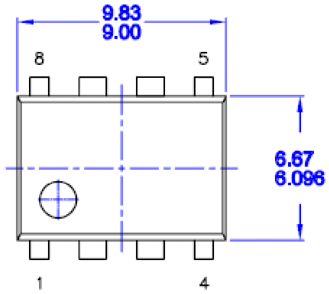


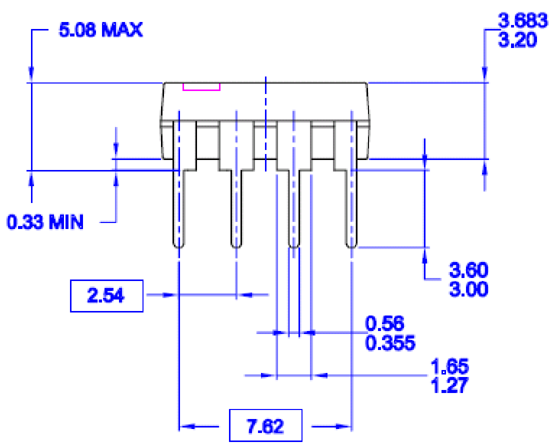
Figure 30. PCB Layout – Top- Side Print (Top) and Bottom-Side Print (Bottom)

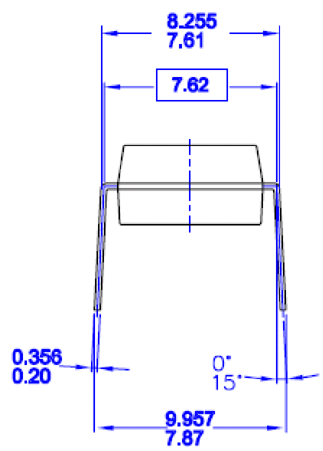
Physical Dimensions

8-DIP

Dimensions are in millimeters (inches) unless otherwise noted.







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MKT-N08FrevB

Physical Dimensions (Continued)

8-LSOP

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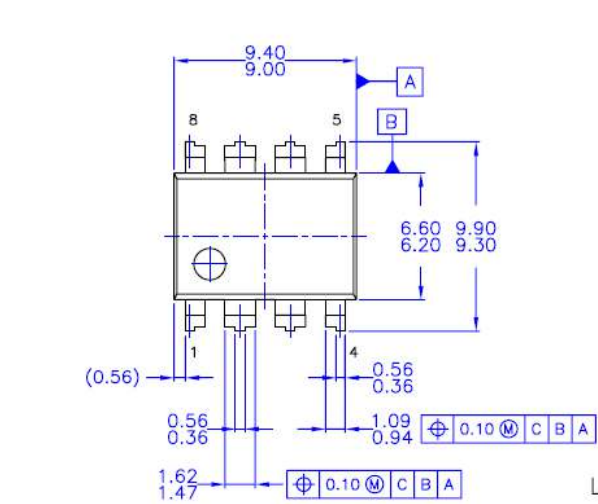
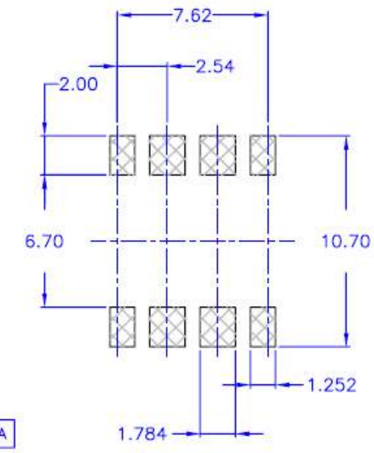
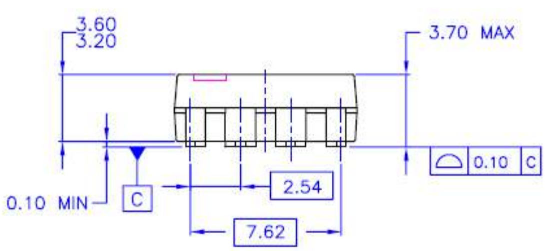
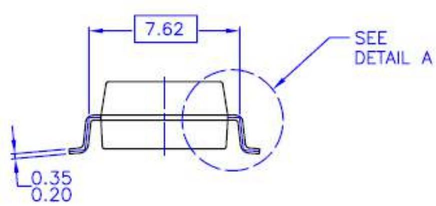
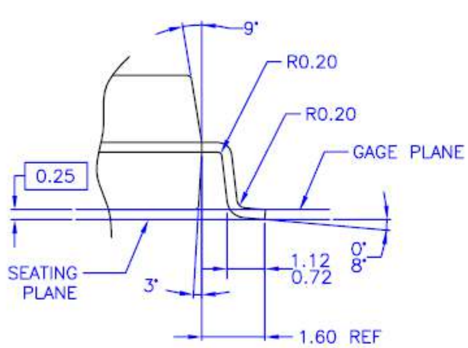




LAND PATTERN RECOMMENDATION







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