

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

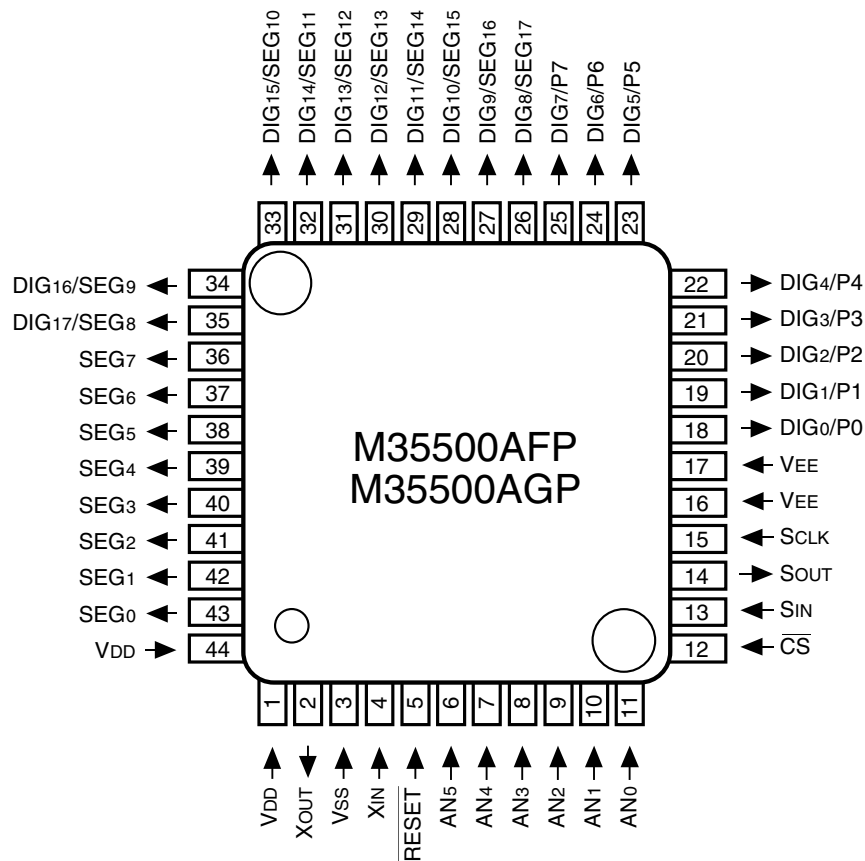
MITSUBISHI LINEAR IC's **M35500AFP/AGP**

FLD CONTROLLER

DESCRIPTION/FEATURES

- High-breakdown-voltage output port 26
 - Segment output 8 to 18
 - Digit output 7 to 10
 (Ports P0 to P7 are also used as ordinary output ports)
 - Output breakdown $V_{cc} - 45 V$
 - Output current $-18 mA$ (DIG0 to DIG17),
 $-7 mA$ (SEG0 to SEG7)
 - Pull-down resistor build-in
 - Dimmer switch 4 levels
- A-D converter 8-bit X 6 channels
 - Absolute accuracy $\pm 3 LSB$
- Serial I/O 4 (CS controller, external clock)
 - Noise filter build-in
 (in serial input pin and clock pin, 2 MHz sampling)
 - FLD display data input
 - A-D conversion data output
 - Command input
- Package 44P6N/44P6X
- Oscillating circuit CR oscillating circuit (external capacitor)
 - Oscillating frequency 4 MHz
- Power source voltage 4.0 to 5.5 V

PIN CONFIGURATION (TOP VIEW)



Package type: 44P6N/44P6X

Fig. 1. Pin configuration of M35500AFP/AGP

FUNCTIONAL BLOCK

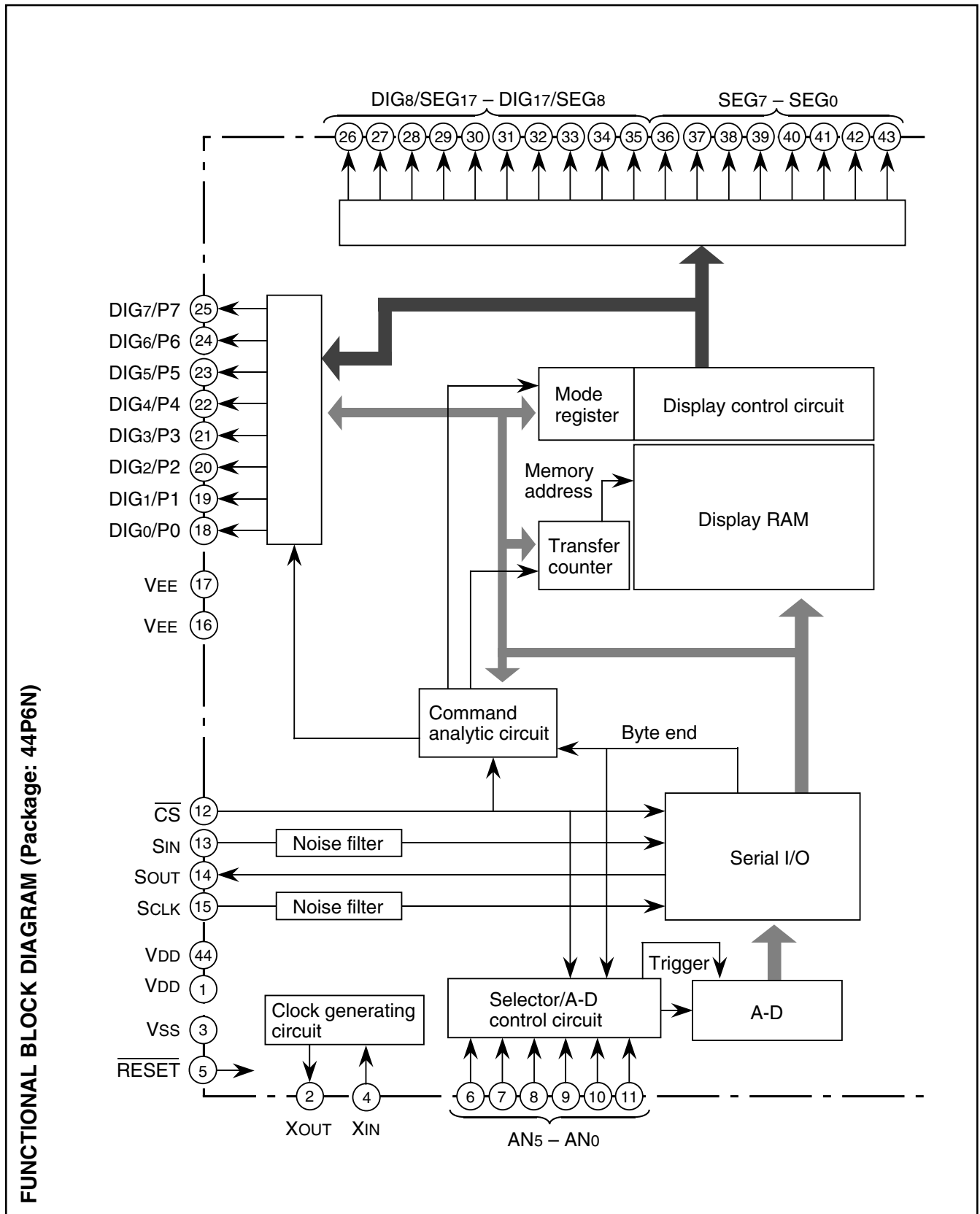


Fig. 2. Functional block diagram

PIN DESCRIPTION

Table. 1. Pin description

Pin	Name	Input	Output	Function
VCC, VSS	Power source			• Apply voltage of 5 V to VCC, and 0 V to VSS.
VEE	Pull-down power source			• Applies voltage supplied to pull-down resistors.
XIN	Clock input	Input		• CR oscillator pins for system clock.
XOUT	Clock output		Output	
RESET	RESET input	CMOS input		• Reset input pin for active "L". • Internal pull-up resistors connected between the $\overline{\text{RESET}}$ and VCC pins.
CS	Chip select	CMOS input		• Serial transfer is possible by inputting "L" signal.
SCLK	Serial clock	CMOS input Noise filter		• Clock for serial transfer is input. • Read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
SOUT	Serial output		N-channel open-drain	• Serial data is output. • During reset it is in high-impedance state.
SIN	Serial input	CMOS input Noise filter		• Serial data is input. • Read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
DIG0/P0 – DIG7/P7	Digit/Port		P-channel open-drain	• Pin for ordinary output or digit output. • At reset this port is set to VEE level through a pull-down resistor.
DIG8/SEG17 – DIG17/SEG8	Digit/Segment		P-channel open-drain	• Pin for digit output or segment output. • At reset this port is set to VEE level through a pull-down resistor.
SEG0 – SEG7	Segment		P-channel open-drain	• Pin for segment output. • At reset this port is set to VEE level through a pull-down resistor.

PORT BLOCK

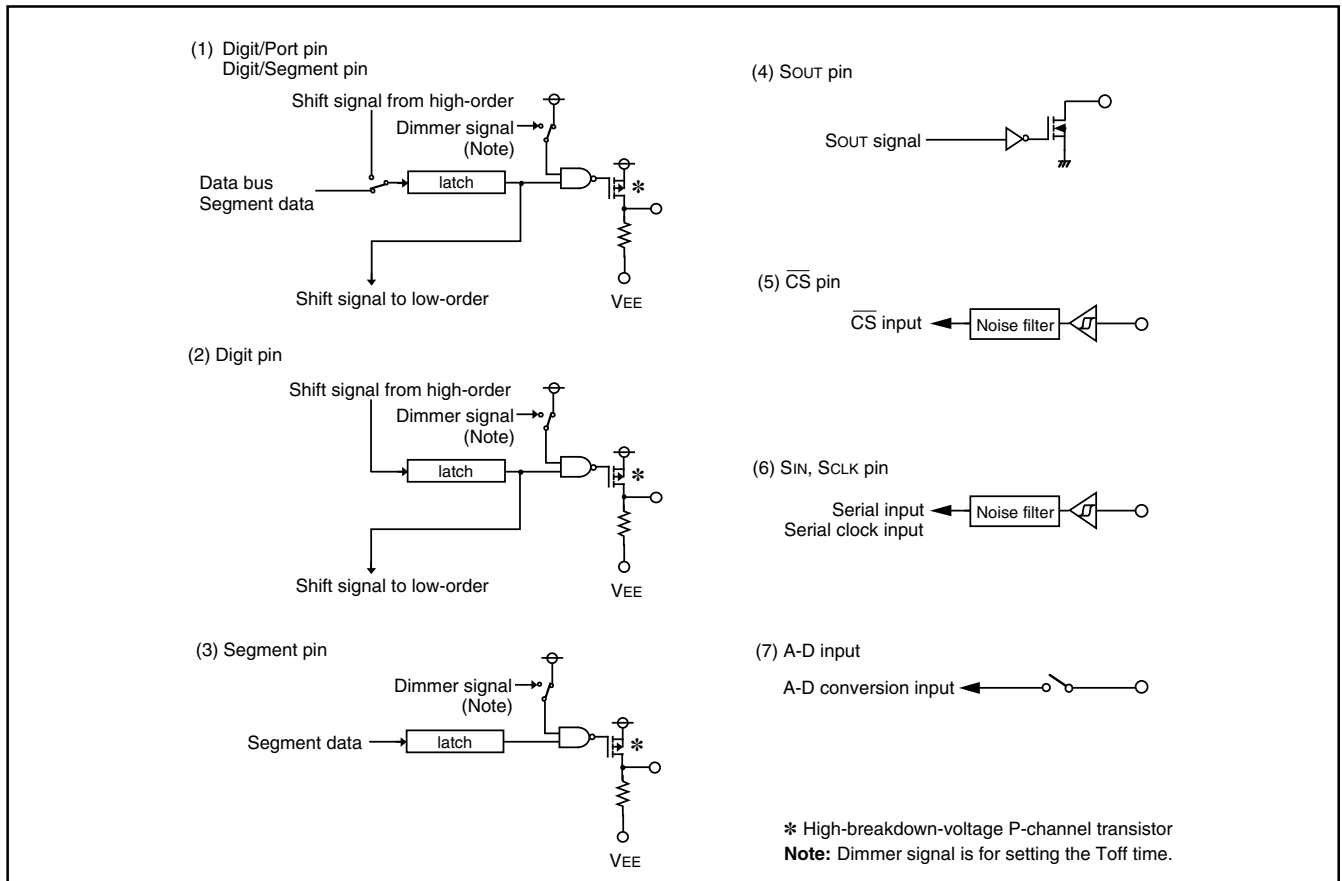


Fig. 3. Port block diagram

COMMAND STYLE

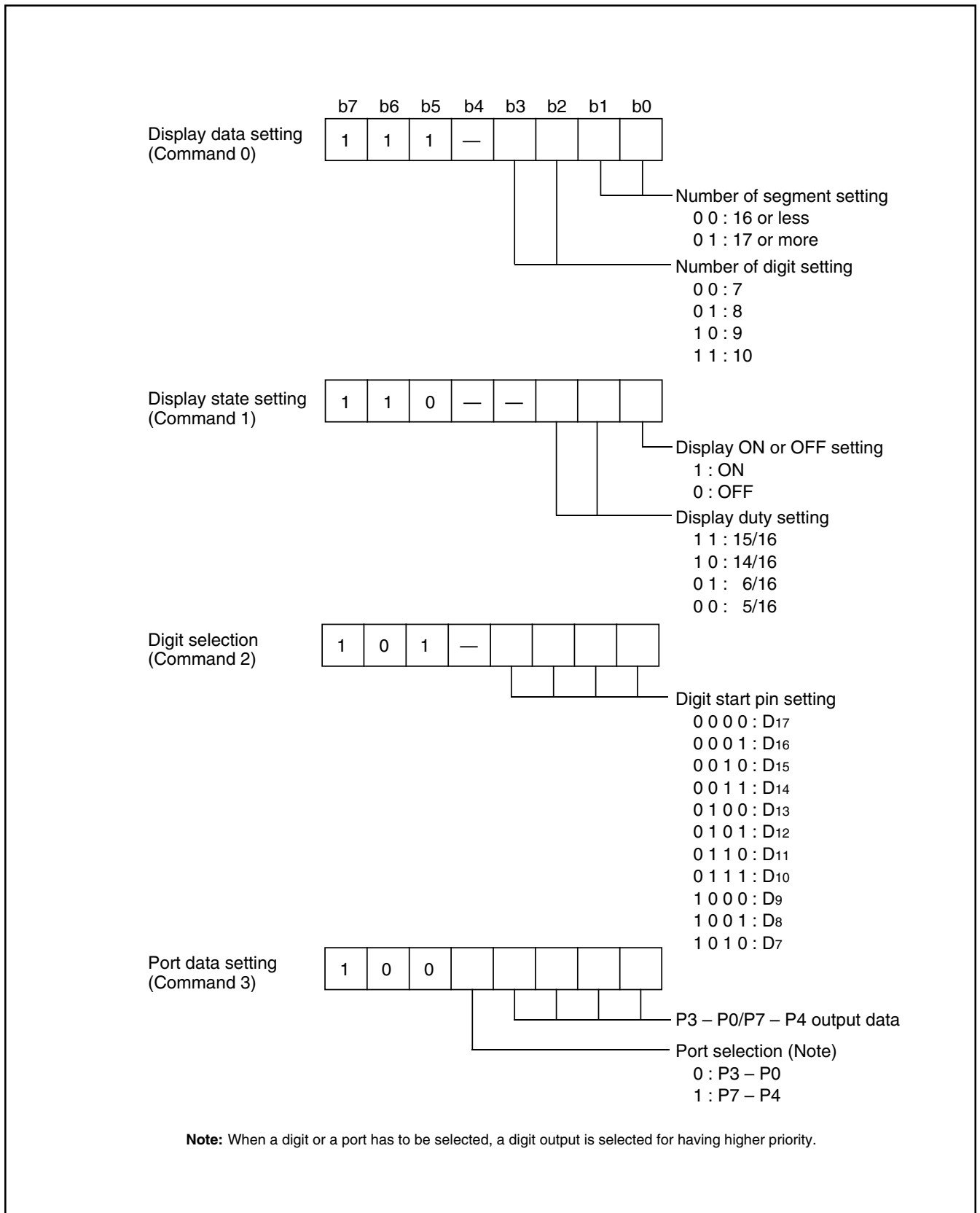


Fig. 4. Command style

SERIAL I/O PROTOCOL

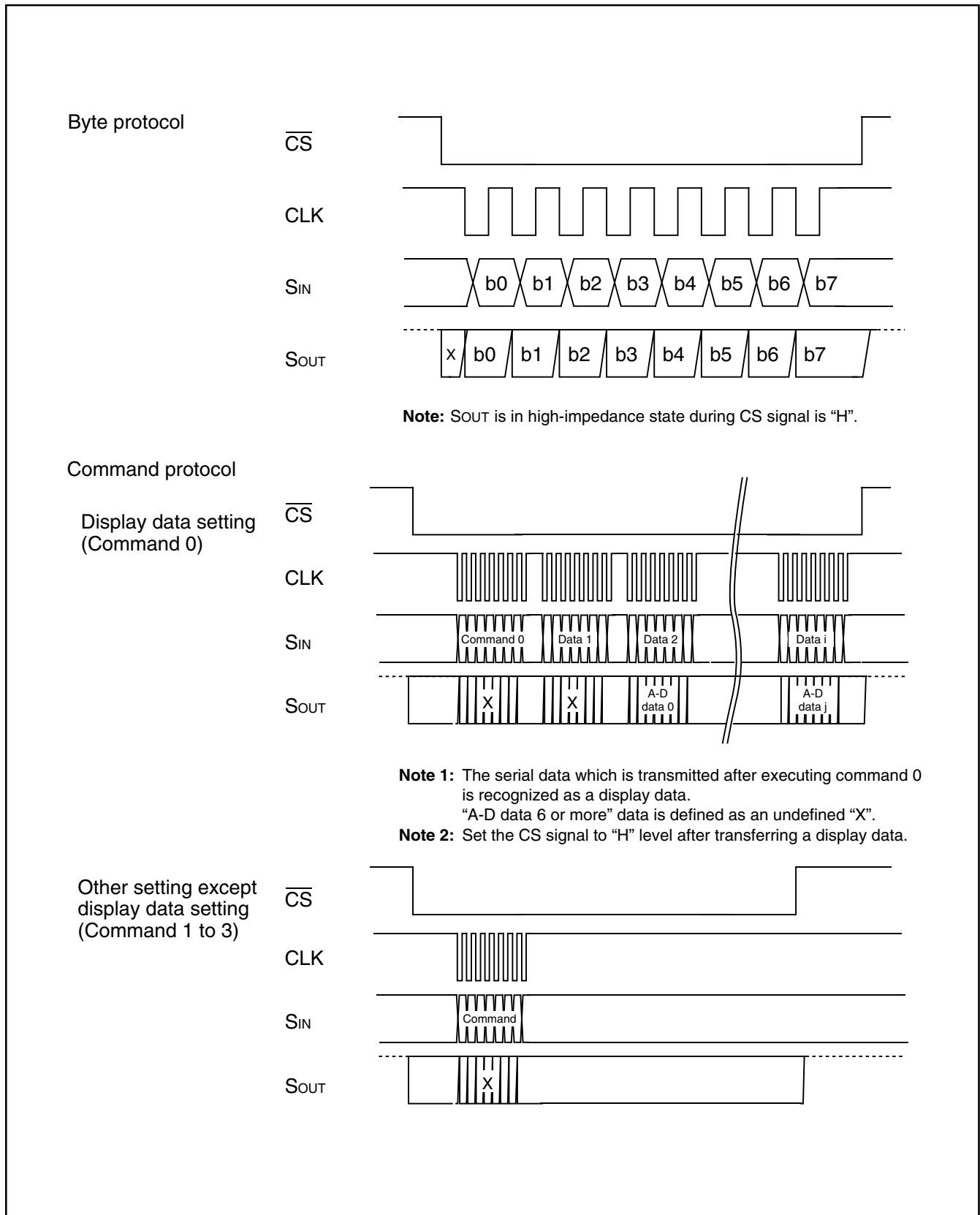


Fig. 5. Serial I/O protocol

SERIAL COMMUNICATION FORMAT (DISPLAY DATA, A-D OUTPUT)

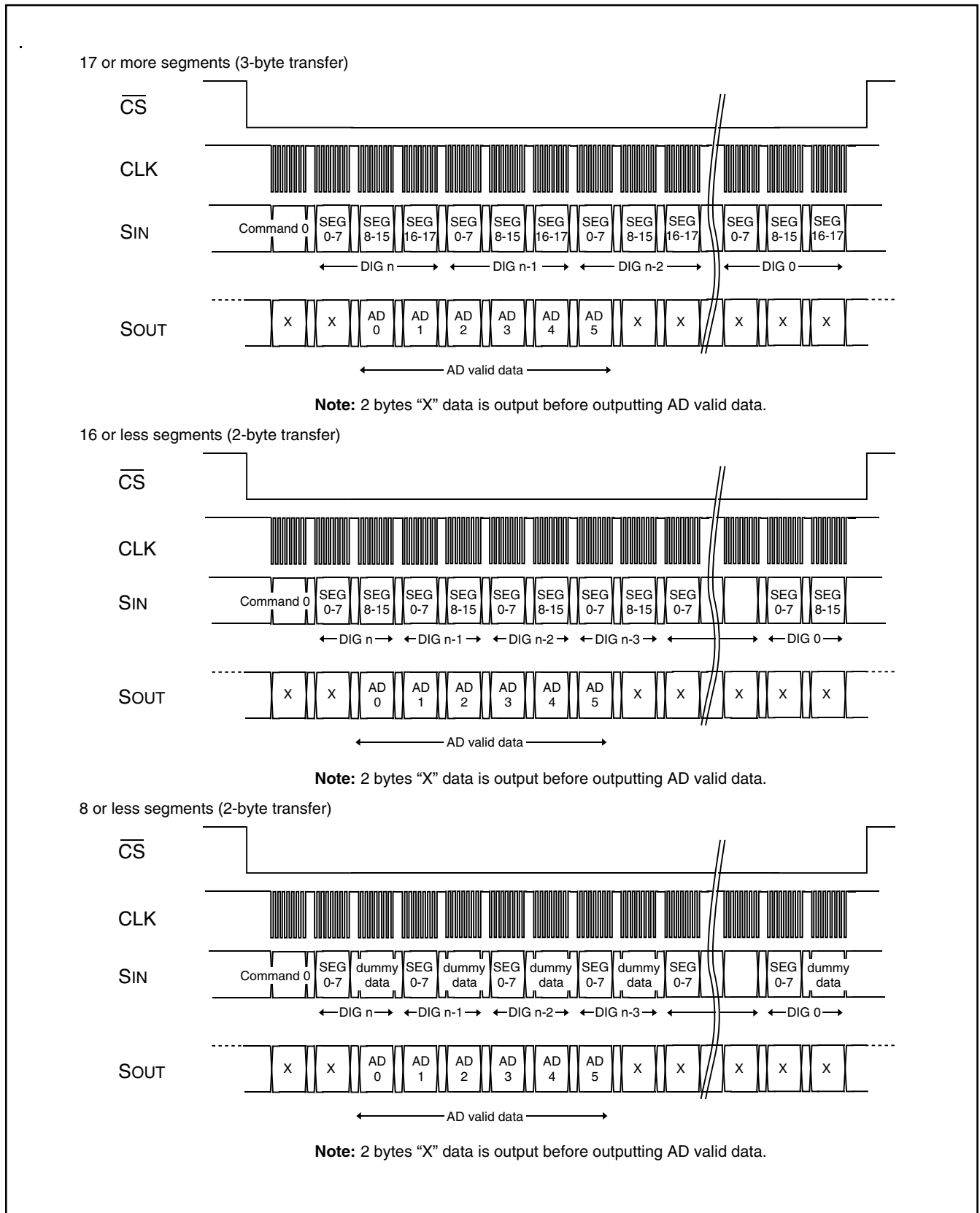


Fig. 6. Serial communication format

FLD DISPLAY TIMING

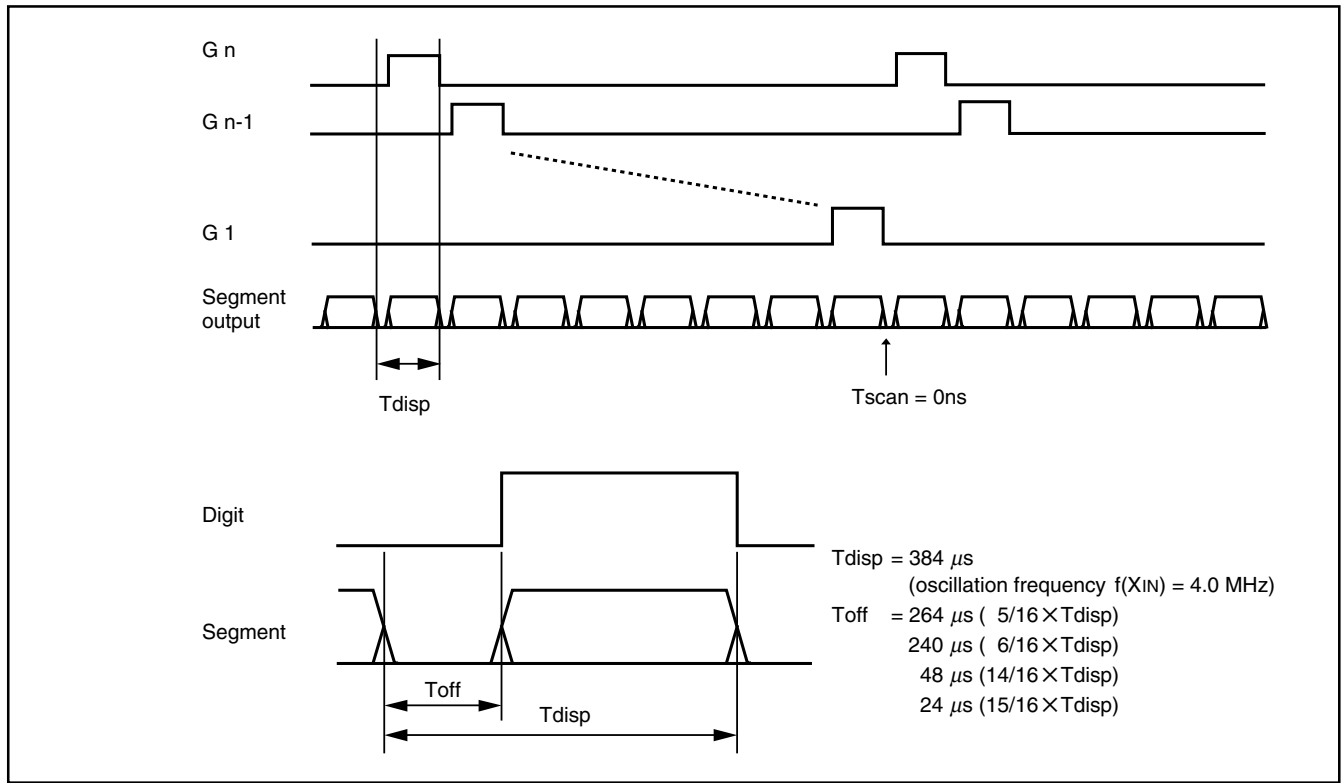


Fig. 7. FLD display timing diagram

SEGMENT/DIGIT SETTING EXAMPLE

	PORT	DIG	SEG	Grid : 7 Segment : 8	Grid : 10 Segment : 8	Grid : 10 Segment : 16	Grid : 7 Segment : 18
1			SEG0	S1	S1	S1	S1
2			SEG1	S2	S2	S2	S2
3			SEG2	S3	S3	S3	S3
4			SEG3	S4	S4	S4	S4
5			SEG4	S5	S5	S5	S5
6			SEG5	S6	S6	S6	S6
7			SEG6	S7	S7	S7	S7
8			SEG7	S8	S8	S8	S8
9		DIG17	SEG8	G7	G10	S9	S9
10		DIG16	SEG9	G6	G9	S10	S10
11		DIG15	SEG10	G5	G8	S11	S11
12		DIG14	SEG11	G4	G7	S12	S12
13		DIG13	SEG12	G3	G6	S13	S13
14		DIG12	SEG13	G2	G5	S14	S14
15		DIG11	SEG14	G1	G4	S15	S15
16		DIG10	SEG15		G3	S16	S16
17		DIG9	SEG16		G2	G10	S17
18		DIG8	SEG17		G1	G9	S18
19	P7	DIG7				G8	G7
20	P6	DIG6				G7	G6
21	P5	DIG5				G6	G5
22	P4	DIG4				G5	G4
23	P3	DIG3				G4	G3
24	P2	DIG2				G3	G2
25	P1	DIG1				G2	G1
26	P0	DIG0				G1	

Fig. 8. Segment/Digit setting example

BIT ALLOCATION FOR DISPLAY RAM

ADDRESS	b7				b0				
09 ₁₆							SEG 17	SEG 16	Digit0
0A ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
0B ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
0D ₁₆							SEG 17	SEG 16	Digit1
0E ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
0F ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
11 ₁₆							SEG 17	SEG 16	Digit2
12 ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
13 ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
15 ₁₆							SEG 17	SEG 16	Digit3
16 ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
17 ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
19 ₁₆							SEG 17	SEG 16	Digit4
1A ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
1B ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
1D ₁₆							SEG 17	SEG 16	Digit5
1E ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
1F ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
21 ₁₆							SEG 17	SEG 16	Digit6
22 ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
23 ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
25 ₁₆							SEG 17	SEG 16	Digit7
26 ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
27 ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
29 ₁₆							SEG 17	SEG 16	Digit8
2A ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
2B ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
2D ₁₆							SEG 17	SEG 16	Digit9
2E ₁₆	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
2F ₁₆	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	

Fig. 9. Bit allocation for display RAM

RESET CIRCUIT

To reset the controller, the $\overline{\text{RESET}}$ pin should be held at a "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 4.0 V and 5.5 V, and XIN oscillation is stable), reset is released.

Make sure that the reset input voltage is 0.5 V or less for 4.0 V of VCC.

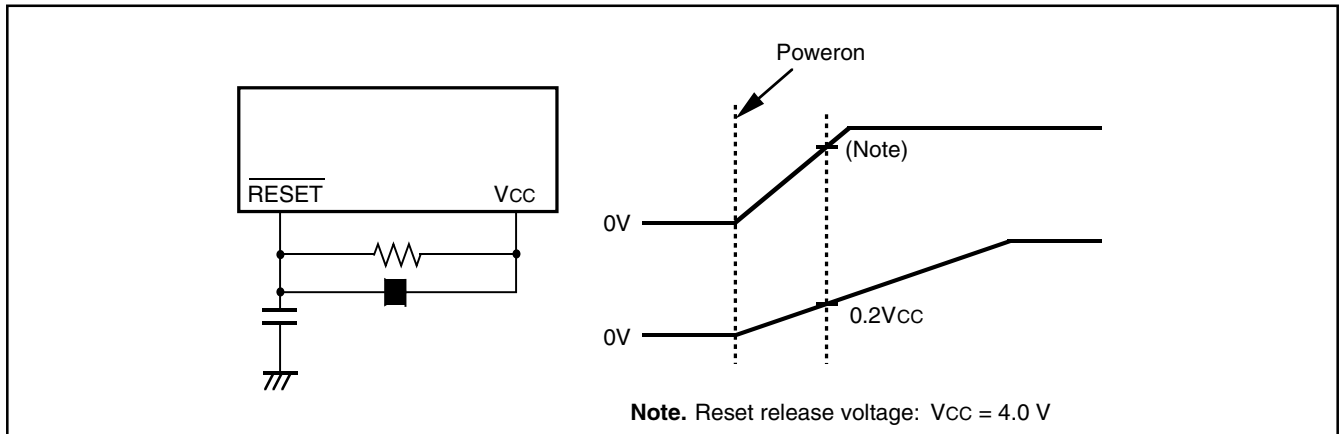


Fig. 10. Reset circuit example

CLOCK GENERATING CIRCUIT

Oscillating circuit is built up by connecting pins XIN and XOUT as short as possible and connecting a capacitor between pins XIN (XOUT) and VSS.

When supplying a clock externally, input it to XIN pin and leave XOUT pin open.

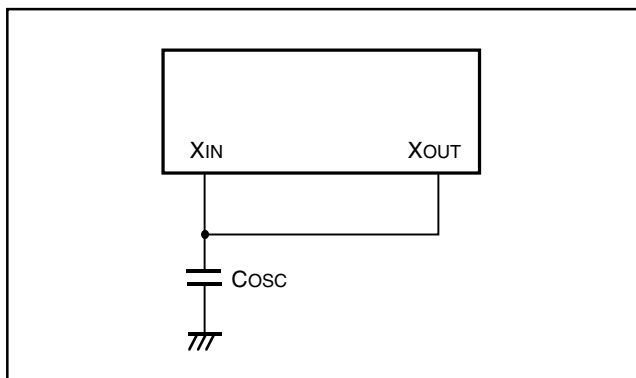


Fig. 11. CR generating circuit

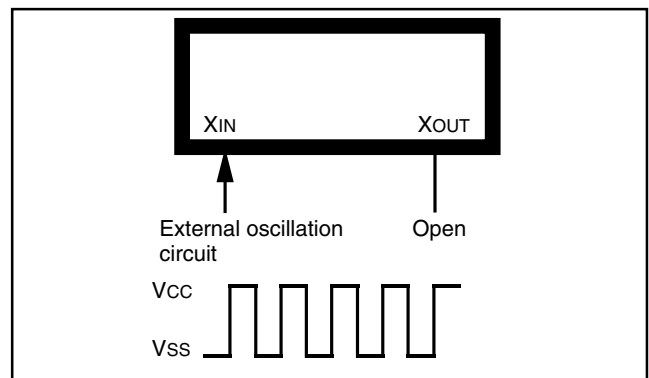


Fig. 12. External clock input circuit

HANDLING OF UNUSED PINS

Handle unused pins as the follow.

Table 2. Handling of unused pins

Pin	Handling
Segment	Open
Digit	Open
Analog input	Connect to VCC or VSS through a resistor.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage	<ul style="list-style-type: none"> • All voltage are based on Vss. • Output transistors are cut off. 	-0.3 to 7.0	V
VEE	Pull-down power source voltage		VCC-45 to VCC+0.3	V
Vi	Input voltage AN0 – AN5		-0.3 to VCC+0.3	V
Vi	Input voltage CS, SIN, SCLK		-0.3 to VCC+0.3	V
Vi	Input voltage RESET		-0.3 to VCC+0.3	V
Vo	Output voltage DIG0 – DIG17 SEG0 – SEG17		<ul style="list-style-type: none"> • All voltage are based on Vss. • Output transistors are cut off. • A waveform: 450 μs or more frequency and 30 μs or less pulse width. • Connect only capacitor load (CL = 200pF). 	VCC-45 to VCC+0.3
Vo	Output voltage SOUT	VCC-50 to VCC+0.3		
Pd	Power dissipation	Ta = 25 °C	600	mW
Topr	Operating temperature		-20 to 85	°C
Tstg	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (VCC = 4.0 to 5.5 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC	Power source voltage	4.0	5.0	5.5	V
VSS	Power source voltage		0		V
VEE	Pull-down power source voltage	VCC-38		VCC	V
VIH	"H" input voltage CS, SIN, SCLK	0.75VCC		VCC	V
VIH	"H" input voltage RESET	0.8VCC		VCC	V
VIL	"L" input voltage CS, SIN, SCLK	0		0.25VCC	V
VIL	"L" input voltage RESET	0		0.2VCC	V

RECOMMENDED OPERATING CONDITIONS (VCC = 4.0 to 5.5 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current DIG0 – DIG17, SEG0 – SEG17 (Note 1)			-240	mA
ΣIOH(avg)	"H" total peak output current DIG0 – DIG17, SEG0 – SEG17			-120	mA
IOH(peak)	"H" peak output current DIG0 – DIG17 (Note 2)			-40	mA
IOH(peak)	"H" peak output current SEG0 – SEG7 (Note 2)			-20	mA
IOL(peak)	"L" peak output current SOUT			10	mA
IOH(avg)	"H" peak output current DIG0 – DIG17 (Note 3)			-18	mA
IOH(avg)	"H" peak output current SEG0 – SEG7 (Note 3)			-7	mA
IOL(avg)	"L" peak output current SOUT			5.0	mA
f(XIN)	Main clock input oscillation frequency (Note 4)		4.0	5.2	MHz
f(SCLK)	Serial I/O external clock frequency		250		kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the oscillation frequency has a 50 % duty cycle.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VOH	“H” output voltage	DIG output	IOH = -18 mA	VCC-2.0			V
		SEG output	IOH = -7 mA	VCC-2.0			V
VOL	“L” output voltage	SOUT	IOH = 5 mA			2.0	V
VT+ — VT-	Hysteresis	SIN, SCLK, CS	VCC = 5.0 V		0.5		V
		RESET, XIN			0.5		V
IIH	“H” input voltage	SIN, SCLK, CS	VI = VCC			5.0	μA
		RESET				5.0	μA
		XIN			4.0		μA
IIL	“L” input voltage	SIN, SCLK, CS	VI = VSS			-5.0	μA
		RESET			-150		μA
		XIN			-4.0		μA
ILOAD	Output load current	DIG0 – DIG17 SEG0 – SEG17	VEE = VCC-36 V VOL = VCC Output transistors “off”	250	500	750	μA
I LEAK	Output leakage current	DIG0 – DIG17 SEG0 – SEG17	VEE = VCC-38 V VOL = VCC-38 V Output transistors “off”			-10	μA

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VRAM	RAM hold voltage		When clock is stopped	2.0		5.5	V
ICC	Power source current		VCC = 5 V, f(XIN) = 4.2 MHz Output transistors “off” at A-D converter operating		0.5	1.0	mA

A-D CONVERTER CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy (excluding quantization error)		VCC = 5.12 V			±3	LSB
Tconv	Conversion time					100	tc(XIN)
VIA	Analog input voltage			0		VCC	V
IIA	Analog port input current				0.5	5.0	μA
RLADDER	Ladder resistor				35		kΩ

TIMING REQUIREMENTS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(RESET)}$	Reset input "L" pulse width	2			μs
$t_c(XIN)$	Main clock input cycle time (XIN input)	238			ns
$t_{wH}(XIN)$	Main clock input "H" pulse width	60			ns
$t_{wL}(XIN)$	Main clock input "L" pulse width	60			ns
$t_c(SCLK)$	Serial clock input cycle time (Note)	4			CLKs
$t_{wH}(SCLK)$	Serial clock input "H" pulse width (Note)	2			CLKs
$t_{wL}(SCLK)$	Serial clock input "L" pulse width (Note)	2			CLKs
$t_{su}(SIN-SCLK)$	Serial input setup time (Note)	2			CLKs
$t_h(SCLK-SIN)$	Serial input hold time (Note)	3			CLKs
$t_{su}(\overline{CS})$	Serial input setup time	$50 t_c(XIN)$			ns
$t_h(\overline{CS})$	Serial input hold time	$50 t_c(XIN)$			ns
$t_{re}(SCLK)$	Serial clock interval time	$50 t_c(XIN)$			ns

Note: The unit means a number of noise filter sampling clock ($2 \times t_c(XIN)$).

SWITCHING CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_d(SCLK-SOUT)$	Serial I/O output delay time (Note 1)				3	CLKs
$t_v(SCLK-SOUT)$	Serial I/O output valid time		0			ns
$t_r(Pch)$	High-breakdown-voltage P-channel open-drain output rising time	$CL = 100pF$ $V_{EE} = V_{CC} - 36 V$		1.8		μs
COSC	External capacitor size (Note 2)			22		pF

Note 1: The unit means a number of noise filter sampling clock ($2 \times t_c(XIN)$).

2: An external capacitor size varies with a mounted condition.

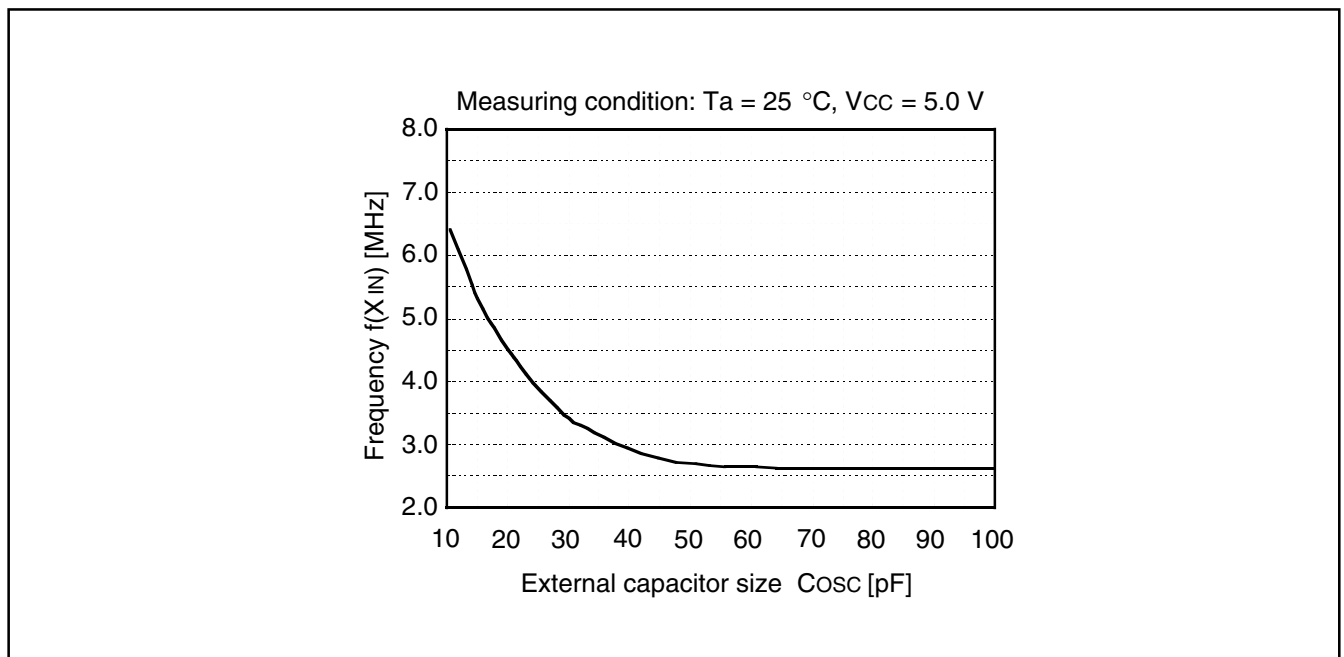


Fig. 13. Standard characteristic example of $f(XIN) - C_{osc}$

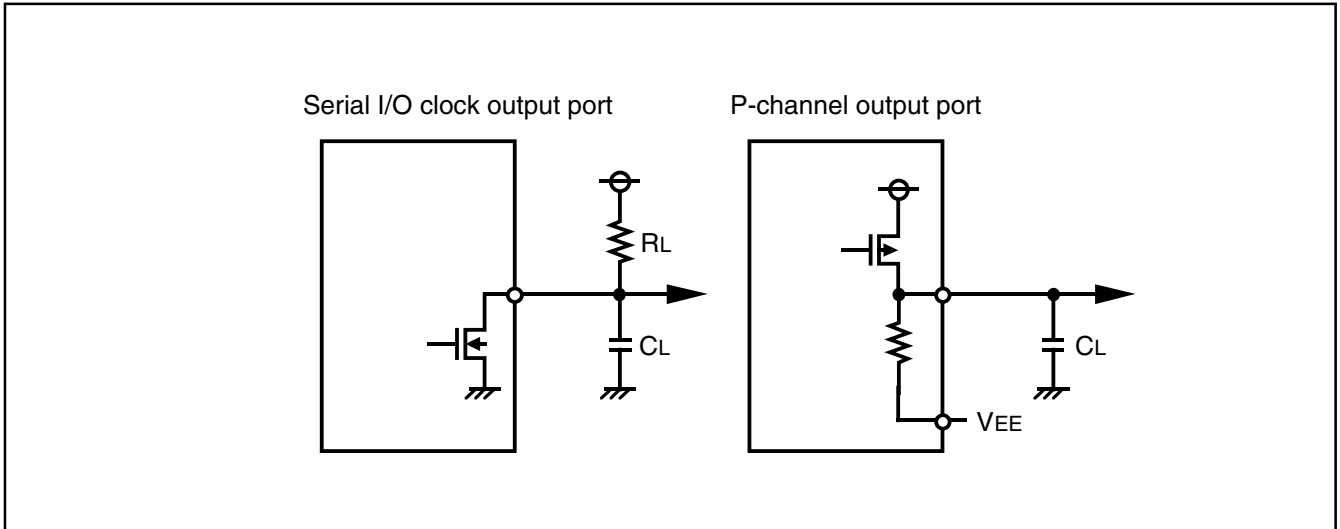


Fig. 14. Output switching characteristics measurement circuit diagram

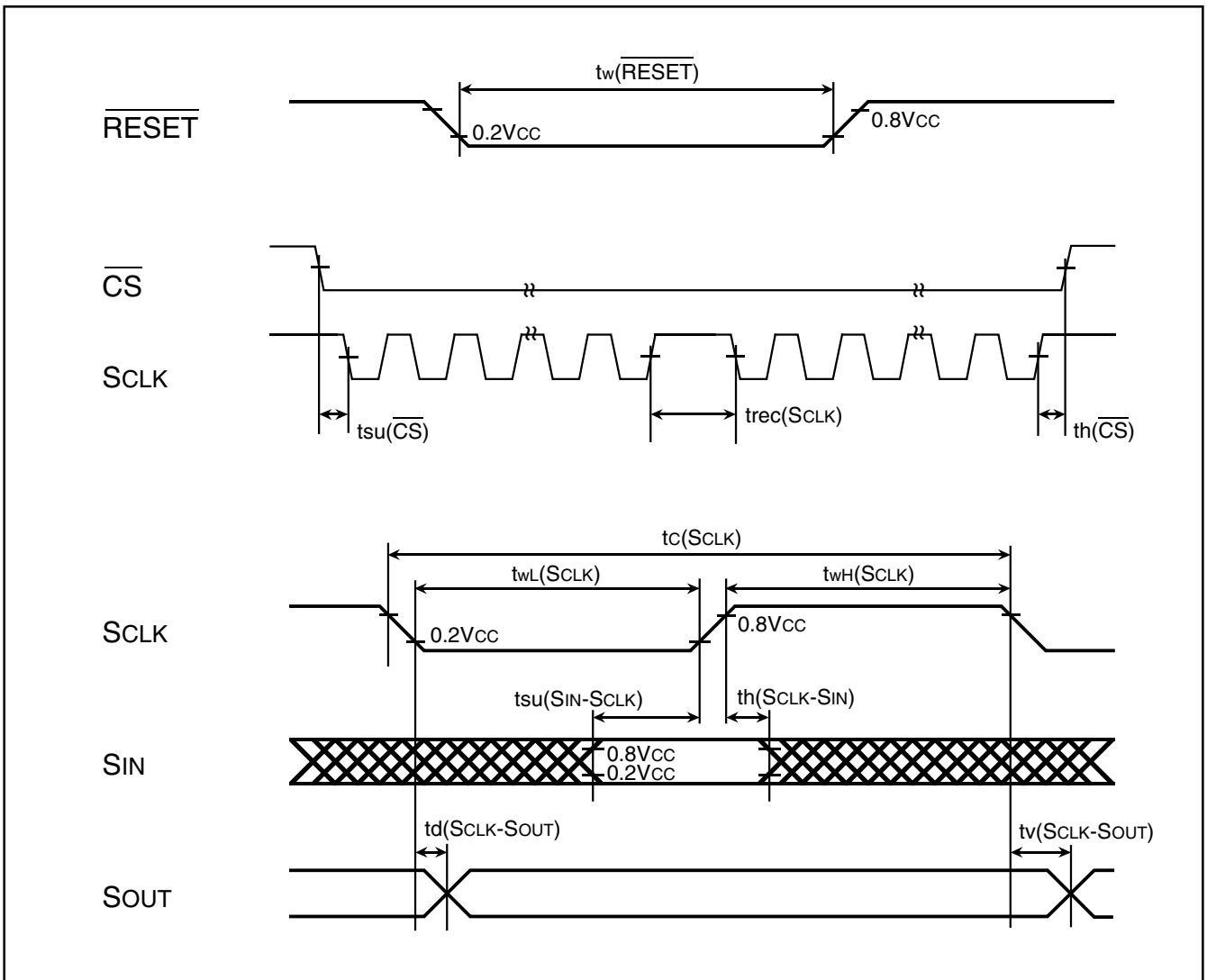


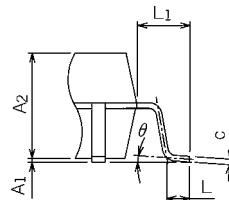
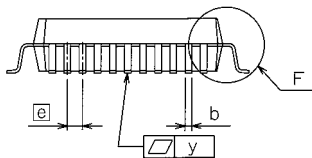
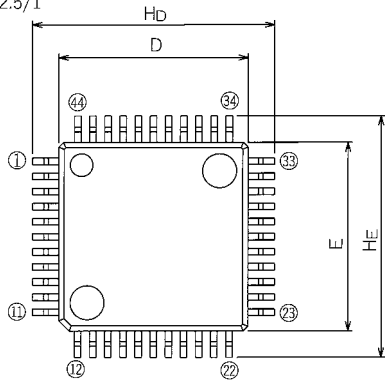
Fig. 15. Timing diagram

44P6N-A

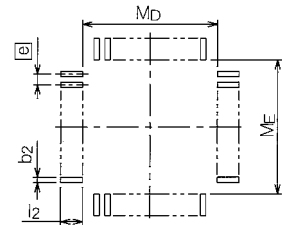
Plastic 44pin 10×10mm body QFP

EIAJ Package Code	JEDEC Code	Weight (g)	Lead Material
QFP44-P-1010-0.80	—	0.59	Alloy 42

Scale : 2.5/1



Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A ₁	0	0.1	0.2
A ₂	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	9.8	10.0	10.2
E	9.8	10.0	10.2
e	—	0.8	—
H _D	12.5	12.8	13.1
H _E	12.5	12.8	13.1
L	0.4	0.6	0.8
L ₁	—	1.4	—
y	—	—	0.1
θ	0°	—	10°
b ₂	—	0.5	—
l ₂	1.3	—	—
M _D	—	10.6	—
M _E	—	10.6	—

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI LINEAR IC's
M35500AFP/AGP

FLD CONTROLLER

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M35500AFP/AGP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	971115