

# 9-Mbit (256K × 36) Flow-Through SRAM

### **Features**

- Supports 133 MHz bus operations
- 256K × 36 common I/O
- 3.3 V 5% and +10% core power supply (V<sub>DD</sub>)
- 2.5 V or 3.3 V I/O power supply (V<sub>DDO</sub>)
- Fast clock-to-output times
  □ 6.5 ns (133-MHz version)
- Provide high performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel<sup>®</sup> Pentium<sup>®</sup> interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package
- "ZZ" sleep mode option

### **Functional Description**

The CY7C1361KVE33 is a 3.3 V, 256K × 36 synchronous flow-through SRAMs, respectively designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ( $\overline{\text{CE}}_1$ ), depth-expansion chip enables ( $\overline{\text{CE}}_2$  and  $\overline{\text{CE}}_3$ ), burst control inputs (ADSC, ADSP, and ADV), write enables ( $\overline{\text{BW}}_x$ , and  $\overline{\text{BWE}}$ ), and global write ( $\overline{\text{GW}}$ ). Asynchronous inputs include the output enable ( $\overline{\text{OE}}$ ) and the ZZ pin.

The CY7C1361KVE33 enables either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs. Address advancement is controlled by the address advancement (ADV) input.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor (ADSP) or address strobe controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin (ADV).

The CY7C1361KVE33 operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

For a complete list of related documentation, click here.

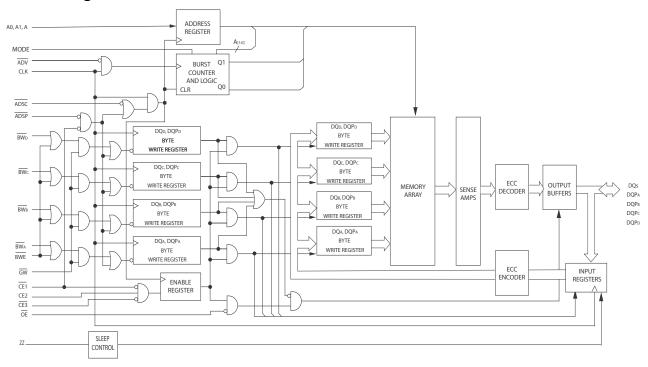
### **Selection Guide**

Description	133 MHz	Unit
Maximum access time	6.5	ns
Maximum operating current	149	mA

**Cypress Semiconductor Corporation**Document Number: 002-12709 Rev. \*A



## Logic Block Diagram - CY7C1361KVE33





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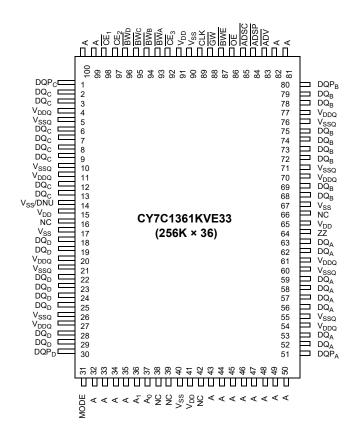
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## **Pin Configurations**

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout





## **Pin Definitions**

Synchronous   If ADSP or ADSC is active LOW, and CE₁ cE₂, and CE₃ are sampled active. A(1.0) feed the 2-bit cour	Name	I/O	Description
BWc,BWo         synchronous on the rising edge of CLK.           GW         Input-synchronous         Gobal write enable input, active LOW. When asserted LOW on the rising edge of CLK, a global write conducted (all bytes are written, regardless of the values on BW <sub>X</sub> and BWE).           CLK         Input-clock         Clock input. Used to capture all synchronous inputs to the device. Also used to increment the brown of the content when ADV is asserted LOW, during a burst operation.           CE1         Input-synchronous         Chip enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with 0 synchronous and CE3 to select/deselect the device. ADSP is ignored if CE₁ is HIGH. CE₁ is sampled only when a new external address is loaded.           CE2         Input-synchronous         Chip enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with 0 synchronous and CE3 to select/deselect the device. CE₂ is sampled only when a new external address is loaded.           OE         Input-asynchronous         Chip enable 3 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with 0 synchronous during the first clock of a read cycle LOW. Controls the direction the I/O pins when a new external address is loaded on the I/O pins abeta during the first clock of a read cycle when emerging from a deselected state.           ADV         Input-synchronous         Advance input signal, sampled on the rising edge of CLK. When asserted, it automatic increments the address register of a read cycle when emerging from a deselected state.           ADSP         Input-synchronous         Address strobe from controller, samp	A <sub>0</sub> , A <sub>1</sub> , A		$A\underline{ddres}$ s in $\underline{puts}$ used to select one $\underline{of}$ the address locations. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$ , $\overline{CE}_2$ , and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
Synchronous onducted (all bytes are written, regardless of the values on BW <sub>X</sub> and BWE).  CLK Input- clock Clock input. Used to capture all synchronous inputs to the device. Also used to increment the bit counter when ADV is asserted LOW, during a burst operation.  CE1 Input- synchronous and CE2 to select/deselect the device. ADSP is ignored if CE1 is HIGH. CE1 is sampled only when a we external address is loaded.  CE2 Input- synchronous and CE3 to select/deselect the device. ADSP is ignored if CE1 is HIGH. CE1 is sampled only when a new external address is loaded.  CE3 Input- synchronous and CE3 to select/deselect the device. CE3 is sampled only when a new external address is loaded.  Chip enable 3 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with C and CE2 to select/deselect the device. CE3 is sampled only when a new external address is loaded and CE3 to select/deselect the device. CE3 is sampled only when a new external address is loaded and CE3 to select/deselect the device. CE3 is sampled only when a new external address is loaded on the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data p OE6 is masked during the first clock of a read cycle when emerging from a deselected state.  ADDV Input- synchronous and CE3 to select/deselect the device are captured in the address registers. Aq1,0] are also load into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDI ginored when CE1 is deasserted HIGH.  ADSC Input- Address strobe from controller, sampled on the rising edge of CLK, active LOW. When asset to the device are captured in the address registers. Aq1,0] are also load into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.  BWE Input- synchronous Byte write enable input, active HIGH. When asserted HIGH places the device in a non-time-critical "sleep" input, active HIGH. When asserted HIGH places the device in a non-time-critical "sleep" input, active HIGH. Sampled on the	BW <sub>A</sub> ,BW <sub>B</sub> , BW <sub>C</sub> ,BW <sub>D</sub>		<b>Byte write select inputs, active LOW</b> . Qualified with BWE to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
CE_1	GW		<b>Global write enable input, active LOW</b> . When asserted LOW on the <u>rising</u> edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $BW_X$ and $BWE$ ).
synchronous and CE <sub>3</sub> to select/deselect the device. ADSP is ignored if CE <sub>1</sub> is HIGH. CE <sub>1</sub> is sampled only when ew external address is loaded.  CE <sub>2</sub> Input-synchronous and CE <sub>5</sub> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded and CE <sub>5</sub> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded and CE <sub>5</sub> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded and CE <sub>5</sub> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded companies to the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pode is masked during the first clock of a read cycle when emerging from a deselected state.  ADSP Input-synchronous increments the address in a burst cycle.  ADSP Input-synchronous increments the address in a burst cycle.  ADSP Input-synchronous increments the address in a burst cycle.  ADSC Input-synchronous increments the address strobe from processor, sampled on the rising edge of CLK, active LOW. When asset to the device are captured in the address registers. A <sub>11:01</sub> are also loar into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDI ignored when CE <sub>1</sub> is deasserted HIGH.  ADSC Input-synchronous CDW, addresses presented to the device are captured in the address registers. A <sub>11:01</sub> are also loar into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDI ignored when CE <sub>1</sub> is deasserted to the device are captured in the address registers. A <sub>11:01</sub> are also loar into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. Byte write enable input, active LOW. Sampled on the rising edge of CLK, active LOW. When asset synchronous into the burst counter when ADSP and ADSC are both asserted, only ADSP is recognized. COW to refet floating, pin has an internal pull down.  DQs I/O-synchronous device and the process of the capture and the process o	CLK		<b>Clock input</b> . <u>Used</u> to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
Synchronous and CE <sub>3</sub> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded SE <sub>3</sub> in Input-synchronous Chip enable 3 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with Combination of the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data processor. ADV Input-synchronous CE is assked during the first clock of a read cycle when emerging from a deselected state.  ADV Input-synchronous Input-synchronous input, active LOW. Controls the direction of the I/O pins. When LO are applied on the rising edge of CLK. When asserted, it automatic increments the address in a burst cycle.  ADSP Input-synchronous In	CE <sub>1</sub>		Chip enable 1 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $CE_3$ to select/deselect the device. ADSP is ignored if $CE_1$ is HIGH. $CE_1$ is sampled only when a new external address is loaded.
Synchronous	CE <sub>2</sub>		Chip enable 2 input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_3$ to select/deselect the device. $\overline{\text{CE}}_2$ is sampled only when a new external address is loaded.
asynchronous be located by the location of the	CE <sub>3</sub>		Chip enable 3 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\text{CE}_2$ to select/deselect the device. $\overline{\text{CE}}_3$ is sampled only when a new external address is loaded.
Synchronous   Increments the address in a burst cycle.	ŌĒ		Output enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
Synchronous LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also load into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDI ignored when CE₁ is deasserted HIGH.  Address strobe from controller, sampled on the rising edge of CLK, active LOW. When asser LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also load into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.  BWE Input-synchronous LOW to conduct a byte write.  ZZ Input-asynchronous LOW to conduct a byte write.  ZZ "sleep" input, active HIGH. When asserted HIGH places the device in a non-time-critical "slee asynchronous condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. pin has an internal pull down.  DQ₂ I/O-synchronous Bidirectional data I/O lines. As inputs, they feed into an on-chip data register that is triggered by rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by addresses presented during the previous clock rise of the read cycle. The direction of the pins controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ₂ and DC are placed in a tristate condition. The outputs are automatically tristated during the data portion of a wasquence, during the first clock when emerging from a deselected state, and when the device deselected, regardless of the state of OE.  DQP <sub>X</sub> I/O-synchronous Bidirectional data parity I/O lines. Functionally, these signals are identical to DQ₂. During wasquences, DQP <sub>X</sub> is controlled by BW <sub>X</sub> correspondingly.  MODE Input-static selects burst order. When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left float selects interleaved burst sequence. This is a strap pin and should remain static during device operate Mode Pin has an internal pull-up.  VDD Power supply Power supply inputs to the core of the device.	ADV		Advance input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
synchronous LOW, addresses presented to the device are captured in the address registers. A[1:0] are also load into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.  BWE Input-synchronous Byte write enable input, active LOW. Sampled on the rising edge of CLK. This signal must be asser LOW to conduct a byte write.  ZZ "sleep" input, active HIGH. When asserted HIGH places the device in a non-time-critical "sle condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. pin has an internal pull down.  Bidirectional data I/O lines. As inputs, they feed into an on-chip data register that is triggered by rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by addresses presented during the previous clock rise of the read cycle. The direction of the pin controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>8</sub> and DC are placed in a tristate condition. The outputs are automatically tristated during the data portion of a w sequence, during the first clock when emerging from a deselected state, and when the device deselected, regardless of the state of OE.  DQP <sub>X</sub> I/O-synchronous Bidirectional data parity I/O lines. Functionally, these signals are identical to DQ <sub>8</sub> . During w sequences, DQP <sub>X</sub> is controlled by BW <sub>X</sub> correspondingly.  MODE Input-static Selects burst order. When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left float selects interleaved burst sequence. This is a strap pin and should remain static during device operation Mode Pin has an internal pull-up.  Power supply Power supply inputs to the core of the device.  Power supply for the I/O circuitry.	ADSP		Address strobe from processor, sampled on the rising edge of CLK, active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
Synchronous   LÓW to conduct a byte write.	ADSC		Address strobe from controller, sampled on the rising edge of CLK, active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
asynchronous condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. pin has an internal pull down.  DQs  I/O-synchronous  Bidirectional data I/O lines. As inputs, they feed into an on-chip data register that is triggered by rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by addresses presented during the previous clock rise of the read cycle. The direction of the pins controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and DC are placed in a tristate condition. The outputs are automatically tristated during the data portion of a was equence, during the first clock when emerging from a deselected state, and when the device deselected, regardless of the state of OE.  DQPX  I/O-synchronous  Bidirectional data parity I/O lines. Functionally, these signals are identical to DQs. During was sequences, DQPx is controlled by BWx correspondingly.  MODE  Input-static  Selects burst order. When tied to GND selects linear burst sequence. When tied to VDD or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation Mode Pin has an internal pull-up.  VDD  Power supply  Power supply inputs to the core of the device.  Power supply for the I/O circuitry.	BWE		<b>Byte write enable input, active LOW</b> . Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by addresses presented during the previous clock rise of the read cycle. The direction of the pins controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and DC are placed in a tristate condition. The outputs are automatically tristated during the data portion of a was sequence, during the first clock when emerging from a deselected state, and when the device deselected, regardless of the state of OE.  DQP <sub>X</sub> I/O-  synchronous  Bidirectional data parity I/O lines. Functionally, these signals are identical to DQs. During was sequences, DQP <sub>X</sub> is controlled by BW <sub>X</sub> correspondingly.  MODE  Input-  static  Selects burst order. When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left float selects interleaved burst sequence. This is a strap pin and should remain static during device operation Mode Pin has an internal pull-up.  VDD  Power supply  Power supply inputs to the core of the device.  Power supply for the I/O circuitry.	ZZ		
synchronous sequences, DQP <sub>X</sub> is controlled by $\overline{BW}_X$ correspondingly.  MODE  Input- static  Selects burst order. When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left float selects interleaved burst sequence. This is a strap pin and should remain static during device operation Mode Pin has an internal pull-up.  V <sub>DD</sub> Power supply  Power supply inputs to the core of the device.  Power supply  Power supply for the I/O circuitry.	DQ <sub>s</sub>		<b>Bidirectional data I/O lines</b> . As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, $\overline{DQ_s}$ and $\overline{DQP_X}$ are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$ .
static selects interleaved burst sequence. This is a strap pin and should remain static during device operation Mode Pin has an internal pull-up.  VDD Power supply Power supply inputs to the core of the device.  VDDQ I/O power supply Power supply for the I/O circuitry.	DQP <sub>X</sub>		<b>Bidirectional data parity I/O lines.</b> Functionally, these signals are identical to $DQ_s$ . During write sequences, $DQP_X$ is controlled by $\overline{BW}_X$ correspondingly.
V <sub>DDQ</sub> I/O power supply for the I/O circuitry.	MODE		<b>Selects burst order</b> . When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
supply	$V_{DD}$	Power supply	Power supply inputs to the core of the device.
V <sub>SS</sub> Ground Ground for the core of the device.	$V_{DDQ}$		Power supply for the I/O circuitry.
	V <sub>SS</sub>	Ground	Ground for the core of the device.

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### Pin Definitions (continued)

Name	I/O	Description
$V_{SSQ}$	I/O ground	Ground for the I/O circuitry.
NC		<b>No connects</b> . Not internally connected to the die. 18M, 36M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.
V <sub>SS</sub> /DNU	Ground/DNU	This pin can be connected to ground or should be left floating.

### **Functional Overview**

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CDV}$ ) is 6.5 ns (133 MHz device).

The CY7C1361KVE33 supports secondary cache in systems using either a linear or interleaved burst sequence. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable  $(\underline{BWE})$  and byte write select  $(BW_X)$  inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects  $(\overline{CE}_1, CE_2, \overline{CE}_3)$  and an asynchronous output enable  $(\overline{OE})$  provide for easy bank selection and output tristate control. ADSP is ignored if  $\overline{CE}_1$  is HIGH.

### Single Read Accesses

A single read access is initiated when the <u>following</u> conditions are satisfied at <u>clock</u> rise: (1)  $\overline{CE_1}$ ,  $\overline{CE_2}$ , and  $\overline{CE_3}$  are all asserted active and (2)  $\overline{ADSP}$  or  $\overline{ADSC}$  is asserted LOW (if the access is initiated by  $\overline{ADSC}$ , the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the  $\overline{OE}$  input is asserted LOW, the requested data will be available at the data outputs a maximum to  $t_{\overline{CDV}}$  after clock rise.  $\overline{ADSP}$  is ignored if  $\overline{CE_1}$  is HIGH.

### Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE_1}$ ,  $\overline{CE_2}$ ,  $\overline{CE_3}$  are all asserted active and (2)  $\overline{ADSP}$  is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW_X}$ ) are ignored during this first clock cycle. If the write inputs are asserted active (see Partial Truth Table for Read/Write on page 9 for appropriate states that indicate a write) on the next

clock rise, the appropriate data will be latched and written into the device. Byte writes are allowed. All I/Os are tristated during a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQs. As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of OE.

## Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at <u>clock</u> rise: (1)  $\overline{CE_1}$ ,  $\overline{CE_2}$ , and  $\overline{CE_3}$  are all asserted active, (2)  $\overline{ADSC}$  is asserted LOW, (3)  $\overline{ADSP}$  is deasserted HIGH, and (4) the write input signals ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW_X}$ ) indicate a write access.  $\overline{ADSC}$  is ignored if  $\overline{ADSP}$  is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to  $\mathsf{DQ}_{[A:D]}$  is written into the specified address location. Byte writes are allowed. All I/Os are tristated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous  $\overline{\mathsf{OE}}$  input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to  $\mathsf{DQ}_s.$  As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of  $\overline{\mathsf{OE}}.$ 

### **Burst Sequences**

The CY7C1361KVE33 provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by A<sub>[1:0]</sub>, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

### **Interleaved Burst Address Table**

(MODE = Floating or  $V_{DD}$ )

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00



### **Linear Burst Address Table**

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

## Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation 'sleep' mode. Two clock cycles are required to enter into or exit from this 'sleep' mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the 'sleep' mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the 'sleep' mode.  $\overline{\text{CE}}_1,$   $\overline{\text{CE}}_2,$   $\overline{\text{CE}}_3,$  ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

### **ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions		Min	Max	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \ge V_{DD} - 0.2 \text{ V}$		-	65	mA
t <sub>ZZS</sub>	Device operation to ZZ	$ZZ \ge V_{DD} - 0.2 \text{ V}$		-	2t <sub>CYC</sub>	ns
t <sub>ZZREC</sub>	ZZ recovery time	ZZ ≤ 0.2 V		2t <sub>CYC</sub>	-	ns
$t_{ZZI}$	ZZ active to sleep current	This parameter is sampled		-	2t <sub>CYC</sub>	ns
t <sub>RZZI</sub>	ZZ Inactive to exit sleep current	This parameter is sampled		0	-	ns



## **Truth Table**

The Truth Table for CY7C1361KVE33 follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	CE <sub>1</sub>	CE <sub>2</sub>	CE <sub>3</sub>	ZZ	ADSP	ADSC	ADV	WRITE	OE	CLK	DQ
Deselected cycle, power-down	None	Н	Х	Х	L	Х	L	Х	Х	Х	L–H	Tri-state
Deselected cycle, power-down	None	L	L	Х	L	L	Х	Х	Х	Х	L–H	Tri-state
Deselected cycle, power-down	None	L	Х	Н	L	L	Х	Х	Х	Χ	L–H	Tri-state
Deselected cycle, power-down	None	L	L	Х	L	Н	L	Х	Х	Χ	L–H	Tri-state
Deselected cycle, power-down	None	Х	Х	Н	L	Н	L	Х	Х	Х	L–H	Tri-state
Sleep mode, power-down	None	Х	Х	Х	Н	Х	Х	Х	Х	Χ	Х	Tri-state
Read cycle, begin burst	External	L	Н	L	L	L	Х	Х	Х	L	L–H	Q
Read cycle, begin burst	External	L	Н	L	L	L	Х	Х	Х	Н	L–H	Tri-state
Write cycle, begin burst	External	L	Н	L	L	Н	L	Х	L	Χ	L–H	D
Read cycle, begin burst	External	L	Н	L	L	Н	L	Х	Н	L	L–H	Q
Read cycle, begin burst	External	L	Н	L	L	Н	L	Х	Н	Н	L–H	Tri-state
Read cycle, continue burst	Next	Х	Х	Х	L	Н	Н	L	Н	L	L–H	Q
Read cycle, continue burst	Next	Х	Х	Х	L	Н	Н	L	Н	Н	L–H	Tri-state
Read cycle, continue burst	Next	Н	Х	Х	L	Х	Н	L	Н	L	L–H	Q
Read cycle, continue burst	Next	Н	Х	Х	L	Х	Н	L	Н	Н	L–H	Tri-state
Write cycle, continue burst	Next	Х	Х	Х	L	Н	Н	L	L	Χ	L–H	D
Write cycle, continue burst	Next	Н	Х	Х	L	Х	Н	L	L	Χ	L–H	D
Read cycle, suspend burst	Current	Х	Х	Х	L	Н	Н	Н	Н	L	L–H	Q
Read cycle, suspend burst	Current	Х	Х	Х	L	Н	Н	Н	Н	Н	L–H	Tri-state
Read cycle, suspend burst	Current	Н	Х	Х	L	Х	Н	Н	Н	L	L–H	Q
Read cycle, suspend burst	Current	Н	Х	Х	L	Х	Н	Н	Н	Н	L–H	Tri-state
Write cycle, suspend burst	Current	Х	Х	Х	L	Н	Н	Н	L	Χ	L–H	D
Write cycle, suspend burst	Current	Н	Х	Х	L	Х	Н	Н	L	Χ	L–H	D

### Notes

- 1. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
  2. WRITE = L when any one or more byte write enable signals and BWE = L or GW = L. WRITE = H when all byte write enable signals, BWE, GW = H.
- The DQ pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not sampled with the clock.
   The SRAM always initiates a read cycle when ADSP is asserted, regardless of the state of GW, BWE, or BW<sub>X</sub>. Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result, OE must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. OE is a don't care for the remainder of the write cycle.
- 5.  $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked inte<u>rnally</u> during write cycles. During a read cycle all data bits are tri-state when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when  $\overline{OE}$  is active (LOW).



## **Partial Truth Table for Read/Write**

The Partial Truth Table for Read/Write for CY7C1361KVE33 follows. [6, 7]

Function (CY7C1361KVE33)	GW	BWE	BW <sub>D</sub>	BW <sub>C</sub>	BW <sub>B</sub>	BW <sub>A</sub>
Read	Н	Н	Х	Х	Х	Х
Read	Н	L	Н	Н	Н	Н
Write byte (A, DQP <sub>A</sub> )	Н	L	Н	Н	Н	L
Write byte (B, DQP <sub>B</sub> )	Н	L	Н	Н	L	Н
Write bytes (B, A, DQP <sub>A</sub> , DQP <sub>B</sub> )	Н	L	Н	Н	L	L
Write byte (C, DQP <sub>C</sub> )	Н	L	Н	L	Н	Н
Write bytes (C, A, DQP <sub>C</sub> , DQP <sub>A</sub> )	Н	L	Н	L	Н	L
Write bytes (C, B, DQP <sub>C</sub> , DQP <sub>B</sub> )	Н	L	Н	L	L	Н
Write bytes (C, B, A, DQP <sub>C</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	Н	L	Н	L	L	L
Write byte (D, DQP <sub>D</sub> )	Н	L	L	Н	Н	Н
Write bytes (D, A, DQP <sub>D</sub> , DQP <sub>A</sub> )	Н	L	L	Н	Н	L
Write bytes (D, B, DQP <sub>D</sub> , DQP <sub>A</sub> )	Н	L	L	Н	L	Н
Write bytes (D, B, A, DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	Н	L	L	Н	L	L
Write bytes (D, B, DQP <sub>D</sub> , DQP <sub>B</sub> )	Н	L	L	L	Н	Н
Write bytes (D, B, A, DQP <sub>D</sub> , DQP <sub>C</sub> , DQP <sub>A</sub> )	Н	L	L	L	Н	L
Write bytes (D, C, A, DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	Н	L	L	L	L	Н
Write all bytes	Н	L	L	L	L	L
Write all bytes	L	Х	Х	Х	Х	Х

<sup>6.</sup> X = "Don't Care." H = Logic HIGH, L = Logic LOW.
7. Table only lists a partial listing of the byte write combinations. Any Combination of BW<sub>X</sub> is valid Appropriate write will be done based on which byte write is active.



## **Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature65 °C to + 150 °C
Ambient temperature with power applied
Supply voltage on $V_{DD}$ relative to GND–0.5 V to + 4.6 V
Supply voltage on $\rm V_{DDQ}$ relative to GND –0.5 V to + $\rm V_{DD}$
DC voltage applied to outputs in tri-state–0.5 V to $V_{DDQ}$ + 0.5 V
DC input voltage $-0.5 \text{ V}$ to $\text{V}_{\text{DD}}$ + 0.5 V
Current into outputs (LOW)20 mA
Static discharge voltage (per MIL-STD-883, method 3015)
Latch-up current > 200 mA

## **Operating Range**

Range	Ambient Temperature	$V_{DD}$	$V_{\mathrm{DDQ}}$
Industrial	–40 °C to +85 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V <sub>DD</sub>

## **Neutron Soft Error Immunity**

Parameter	Description	Test Conditions	Тур	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	0	0.01	FIT/ Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single event latch up	85 °C	0	0.1	FIT/ Dev

<sup>\*</sup> No LMBU or SEL events occurred during testing, this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

## Electrical Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions	Min	Max	Unit
$V_{DD}$	Power supply voltage		3.135	3.6	V
$V_{DDQ}$	I/O supply voltage	for 3.3 V I/O	3.135	$V_{DD}$	V
		for 2.5 V I/O	2.375	2.625	V
V <sub>OH</sub>	Output HIGH voltage	for 3.3 V I/O, I <sub>OH</sub> = -4.0 mA	2.4	_	V
		for 2.5 V I/O, I <sub>OH</sub> = -1.0 mA	2.0	_	V
V <sub>OL</sub>	Output LOW voltage	for 3.3 V I/O, I <sub>OL</sub> = 8.0 mA	_	0.4	V
		for 2.5 V I/O, I <sub>OL</sub> = 1.0 mA	_	0.4	V
V <sub>IH</sub>	Input HIGH voltage <sup>[8]</sup>	for 3.3 V I/O	2.0	V <sub>DD</sub> + 0.3 V	V
		for 2.5 V I/O	1.7	V <sub>DD</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW voltage <sup>[8]</sup>	for 3.3 V I/O	-0.3	0.8	V
		for 2.5 V I/O	-0.3	0.7	V
I <sub>X</sub>	Input leakage current except ZZ and MODE	$GND \le V_I \le V_{DDQ}$	-5	5	μА
	Input current of MODE	Input = V <sub>SS</sub>	-30	-	μА
		Input = V <sub>DD</sub>	_	5	μА
	Input current of ZZ	Input = V <sub>SS</sub>	-5	_	μА
		Input = V <sub>DD</sub>	_	30	μА
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ,</sub> output disabled	-5	5	μА

<sup>8.</sup> Overshoot:  $V_{IH(AC)} < V_{DD} + 1.5 \text{ V}$  (Pulse width less than  $t_{CYC}/2$ ), undershoot:  $V_{IL(AC)} > -2 \text{ V}$  (Pulse width less than  $t_{CYC}/2$ ). 9.  $T_{Power-up}$ : Assumes a linear ramp from 0 V to  $V_{DD(min)}$  within 200 ms. During this time  $V_{IH} < V_{DD}$  and  $V_{DDQ} \le V_{DD}$ .



## **Electrical Characteristics** (continued)

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions	Test Conditions		Max	Unit
I <sub>DD</sub>	V <sub>DD</sub> operating supply current	$V_{DD}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = 1/ $t_{CYC}$	7.5 ns cycle, 133 MHz	_	149	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	$\begin{aligned} &\text{Max V}_{\text{DD}}, \text{ device deselected,} \\ &\text{V}_{\text{IN}} \geq \text{V}_{\text{IH}} \text{ or V}_{\text{IN}} \leq \text{V}_{\text{IL}}, \text{f = f}_{\text{MAX,}} \\ &\text{inputs switching} \end{aligned}$	7.5 ns cycle, 133 MHz	_	80	mA
I <sub>SB2</sub>	Automatic CE power-down current – CMOS inputs	$\begin{aligned} &\text{Max V}_{DD}, \text{ device deselected,} \\ &\text{V}_{IN} \geq \text{V}_{DD} - 0.3 \text{ V or V}_{IN} \leq 0.3 \text{ V,} \\ &\text{f} = 0, \text{ inputs static} \end{aligned}$	7.5 ns cycle, 133 MHz	-	70	mA
I <sub>SB3</sub>	Automatic CE power-down current – CMOS inputs	$\begin{aligned} &\text{Max V}_{DD}, \text{ device deselected,} \\ &\text{V}_{IN} \! \geq \! \text{V}_{DDQ} \! - \! 0.3  \text{V or V}_{IN} \! \leq \! 0.3  \text{V,} \\ &\text{f} = \text{f}_{MAX}, \text{ inputs switching} \end{aligned}$	7.5 ns cycle, 133 MHz	-	80	mA
I <sub>SB4</sub>	Automatic CE power-down current – TTL inputs	$\begin{aligned} &\text{Max V}_{\text{DD}}, \text{ device deselected,} \\ &\text{V}_{\text{IN}} \geq \text{V}_{\text{IH}} \text{ or V}_{\text{IN}} \leq \text{V}_{\text{IL}}, \\ &\text{f = 0, inputs static} \end{aligned}$	7.5 ns cycle, 133 MHz	_	70	mA

# Capacitance

Parameter [10]	Description	Test Conditions	100-pin TQFP Max	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz},$	5	pF
C <sub>CLK</sub>	Clock input capacitance	V <sub>DD</sub> = 3.3 V, V <sub>DDQ</sub> = 2.5 V	5	pF
C <sub>I/O</sub>	Input/output capacitance	י אטטי – יי	5	pF

## **Thermal Resistance**

Parameter [10]	Description	Test Conditions		100-pin TQFP Package	Unit
$\Theta_{JA}$	Thermal resistance	Test conditions follow standard	With Still Air (0 m/s)	37.95	°C/W
	(junction to ambient)	test methods and procedures for measuring thermal impedance, according to EIA/JESD51	With Still Air (1 m/s)	33.19	°C/W
			With Still Air (3 m/s)	30.44	°C/W
$\Theta_{JB}$	Thermal resistance (junction to board)		-	24.07	°C/W
$\Theta_{\sf JC}$	Thermal resistance (junction to case)			8.36	°C/W

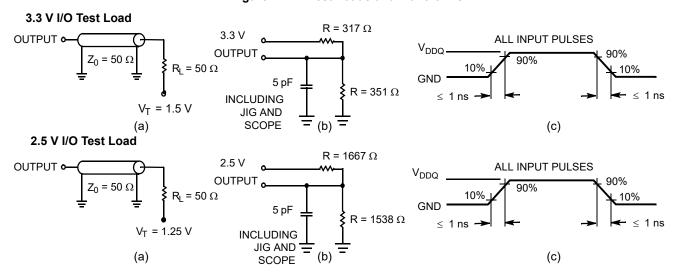
Document Number: 002-12709 Rev. \*A

Note
10. Tested initially and after any design or process change that may affect these parameters.



## **AC Test Loads and Waveforms**

Figure 2. AC Test Loads and Waveforms





## **Switching Characteristics**

Over the Operating Range

Parameter [11, 12]	Description	-1	33	Unit
Parameter [117, 12]	Безсприон		Max	Unit
t <sub>POWER</sub>	V <sub>DD</sub> (typical) to the first access <sup>[13]</sup>	1	_	ms
Clock		<u>.</u>		
t <sub>CYC</sub>	Clock cycle time	7.5	_	ns
t <sub>CH</sub>	Clock HIGH	2.1	_	ns
t <sub>CL</sub>	Clock LOW	2.1	_	ns
Output Times		<u>.</u>		
t <sub>CDV</sub>	Data output valid after CLK rise	_	6.5	ns
t <sub>DOH</sub>	Data output hold after CLK rise	2.0	_	ns
t <sub>CLZ</sub>	Clock to low Z [14, 15, 16]	2.0	_	ns
t <sub>CHZ</sub>	Clock to high Z [14, 15, 16]	_	4.0	ns
t <sub>OEV</sub>	OE LOW to output valid	_	3.2	ns
t <sub>OELZ</sub>	OE LOW to output low Z [14, 15, 16]	0	_	ns
t <sub>OEHZ</sub>	OE HIGH to output high Z [14, 15, 16]	_	4.0	ns
Set-up Times			•	
t <sub>AS</sub>	Address setup before CLK rise	1.5	_	ns
t <sub>ADS</sub>	ADSP, ADSC setup before CLK rise	1.5	_	ns
t <sub>ADVS</sub>	ADV setup before CLK rise	1.5	_	ns
t <sub>WES</sub>	GW, BWE, BW <sub>[A:D]</sub> setup before CLK rise	1.5	_	ns
t <sub>DS</sub>	Data input setup before CLK rise	1.5	_	ns
t <sub>CES</sub>	Chip enable setup	1.5	_	ns
Hold Times			•	
t <sub>AH</sub>	Address hold after CLK rise	0.5	_	ns
t <sub>ADH</sub>	ADSP, ADSC hold after CLK rise	0.5	_	ns
t <sub>WEH</sub>	GW, BWE, BW <sub>[A:D]</sub> hold after CLK rise	0.5	_	ns
t <sub>ADVH</sub>	ADV hold after CLK rise	0.5	_	ns
t <sub>DH</sub>	Data input hold after CLK rise	0.5	_	ns
t <sub>CEH</sub>	Chip enable hold after CLK rise	0.5	-	ns

<sup>11.</sup> Timing reference level is 1.5 V when V<sub>DDQ</sub> = 3.3 V and is 1.25 V when V<sub>DDQ</sub> = 2.5 V.

12. Test conditions shown in (a) of Figure 2 on page 12 unless otherwise noted.

13. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power needs to be supplied above V<sub>DD(minimum)</sub> initially, before a read or write operation can be initiated.

<sup>14.</sup>  $t_{CHZ}$ ,  $t_{OELZ}$ , and  $t_{OEHZ}$  are specified with AC test conditions shown in part (b) of Figure 2 on page 12. Transition is measured  $\pm$  200 mV from steady-state voltage.

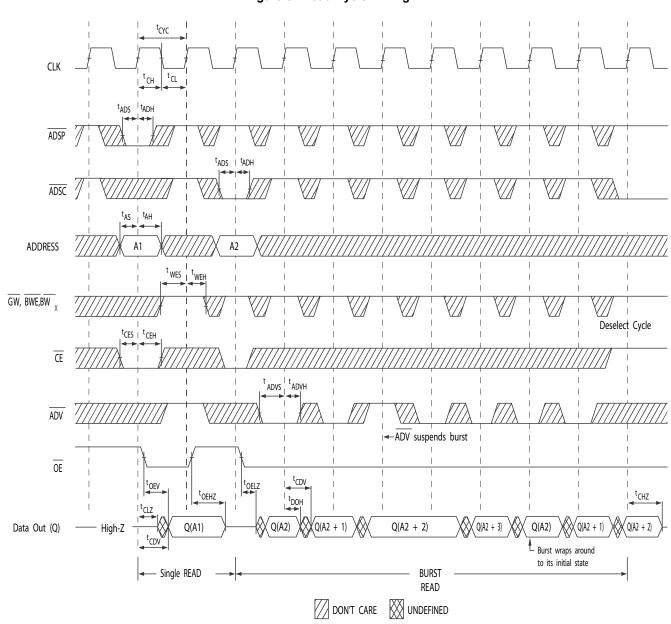
<sup>15.</sup> At any given voltage and temperature, t<sub>OEHZ</sub> is less than t<sub>OELZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.

<sup>16.</sup> This parameter is sampled and not 100% tested.



## **Timing Diagrams**

Figure 3. Read Cycle Timing [17]



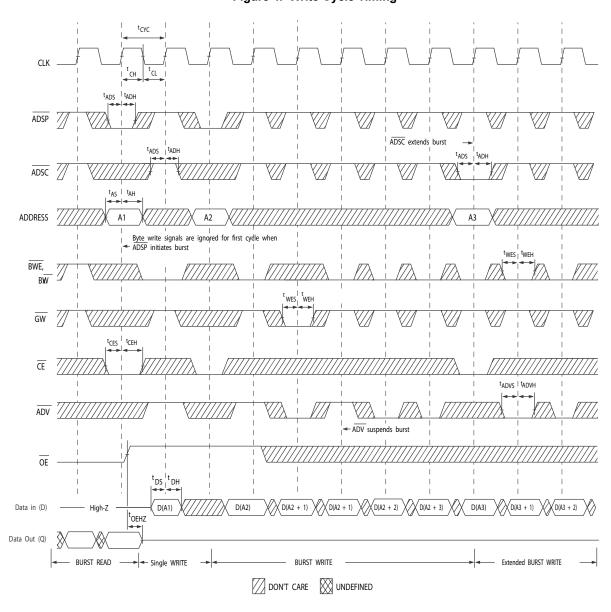
### Note

<sup>17.</sup> On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.



## Timing Diagrams (continued)

Figure 4. Write Cycle Timing [18, 19]



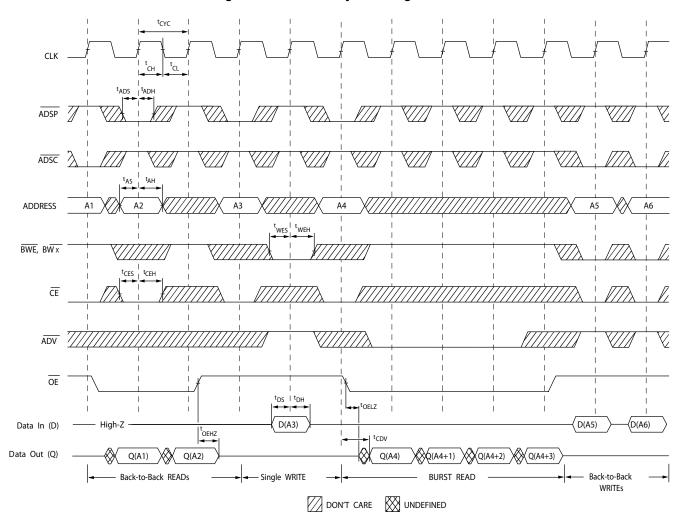
### Notes

<sup>18.</sup> On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH. 19. Full width write can be initiated by either  $\overline{GW}$  LOW; or by  $\overline{GW}$  HIGH,  $\overline{BWE}$  LOW and  $\overline{BW}_X$  LOW.



## Timing Diagrams (continued)

Figure 5. Read/Write Cycle Timing  $^{[20,\ 21,\ 22]}$ 



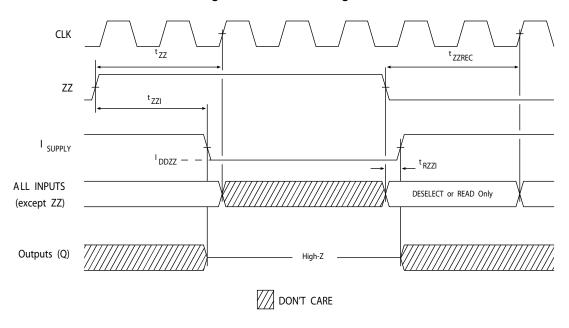
### Notes

<sup>20.</sup> On this diagram, when  $\overline{\text{CE}}$  is LOW:  $\overline{\text{CE}}_1$  is LOW, CE<sub>2</sub> is HIGH and  $\overline{\text{CE}}_3$  is LOW. When  $\overline{\text{CE}}$  is HIGH:  $\overline{\text{CE}}_1$  is HIGH or CE<sub>2</sub> is LOW or  $\overline{\text{CE}}_3$  is HIGH. 21. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by ADSP or ADSC. 22.  $\overline{\text{GW}}$  is HIGH.



## Timing Diagrams (continued)

Figure 6. ZZ Mode Timing  $^{[23,\ 24]}$ 



<sup>23.</sup> Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device. 24. DQs are in high Z when exiting ZZ sleep mode.



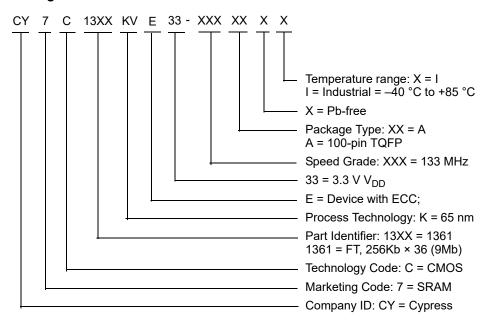
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Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1361KVE33-133AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

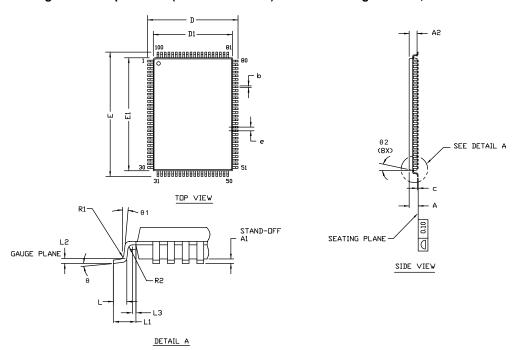
## **Ordering Code Definitions**





## **Package Diagrams**

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



SYMBOL	DIM	ENSIC	NS
STIVIDOL	MIN.	NOM.	MAX.
Α	_	_	1.60
A1	0.05	_	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	_	0.20
R2	0.08	_	0.20
θ	0°	_	7°
θ1	0°	_	ı
θ2	11°	12°	13°
С	_	_	0.20
b	0.22	0.30	
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		С
L3	0.20		_
е	0.65 TYP		

### NOTE:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH.

  MOLD PROTRUSION/END FLASH SHALL

  NOT EXCEED 0.0098 in (0.25 mm) PER SIDE.

  BODY LENGTH DIMENSIONS ARE MAX PLASTIC

  BODY SIZE INCLUDING MOLD MISMATCH.
- 3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 \*G



## **Acronyms**

Acronym	Description		
CMOS	Complementary Metal Oxide Semiconductor		
CE	Chip Enable		
EIA	Electronic Industries Alliance		
I/O	Input/Output		
JEDEC	Joint Electron Devices Engineering Council		
LMBU	Logical Multi-Bit Upsets		
LSB	Least Significant Bit		
LSBU	Logical Single-Bit Upsets		
MSB	Most Significant Bit		
OE	Output Enable		
PBGA	Plastic Ball Grid Array		
SEL	Single Event Latch up		
SRAM	Static Random Access Memory		
TQFP	Thin Quad Flat Pack		
TTL	Transistor-Transistor Logic		

## **Document Conventions**

## **Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



# **Document History Page**

	Document Title: CY7C1361KVE33, 9-Mbit (256K × 36) Flow-Through SRAM Document Number: 002-12709					
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change		
**	5413843	PRIT	08/24/2016	New data sheet.		
*A	6013469	RMES	01/04/2018	Updated Package Diagrams: spec 51-85050 – Changed revision from *E to *G. Updated to new template.		



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