

## MOSFET

### 650 V CoolSiC™ M1 SiC Trench Power Device

The 650 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 650V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.

#### Features

- Optimized switching behavior at higher currents
- Commutation robust fast body diode with low  $Q_f$
- Superior gate oxide reliability
- $T_{j,max}=175^{\circ}\text{C}$  and excellent thermal behavior
- Lower  $R_{DS(on)}$  and pulse current dependency on temperature
- Increased avalanche capability
- Compatible with standard drivers (recommended driving voltage: 0V-18V)
- Kelvin source provides up to 4 times lower switching losses

#### Benefits

- Unique combination of high performance, high reliability and ease of use
- Ease of use and integration
- Suitable for topologies with continuous hard commutation
- Higher robustness and system reliability
- Efficiency improvement
- Reduced system size leading to higher power density

#### Potential applications

- Telecom and Server SMPS
- UPS (uninterruptable power supplies)
- Solar PV inverters
- EV charging infrastructure
- Energy storage and battery formation
- Class D amplifiers

#### Product validation

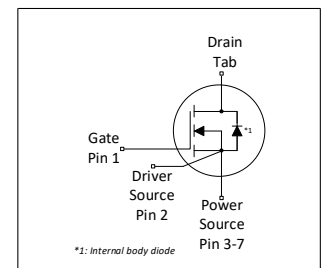
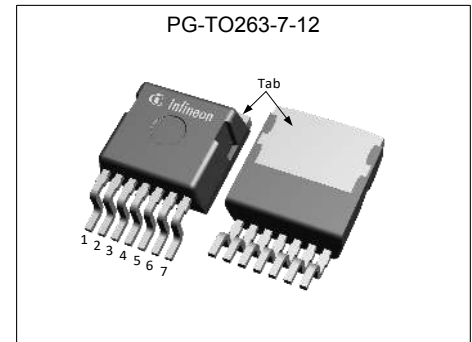
Fully qualified according to JEDEC for Industrial Applications

*Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_J = 25^{\circ}\text{C}$	650	V
$R_{DS(on),typ}$	72	m $\Omega$
$R_{DS(on),max}$	94	m $\Omega$
$Q_{G,typ}$	22	nC
$I_{DM}$	69	A
$Q_{oss} @ 400\text{ V}$	52	nC
$E_{oss} @ 400\text{ V}$	7.8	$\mu\text{J}$

Type / Ordering Code	Package	Marking	Related Links
IMBG65R072M1H	PG-TO263-7-12	65R072M1	see Appendix A



RoHS

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## 1 Maximum ratings

at  $T_J = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous DC drain current <sup>1)</sup>	$I_D$	-	-	33 23	A	$T_C = 25\text{ °C}$ $T_C = 100\text{ °C}$
Peak drain current <sup>2)</sup>	$I_{DM}$	-	-	69	A	$T_C = 25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	114	mJ	$I_D = 4.3\text{ A}$ , $V_{DD} = 50\text{ V}$ ; see table 11
Avalanche energy, repetitive	$E_{AR}$	-	-	0.57	mJ	$I_D = 4.3\text{ A}$ , $V_{DD} = 50\text{ V}$ ; see table 11
Avalanche current, single pulse	$I_{AS}$	-	-	4.3	A	-
MOSFET $dv/dt$ ruggedness	$dv/dt$	-	-	200	V/ns	$V_{DS} = 0\text{...}400\text{ V}$
Gate source voltage (static) <sup>3)</sup>	$V_{GS}$	-5	-	23	V	static
Gate source voltage (transient)	$V_{GS}$	-7	-	25	V	$t_{pulse, positive} \leq 1\%$ duty cycle/ $f_{sw}$
Power dissipation	$P_{tot}$	-	-	140	W	$T_C = 25\text{ °C}$
Storage temperature	$T_{stg}$	-55	-	150	°C	-
Operating junction temperature	$T_J$	-55	-	175	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous reverse drain current <sup>1)</sup>	$I_{SDC}$	-	-	33 22	A	$V_{GS}=18\text{ V}$ , $T_C = 25\text{ °C}$ $V_{GS}=0\text{ V}$ , $T_C = 25\text{ °C}$
Repetitive peak reverse drain current <sup>1)</sup>	$I_{SRM}$	-	-	69	A	$T_C = 25\text{ °C}$ , pulse width $t_p \leq 250\text{ ns}$
Insulation withstand voltage	$V_{ISO}$	-	-	n.a.	V	$V_{rms}$ , $T_C = 25\text{ °C}$ , $t = 1\text{ min}$

<sup>1)</sup> Limited by  $T_{J,max}$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{J,max}$

<sup>3)</sup> The maximum gate-source voltage in the application design should be in accordance to IPC-9592B

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	1.07	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

## 3 Operating range

**Table 4 Operating range**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate-source voltage operating range including undershoots <sup>1)</sup>	$V_{GS}$	-2	-	20	V	-

<sup>1)</sup> **Important note: the selection of positive and negative gate-source voltages impacts the long-term behavior of the device.** The design guidelines described in the CoolSiC™ MOSFET 650 V M1 trench power device application note AN\_1907\_PL52\_1911\_144109 must be considered to ensure sound operation of the device over the planned lifetime.

## 4 Electrical characteristics

at  $T_J = 25\text{ °C}$ , unless otherwise specified

**Table 5 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS} = 0\text{ V}$ , $I_D = 0.4\text{ mA}$
Gate threshold voltage <sup>1)</sup>	$V_{GS(th)}$	3.5	4.5	5.7	V	$V_{DS} = V_{GS}$ , $I_D = 4\text{ mA}$
Zero gate voltage drain current	$I_{DSS}$	-	1 3	150 -	$\mu\text{A}$	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 25\text{ °C}$ $V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 175\text{ °C}$
Gate leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.072 0.101	0.094 -	$\Omega$	$V_{GS} = 18\text{ V}$ , $I_D = 13.3\text{ A}$ , $T_J = 25\text{ °C}$ $V_{GS} = 18\text{ V}$ , $I_D = 13.3\text{ A}$ , $T_J = 175\text{ °C}$
Internal gate resistance	$R_G$	-	9.0	-	$\Omega$	$f = 1\text{ MHz}$

**Table 6 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	744	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$
Reverse transfer capacitance	$C_{riss}$	-	9	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$
Output capacitance <sup>2)</sup>	$C_{oss}$	-	86	112	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$
Output charge <sup>2)</sup>	$Q_{oss}$	-	52	68	nC	calculation based on $C_{oss}$
Effective output capacitance, energy related <sup>3)</sup>	$C_{o(er)}$	-	98	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{...}400\text{ V}$
Effective output capacitance, time related <sup>4)</sup>	$C_{o(tr)}$	-	129	-	pF	$I_D = \text{constant}$ , $V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{...}400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	6.1	-	ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = 18\text{ V}$ , $I_D = 13.3\text{ A}$ , $R_G = 1.8\text{ }\Omega$ ; see table 10
Rise time	$t_r$	-	7.9	-	ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = 18\text{ V}$ , $I_D = 13.3\text{ A}$ , $R_G = 1.8\text{ }\Omega$ ; see table 10
Turn-off delay time	$t_{d(off)}$	-	12.1	-	ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = 18\text{ V}$ , $I_D = 13.3\text{ A}$ , $R_G = 1.8\text{ }\Omega$ ; see table 10
Fall time	$t_f$	-	7	-	ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = 18\text{ V}$ , $I_D = 13.3\text{ A}$ , $R_G = 1.8\text{ }\Omega$ ; see table 10

<sup>1)</sup> Tested after 1 ms pulse at  $V_{GS} = +20\text{ V}$

<sup>2)</sup> Maximum specification is defined by calculated six sigma upper confidence bound

<sup>3)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

<sup>4)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

**Table 7 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	6	-	nC	$V_{DD} = 400\text{ V}$ , $I_D = 13.3\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	$Q_{gd}$	-	5	-	nC	$V_{DD} = 400\text{ V}$ , $I_D = 13.3\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$
Gate charge total	$Q_g$	-	22	-	nC	$V_{DD} = 400\text{ V}$ , $I_D = 13.3\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$

**Table 8 Body diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	$V_{SD}$	-	4.0	-	V	$V_{GS} = 0\text{ V}$ , $I_S = 13.3\text{ A}$ , $T_J = 25\text{ °C}$
MOSFET forward recovery time	$t_{fr}$	-	18.7	-	ns	$V_{DD} = 400\text{ V}$ , $I_{S0} = 13.3\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9
MOSFET forward recovery charge	$Q_f$	-	60	-	nC	$V_{DD} = 400\text{ V}$ , $I_{S0} = 13.3\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9
MOSFET peak forward recovery current	$I_{frm}$	-	6.1	-	A	$V_{DD} = 400\text{ V}$ , $I_{S0} = 13.3\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9

## 5 Electrical characteristics diagrams

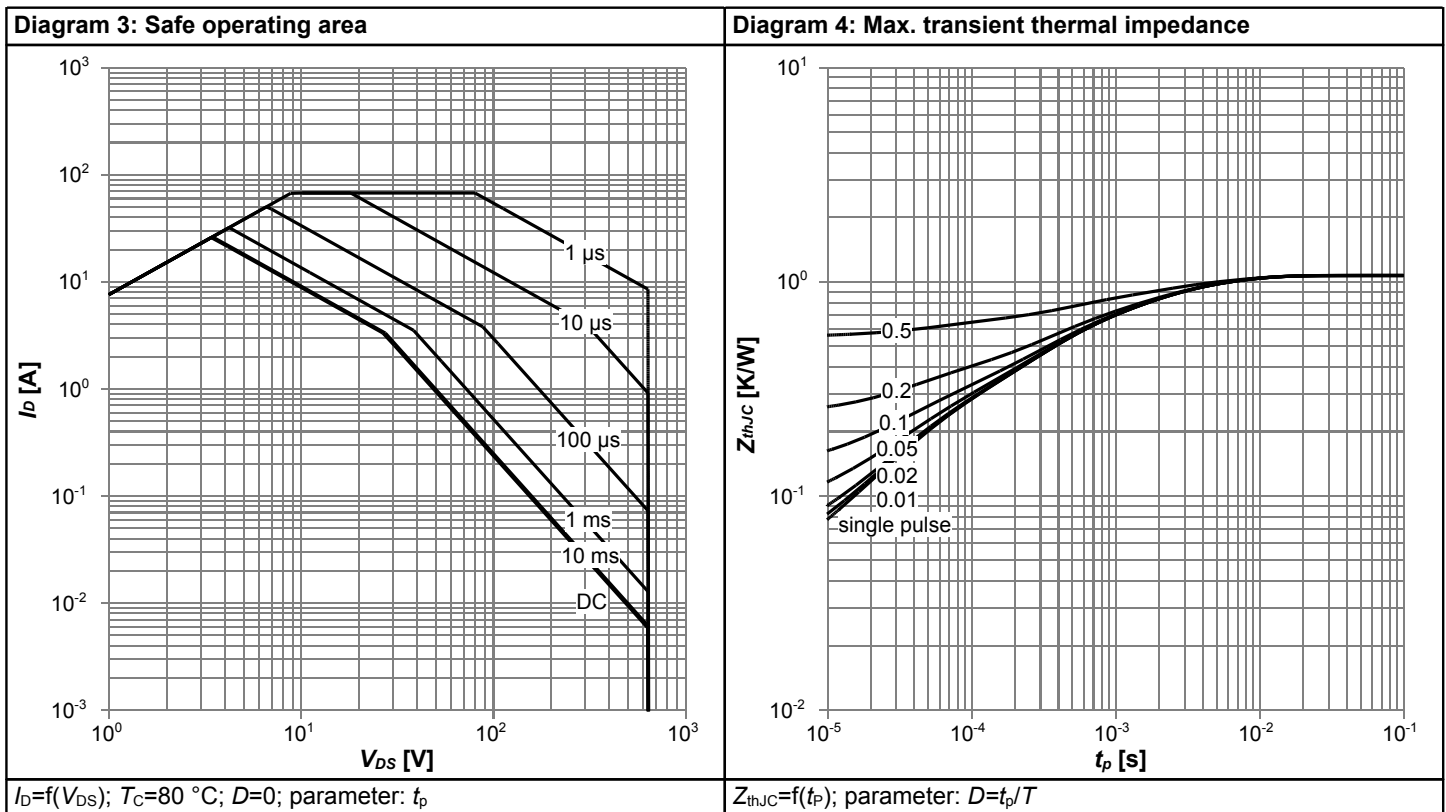
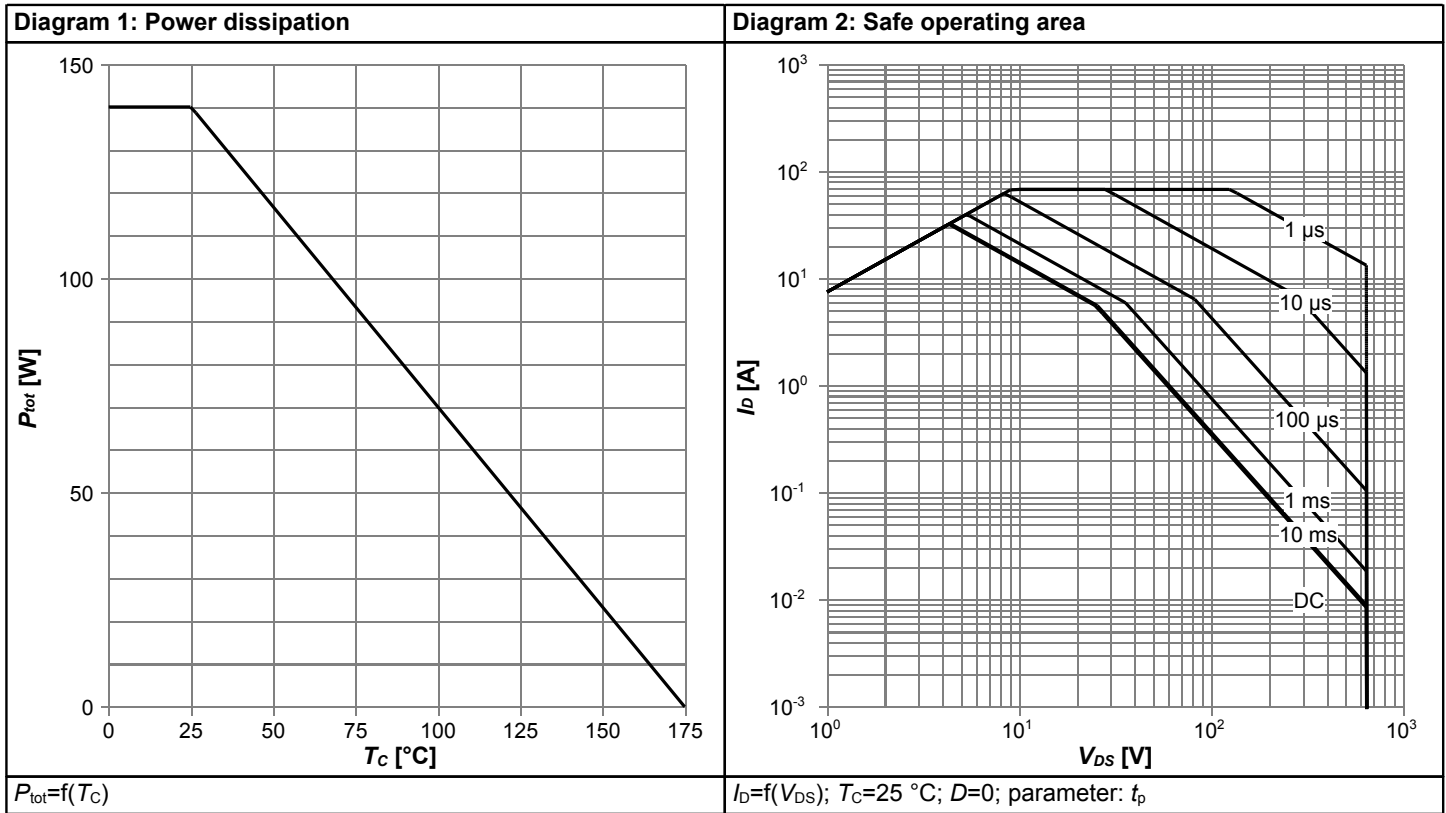
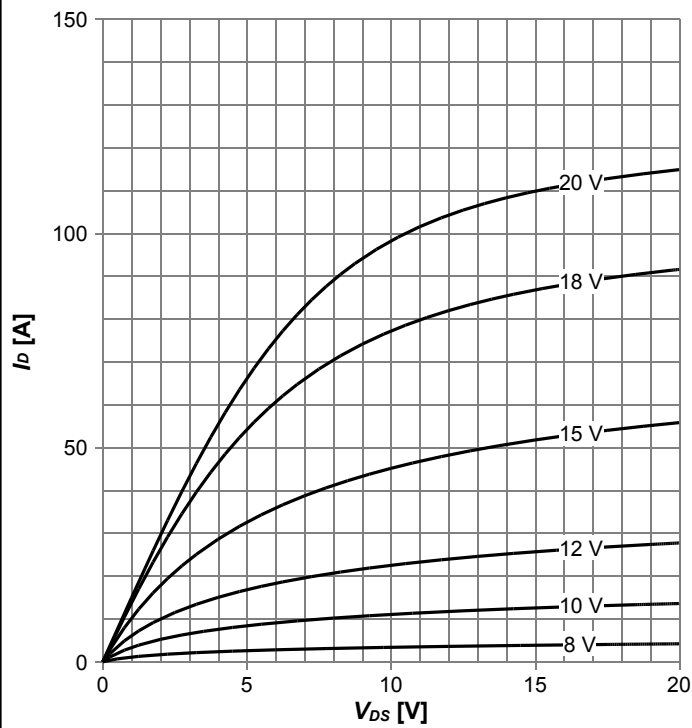
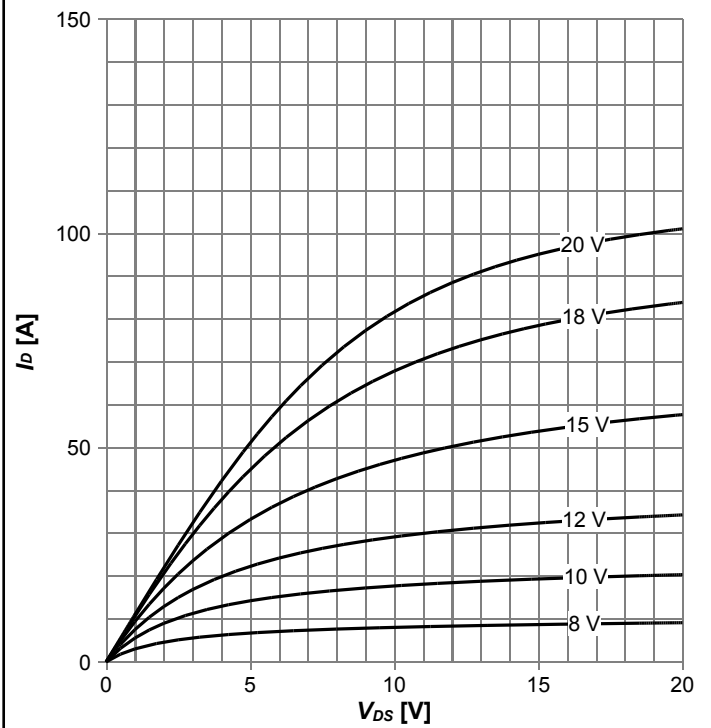


Diagram 5: Typ. output characteristics



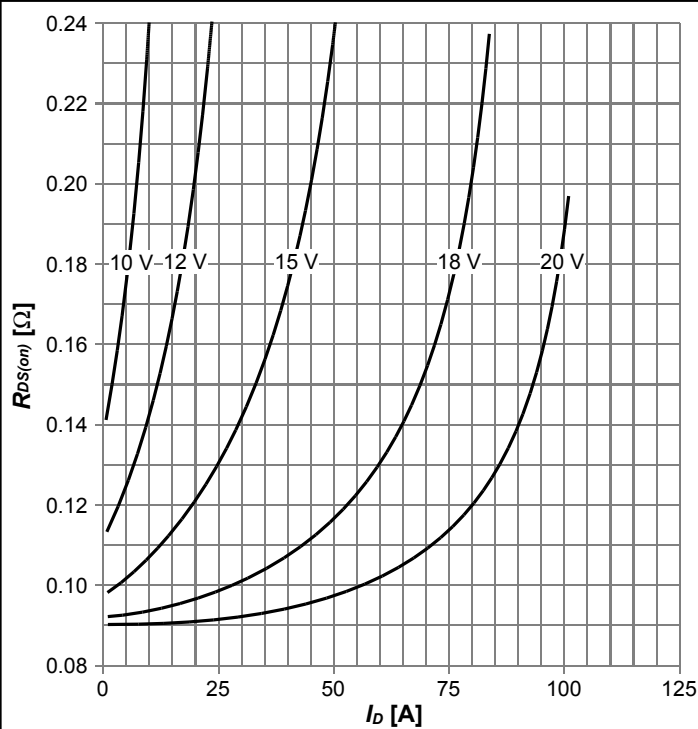
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



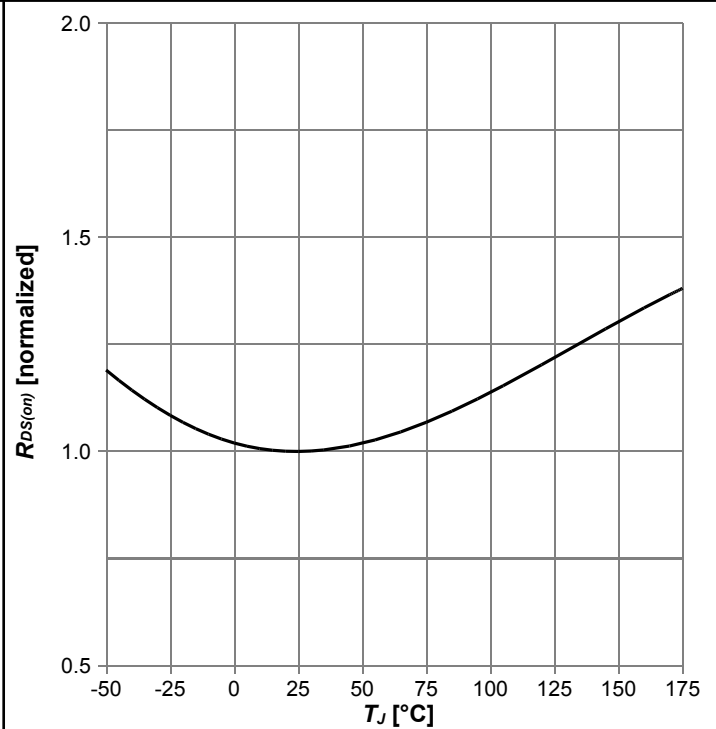
$I_D = f(V_{DS})$ ;  $T_j = 150^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D)$ ;  $T_j = 150^\circ\text{C}$ ; parameter:  $V_{GS}$

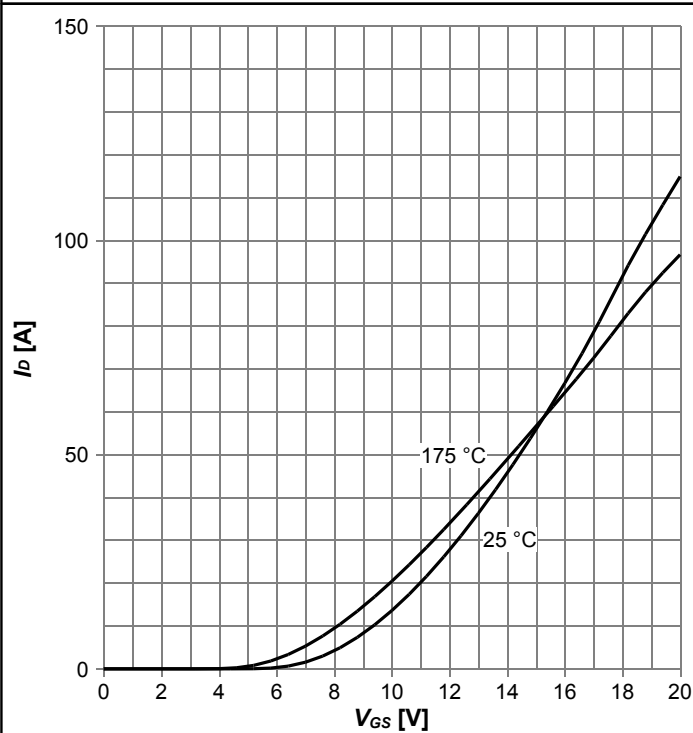
Diagram 8: Drain-source on-state resistance



$R_{DS(on)} = f(T_j)$ ;  $I_D = 13.3\text{ A}$ ;  $V_{GS} = 18\text{ V}$

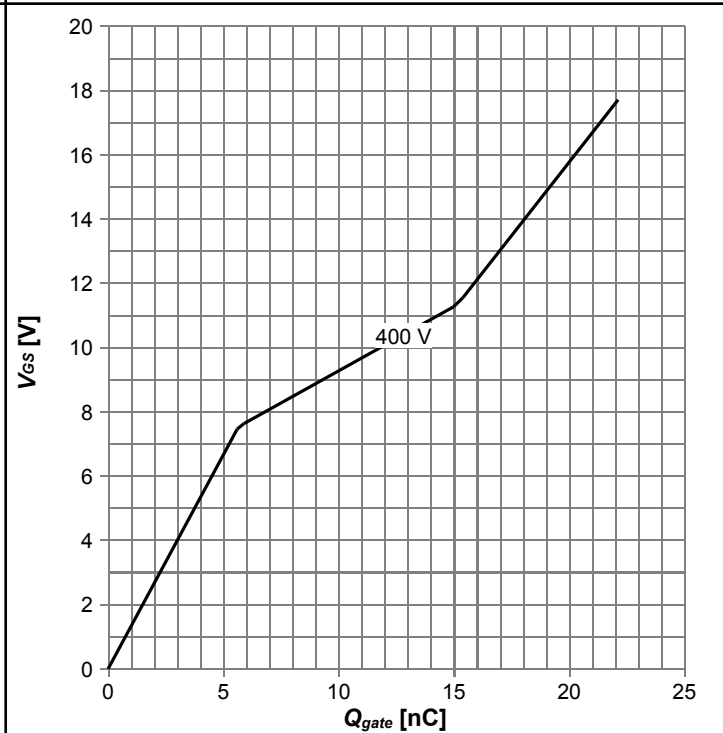


Diagram 9: Typ. transfer characteristics



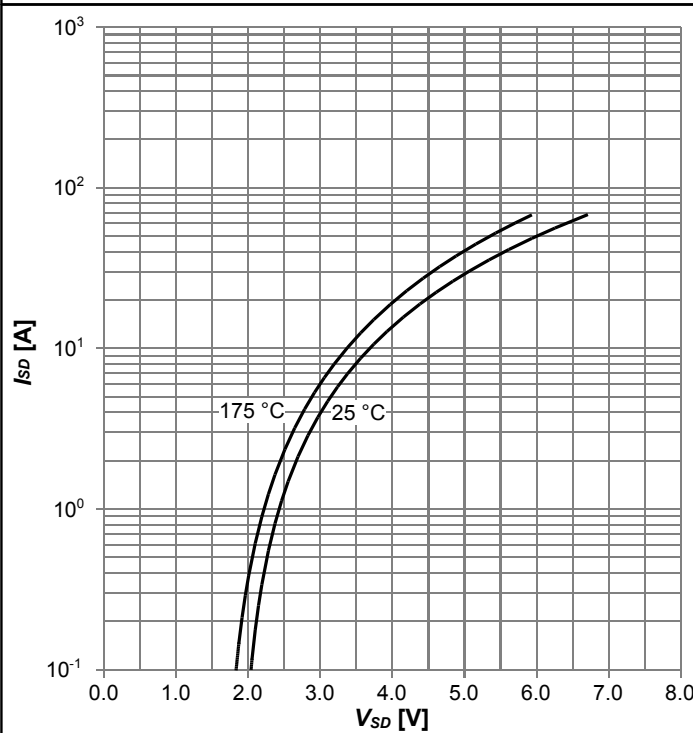
$I_D = f(V_{GS})$ ;  $V_{DS} = 20V$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



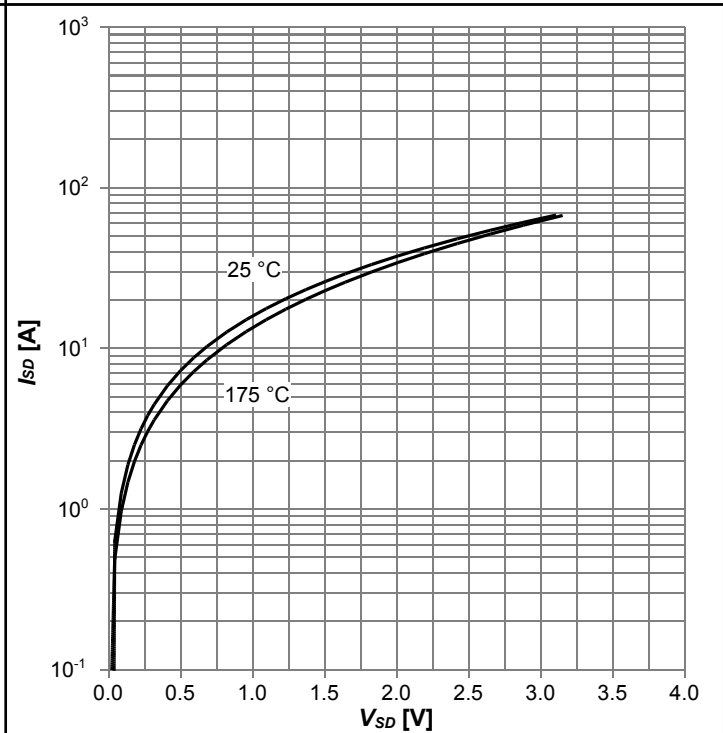
$V_{GS} = f(Q_{gate})$ ;  $I_D = 13.3 A$  pulsed; parameter:  $V_{DD}$

Diagram 11: Typ. reverse characteristics



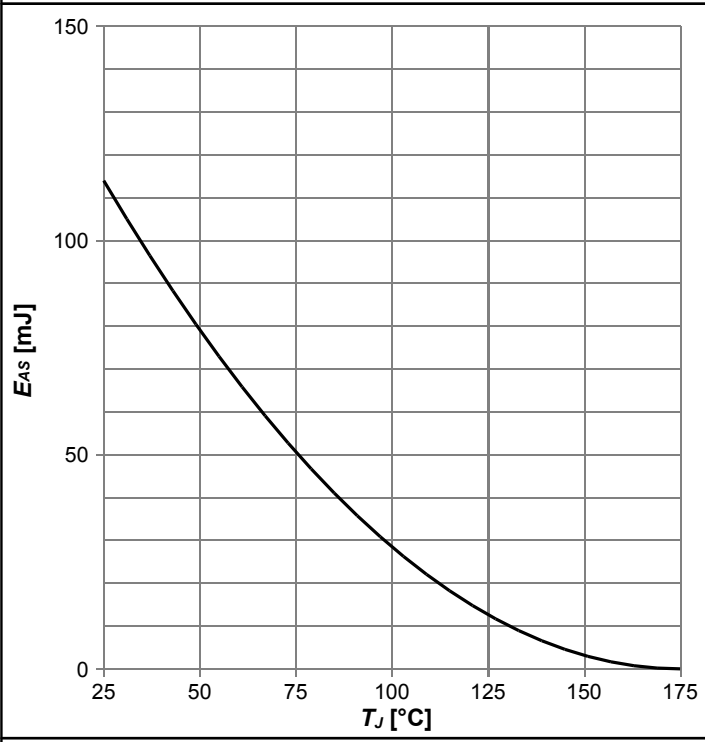
$I_{SD} = f(V_{SD})$ ;  $V_{GS} = 0 V$ ; parameter:  $T_j$

Diagram 12: Typ. reverse characteristics



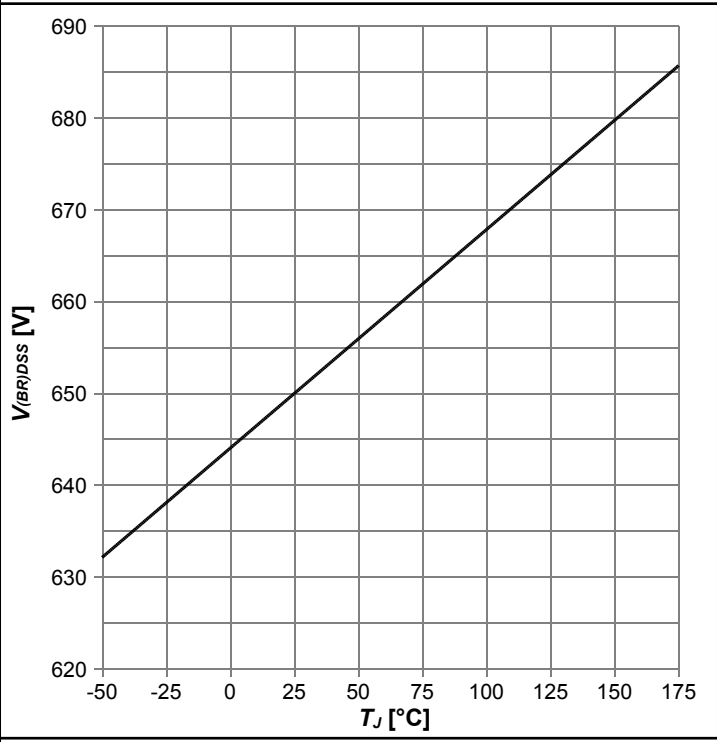
$I_{SD} = f(V_{SD})$ ;  $V_{GS} = 18 V$ ; parameter:  $T_j$

Diagram 13: Avalanche energy



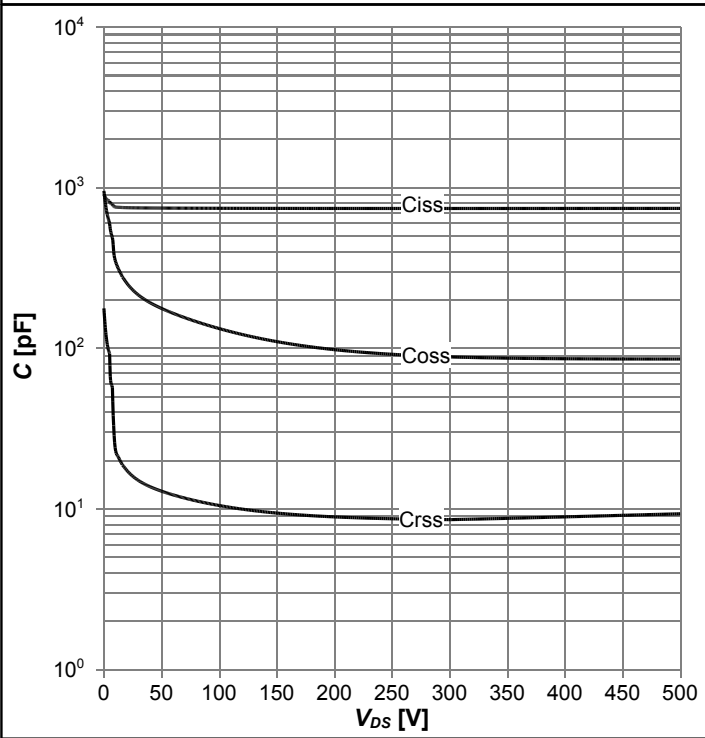
$E_{AS}=f(T_J)$ ;  $I_D=4.3$  A;  $V_{DD}=50$  V

Diagram 14: Drain-source breakdown voltage



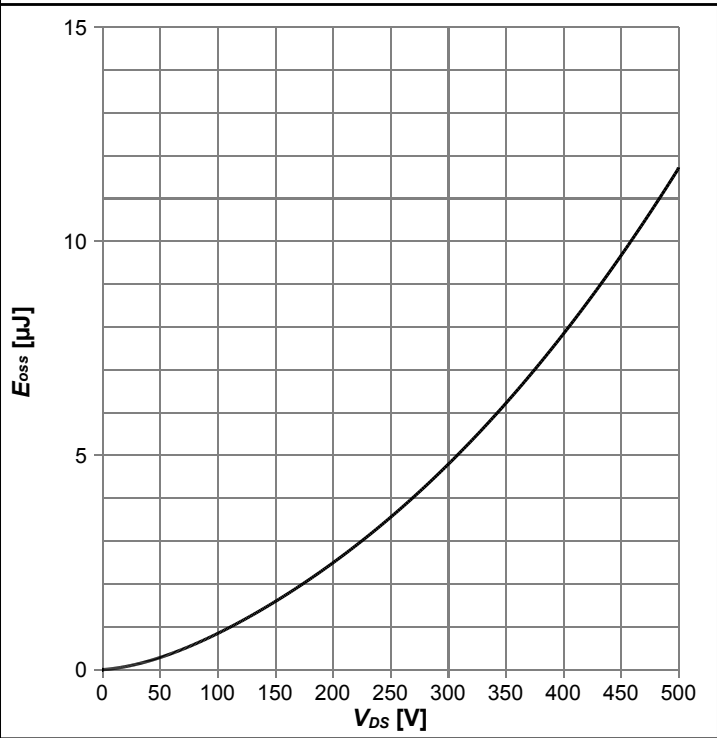
$V_{(BR)DSS}=f(T_J)$ ;  $I_D=0.4$  mA

Diagram 15: Typ. capacitances

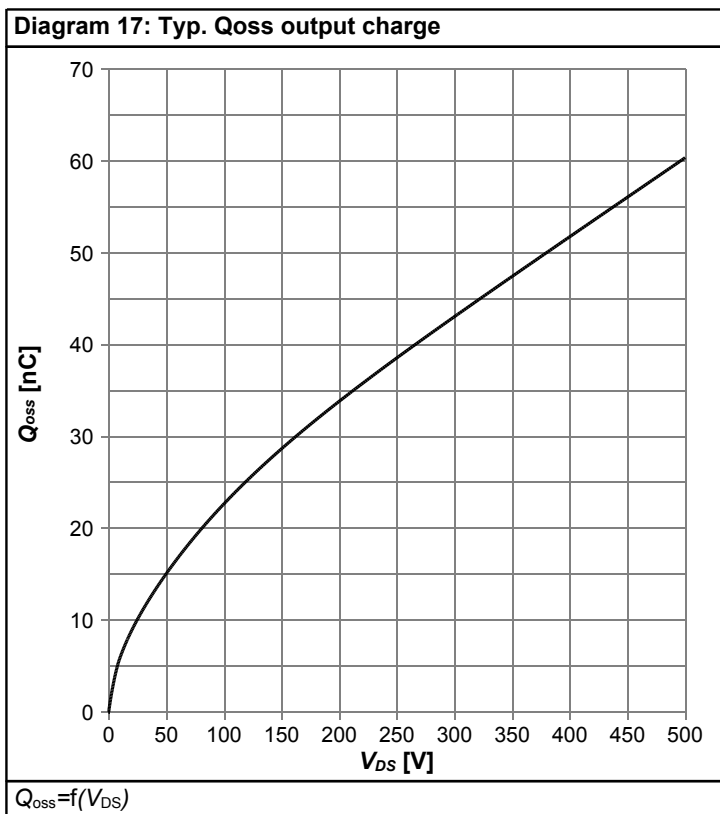


$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=250$  kHz

Diagram 16: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$



## 6 Test Circuits

**Table 9 Body diode characteristics (650V CoolSiC)**

Test circuit for body diode characteristics	Body diode recovery waveform

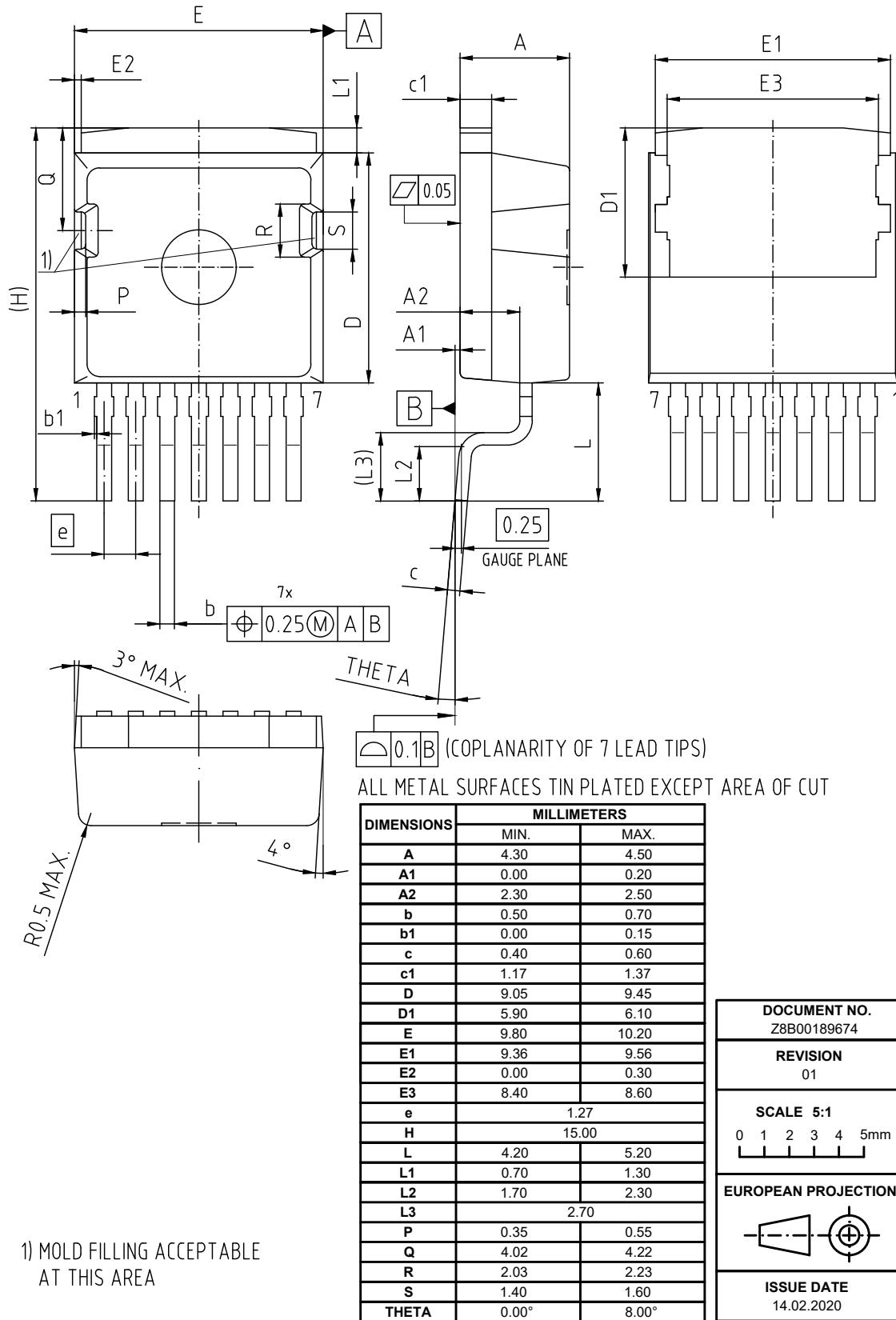
**Table 10 Switching times (650V CoolSiC)**

Switching times test circuit for inductive load	Switching times waveform

**Table 11 Unclamped inductive load (650V CoolSiC)**

Unclamped inductive load test circuit	Unclamped inductive waveform

**7 Package Outlines**



**Figure 1 Outline PG-TO263-7-12, dimensions in mm**

## 8 Appendix A

### Table 12 Related Links

- IFX CoolSiC M1 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolSiC M1 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolSiC M1 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IMBG65R072M1H

**Revision: 2021-12-10, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-12-10	Release of final version

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