TDC-GP1

General Purpose TDC

2 chan. 250ps / 1 chan. 125ps resolution

Functional description

12.2.2001

acam - solutions in time

Precision Time Interval Measurement

acam
9822YCI
TDC-GP1

mess-electronic

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The structure of the manual

The manual of the TDC-GP1 is divided into 5 main sections. It is designed as an information and reference book. It's structure is clear so that it can answer almost any questions you have while working with the TDC-GP1 without drowning or overwhelming you in masses of unnecessarily detailed information. Certain information can therefore be found in various sections of this manual so that continuous searching and turning of pages becomes unnecessary.

The 5 main sections are:

- **An introduction to the TDC-GP1**
  This section surveys the various functional possibilities the TDC-GP1 offers without describing any details regarding the specific functions. You will find everything noteworthy in this section concerning principle applications and measurement problems. This section should be interesting for anyone who is dealing with the chip for the first time or who is interested in getting a brief overview regarding new developments and applications.

- **Details of the TDC-GP1**
  This section reveals in detail the functions of the chip. The various application possibilities are described with precision. A developer can find information here regarding circuit and software design.

- **Application examples, application references**
  This section of the manual describes several specific examples regarding the circuit and controlling of the TDC-GP1.

- **Measurement results and diagrams**
  All theory is grey. How good is the TDC-GP1 in fact? This is where the GP1 reveals it's skills as well as it's limits. This section of the manual is interesting for everyone, but especially for those customers who plan to - or have to - exhaust the chip's limits. It is also interesting for anyone looking to compare his own test results to ours. Are your measurement results clearly better or worse than ours, then call us or write us an email. We gladly give and receive tips.

- **Known problems and solutions**
  Here you'll find descriptions and work around possibilities of problems of the TDC-GP1. 'Nobody is Perfect', the TDC-GP1 also has 'functionality', which weren't planned in this way or which are note very meaningful. This chapter should be read through in each case to be informed from the start.

- **Last changes:**
  Okt-2000: Chapter 5.1 Secure calibration software routine
  Feb-2001: Chapter 2.4.4, 2.11.1 No Hit-Disable in MB2

1. Features of the TDC-GP1

1.1 General Description

Even in today's high-tech world TDCs are still unfamiliar and unknown chips. Therefore, let's begin with a brief introduction.

The abbreviation TDC stands for Time to Digital Converter. These chips transform time intervals into digital values with highest precision. They can therefore be described as analogies to ADCs (Analogue to Digital Converter), which have the same function with analogous voltage. Although this definition would permit wrist watches or simple digital meters to be considered TDCs, the term TDC is used only to describe high precision time measuring devices. Generally the term 'TDC' is used for converters with a resolution of less than one nanosecond. This high resolution cannot be achieved using meters or similar devices without high expenditures so that new customized solutions become necessary.

The TDCs of the acam-messelectronic gmbh are based on the use of digital propagation times - mainly with CMOS processors. The resolution that can actually be achieved is in the range of 30 ps - 300 ps - depending on the semiconductor process used.

The GP1 seems to cover the lower resolution area with it's 250 ps in 2 channel mode or it's 125 ps in High Resolution Mode. This is however the area where most applications can be found. Just like any other chip, a TDC is not characterized by it's 'key features' alone such as for instance it's resolution but also by various other characteristics such as it's usability, it's flexibility regarding applications, it's smooth integration into available circuits, etc. We dedicated a lot of time and attention to these additional items and attempted to equip the GP1 with extensive functionality. We created a chip that enables a smooth application for many users.

1.2 Key features

- 2 channels with 250 ps resolution or 1 channel with 125ps resolution
- 4-fold multihit capabilities per channel Queuing for up to 8-fold multihit
- Resolution on both channels absolutely identical.
- Double pulse resolution approx. 15 ns
- Retriggerability
- 2 measurement ranges
    - a. 3 ns - 7,6 µs
    - b. 60 ns -200 ms (with predivider, only 1 channel)
- The 8 events on both channels can be measured against one another arbitrarily, no minimum time difference, negative time differences possible
- Resolution Adjust Mode: quartz-accurate adjustment of resolution via software
- 4 ports for the measurement of resistors, inductors or capacitors
- Edge sensitivities of the measurement inputs are adjustable
- Enable pins are available to both stop inputs for powerful windowing possibilities
- Efficient internal 16-bit ALU, the measured result can be calibrated and multiplied with a 24 bit integer
- ALU's time for calculation is independent of the external clock. Approx. 4 µs for complete calibration and multiplication
- Up to 4 calibrated or 8 uncalibrated measurement values can be stored internally.
- Calibration and control clocks from 500 kHz up to 35 MHz (up to 100 MHz with use of internal predivider)
- Space saving and easy to handle 44-TQFP package (0.8 mm pitch, 1.27 mm max. building height)
- Industrial temperature range: -40 ºC ... +85 ºC
- Operating voltage : 2.7 V ... 5.5 V
- Extremely low power consumption, battery-driven operation possible

1.3 Block diagram of the GP1

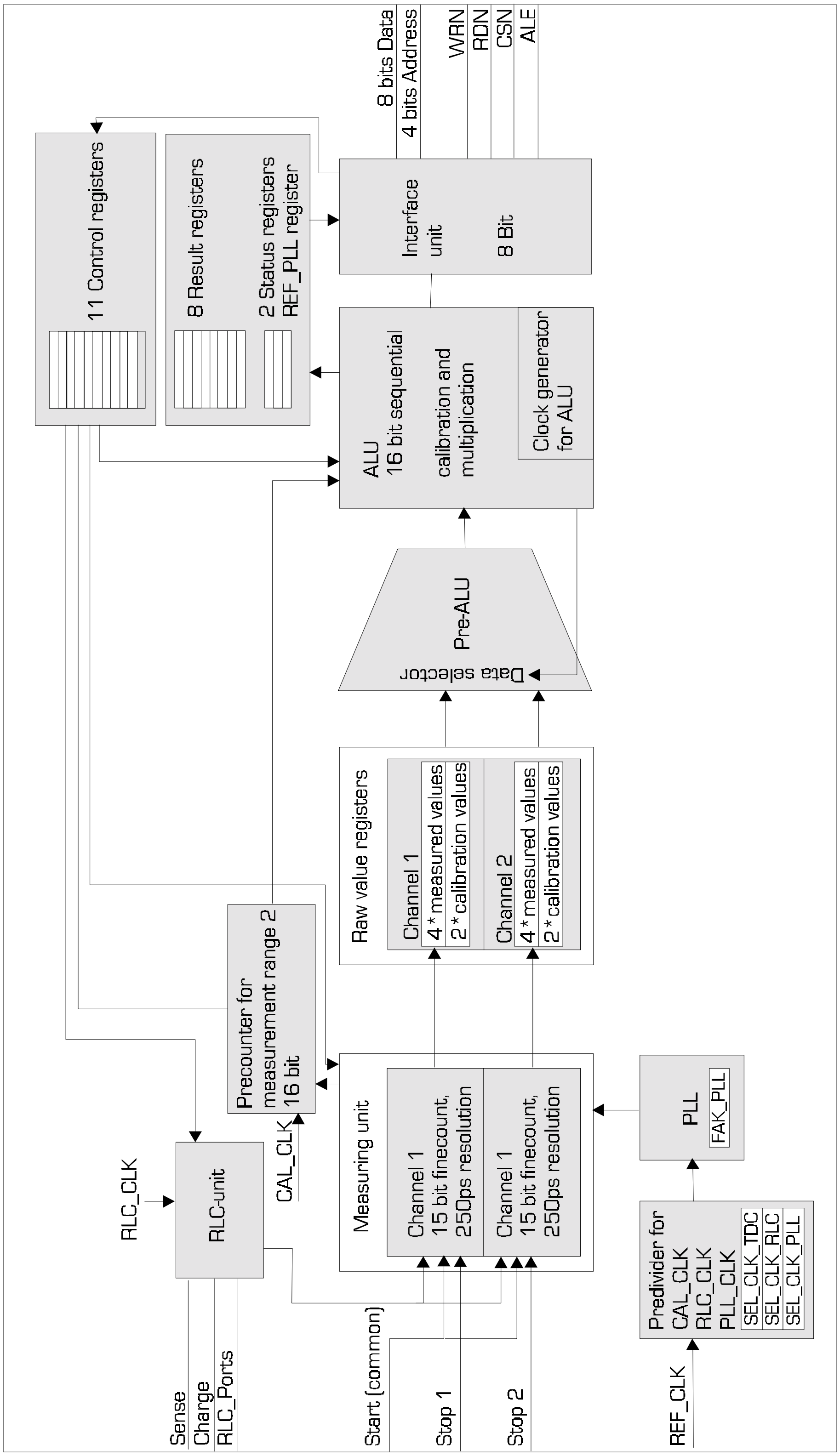

8 bits Data
4 bits Address
WRN
RDN
CSN
ALE
11 Control registers
8 Result registers
2 Status registers
REF_PLL register
Interface unit
8 Bit
ALU
16 bit sequential
calibration and multiplication
Clock generator for ALU
Pre-ALU
Data selector
Raw value registers
Channel 1
4 * measured values
2 * calibration values
Channel 2
4 * measured values
2 * calibration values
Precounter for measurement range 2
16 bit
CAL_CLK
Measuring unit
Channel 1
15 bit finecount,
250ps resolution
Channel 1
15 bit finecount,
250ps resolution
PLL
FAK_PLL
Predivider for
CAL_CLK
RLC_CLK
PLL_CLK
SEL_CLK_TDC
SEL_CLK_RLC
SEL_CLK_PLL
REF_CLK
RLC_CLK
RLC-unit
Sense
Charge
RLC_Ports
Start (common)
Stop 1
Stop 2

Figure 1: Blockdiagram

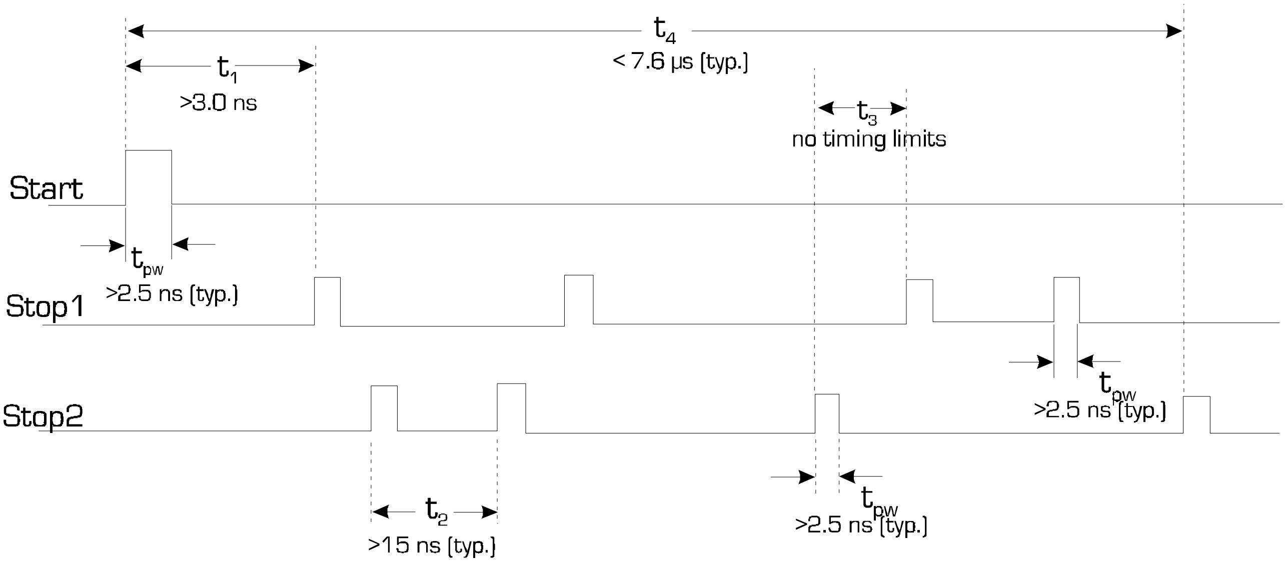
1.4 Measurement range 1

The GP1 offers 2 measuring channels with 250 ps resolution each and a basic measurement range of 15 bit.

- Both channels are absolutely identical with regard to resolution.
- Both channels have a common start input and measure up to four independent stops.
- The channels can optionally be queued behind one another, resulting in 1 channel with 8-fold multihit capability.

The various stops pulses can not only be calculated against the start pulse, but also each other. It makes no difference if the stops arrive on the same or different channels. All time difference combinations between the 8 possible results can be calculated. If you compare events which arrive on different channels it is possible to measure time differences down to zero. When comparing the events that arrive on one channel, the double pulse resolution of the specific channel limits the precision. Figure 1 illustrates the timings. The double pulse resolution is in the range of 15 ns typ. I.e. if two stops arrive on the same channel within less than 15 ns the second stop will be ignored since it arrived during the recovery time of the measurement unit.

Figure 2: Possible measuring sequences in 2-channel operation



It is not necessary to know which one of the two events was the first. If the time difference is negative the result will be negative as well.

Take as example the measurement of the phase difference of two signals which are phase modulated against each other. The first signal may be found on channel 1 and the second signal on channel 2. Not only the smallest possible phase differences can be measured but also negative phase situations can be identified and measured. The direct measurement of a phase modulation around 0 is possible.

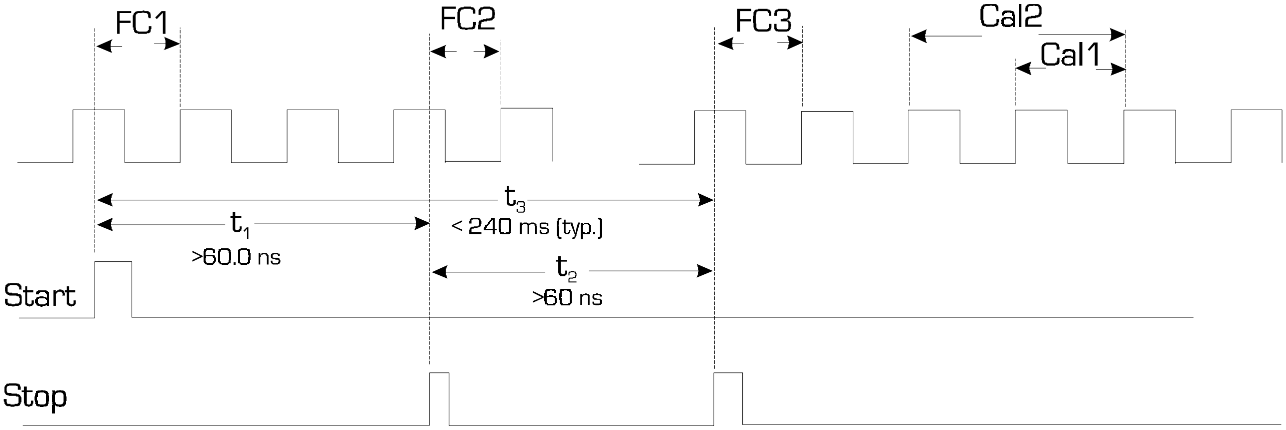
The start on both channels must be activated at least 3 ns before the first stop. The last event that can be measured must arrive within 2^{15} LSBs (approx. 7.6 µs) from the activation of the start. Otherwise the TDC will go into time-out. For measurements between stop 1 and stop 2, the position of the start pulse is not relevant to, but the time-out condition must be respected.

An additional feature in measurement range 1 is queuing. In this mode the two channels are connected internally one after the other. This results in the formation of a 1 channel TDC with 8-fold multihit capability. If the TDC is set to this option the value register of channel 1 will automatically move the stop from channel 1 to channel 2 after the register is full of hits. The stop input of channel 2 is ignored in this mode.

1.5 Measurement range 2

It is necessary to introduce a predivider in order to carry out measurements of large time intervals. When start is activated, the time difference from start to the next rising edge of the calibration clock is measured by the measurement unit (FC1). Afterwards a counter is activated that counts the periods of the predivider. The stop pulse of the measurement signal restarts the measurement unit. The following rising edge of the calibration clock stops the measurement unit (FC2). In the following one and two periods of the calibration clock will be measured for calibration. The GP1 is in possession of a 16 bit predivider. This allows the measurement of large time intervals (> 200 ms) with the undiminished resolution of the TDCs. The maximum measurement range is defined as T_{ref}*SEL_CLK_TDC*2^{16} ($2*T_{ref} < 7.6\mu s$).

Figure 3: Measuring large time intervals with the predivider



$$time = period * \left(cc + \frac{FC1 - FC2}{Cal2 - Cal1} \right),\ cc{=}value\ of\ the\ precounter$$

For measurements in the measurement range 2 the GP1 is only in possession of 1 channel. The stop 1 input is active. This channel has 4-fold multihit capabilities in normal resolution mode. The stop events cannot be measured against each other, only against the start event. The double pulse resolution is 1.5 *(T_{ref}*SEL_CLK_TDC)+25 ns of the calibration clock.

1.6 R-L-C Unit

Simple circuiting techniques make it possible to derive resistor, capacitor or inductor values from time interval measurements. The R-L-C unit makes this possible with only a few external components connected to the GP1. This unit enables the operation of the TDC with different sensor applications that fall back on the 3 basic dimensions of electronics. The GP1 has 4 measurement ports where resistors, inductors or capacitors can be connected. Generally, a ratio measurement happens, which means that e.g. a measuring resistor is set in proportion with a reference resistor. If the measured resistor is changing with temperature, a simple temperature measurement can be done. The same applies for other basic dimensions in electronics such as capacities and inductivities. One can also set them in relation to one another and measure other physical dimensions via time difference measurement.

1.7 High Resolution Mode

Due to it's circuit technique, the TDC-GP1 offers the possibility of combining both channels and therefore double the resolution of the device. This option can be activated via mode registers in the chips. This results in a 1 channel 4-fold multihit TDC with a resolution of approx. 125 ps. The stop 2 input of the TDC is turned off. The measuring possibilities of 1 channel remain according to Fig. 1. Events can still be measured against each other or against the start. If you use the High Resolution Mode in measurement range 2, only a 3-fold multihit capability remains.

1.8 Resolution Adjust Mode

Another important feature of the GP1 is the Resolution Adjust Mode. In this mode the resolution of the TDC is quartz-accurately adjustable to a programmable value and simultaneously for both channels. As a reference for the regulation loop a clock is used which is derived from the external reference clock. The adjustment of the resolution happens via software by setting registers. The resulting resolution is defined by the programmer!

The resolution remains stable due to the changes in the measurement core voltage, which is regulated via PLL (Phase Locked Loop). The external circuit of the PLL regulation needs only a few small and cheap components.

The Resolution Adjust Mode does not posses a start. It works with 2 channels with 4-fold multihit capabilities each. The stop events can be measured against one another. The measurement range of this mode is only the half (2^{14} LSB, about 3.8 µs) which means that between the first and the last stop a time interval of more than 2^{14} LSBs is not permitted.

In this mode the resolution is not dependent on the single units anymore. It is independent of temperature and voltage and absolutely long-term stable. In this mode separate calibration is not necessary.

The range for resolution adjustment can reach values from -30% up to +8% of the normal resolution at 5 V and 25°C. During the entire process the unit can always be queried to check the lock of the regulation loop. If, e.g. the temperature differences are too large or an adjustment is too close to the physical limit of the resolution, the device will automatically switch to the floating resolution mode. It observes the process and switches back to regulation as soon as possible.

In this mode the unit needs more power. In contrast with normal mode the unit needs power also if no measurement is in progress. The necessary power reaches approx. 25 mA, regardless of the measuring rate. Battery operation of the GP1 is very limited in this mode.

The Resolution Adjust Mode also works in the High Resolution Mode. It does not however work in the measurement range 2.

1.9 Calibration

The GP1 can be calibrated via direct command or automatically via start/stop event. During the calibration process the length of one and two periods of the calibration clock are measured in a multihit process. The resulting calibration values are stored in a calibration value register. During a calculation process the main ALU refers to these registers.

A separate calibration process is activated in control register 0 setting bit 7 to '1'. This bit is automatically deleted after the process has ended.

When autocalibration is activated, a calibration run is started after reaching the number of selected hits on both channels. (please regard 'Known problems and solutions')

1.10 Main-ALU and Pre-ALU

The GP1 has 2 arithmetic logic units. In responsibility of the Pre-ALU is the conversion of raw values of the measuring unit, which are available in their own format, into unsigned integer values, so that further arithmetical calculations become possible. A data selection unit is connected in front of this ALU, which is responsible for the selection of the single raw values of the register. The pre-ALU does not need a clock.
The main ALU has several purposes

- Offset correction and subtraction of non-calibrated values
- Calibration of the measured values with the Cal Values
- Multiplication of the calibrated values with a 24-bit integer. The MSB of the multiplication factor has the value 2^0.

All values are channeled through the main ALU. According to the selected operation mode the values will be simply passed, will be calibrated inclusive offset correction, or they will be multiplied with a factor < 2.

The main ALU has it's own clock generator that makes it independent of external clocks. The calculation time for one calibration takes approx. 2µs, for an adjoining multiplication also approx. 2µs, so that approx. 4 µs are needed for a complete cycle. The frequency of the clock generator can be adjusted. The main ALU is a 16 bit ALU.

1.11 Result registers

The main ALU stores the measurement results into the result registers (8 registers at 16 bit). Only result register values can be read out via microcontroller interface. An uncalibrated measured value (which is possible only in measurement range 1/resolution adjust) occupies 1 register. A calibrated and perhaps multiplied value occupies 2 registers. This means that 8 uncalibrated or 4 calibrated values can be stored in the GP1. Single registers or all registers can be read out at any time without destroying or promoting specific actions.

The values are rotated and stored in register 0 through 7. If a further calculation process is started after the values were stored already into the top register, the new value will be stored in the lowest register. Since the micro-controller interface can activate numerous calculation processes, it is possible to perform many calculations of time differences between various hits without limitation by the number of output registers of the GP1.

1.12 Control and value registers

The following registers are available from GP1
Write:

- 7 control registers 8 bit each
- 4 value registers 8 bit each, 3 for the multiplication values and one for the adjust value of the PLL in the Resolution Adjust Mode

Read:

- 8 value registers for the measurement results
- 2 status registers (read only)
- 1 value register (read only) for the PLL adjust value proposal (Resolution Adjust Mode)

The registers are read out and stored via micro-controller interface

1.13 Microcontroller interface

The GP1 offers a standard 8-bit micro-controller interface. The values are stored and read out via the following signals

- WRN
- RDN
- CSN
- ALE

The addressing happens via a 4 bit address bus. The architecture of the interface is realized with target on familiar and common standards. The data bus and the address bus realized with separate pins. The pins can however be connected. Also, a '1' at the ALE input makes the internal address latch transparent so that the register can receive addresses directly. The data bus is bi-directional, the address bus unidirectional.

While reading the value registers an internal counter is responsible for the automatically address increment as long a the addresses remain unchanged. By simply setting the reading counter in the appropriate space and the appropriate number of reads, the measured values can be read out very simply. However, one can also jump to another measured value by setting the address pointer to a new value. A status register can be read out at any time if directly addressed. An automatic incrementation does not happen here.

1.14 Miscellaneous functions of the GP1

a. Auto Noise Unit

The GP1 has a unit that adds a pseudo-random offset to the stop hits. The same offset is also added in the following calibration measurements. While measuring very stable time intervals this noise effect can achieve a suppression of the quantifying effects. A weighted average of several measured values becomes necessary. Single events are not effected in their precision. The Auto Noise Unit makes no sense in the Resolution Adjust Mode because the required effect is given automatically in this mode of measurement.

b. Adjustable edge sensitivity

The edge sensitivity of the start input and the stop input can be adjusted via mode register.

c. Channel enable

Every stop input can be disabled via external pins. This permits the control of a channel by adding external logic e g . Any number of hits can be faded out.

d. Spike suppression for RDN and CSN

In case of a rough and disturbing environment it makes sense to limit the border frequency of the RDN and CSN signals so that spikes in the wires can be suppressed. This can be adjusted by the GP1 via mode register. If the **S**pike **S**uppression **I**nterface is activated spikes can be suppressed for up to 6 ns. Without spike suppression such pulses - depending on their length - are either read by the GP1 or identified as a chip select signal. As a result false values may be stored in the register or the is retracted by mistake.

By activating the SUI interface the timing in the interface becomes slower. This should be taken into consideration.

e. Half Resolution

Physically seen the GP1 has a relatively bad differential non-linear characteristic in normal or double resolution. This doesn't affect most applications. In some applications however (especially those involving physical experiments) a small differential non-linear characteristic is of great importance.

The characteristics of the digital TDC-principle used can be positively exploited. The differential non-linear characteristics are strictly periodical with period 2. This means that a narrow LSB is always followed by a wide LSB and vice versa. By combining 2 LSBs one can improve the non-linear characteristics by a lot. This is why the TDC-GP1 offers the option of dividing the resolution in half. The result is no more than a division by 2 of the uncalibrated measuring results.

f. Retriggerability

If, during a measurement, more than one start pulse arrives (without retrigger) all starts after the first start will be ignored. This may not be convenient for all applications. It would sometimes be better if the last start could be measured against the stops. This option is however available in the Retrigger mode.

If more than one start arrives in retrigger mode without being intervened by a stop, every start initializes the measuring unit. As soon as the first stop arrived on one of the two channels, additional start pulses will be ignored. If the measurement unit overflows after a start and a second start arrives, the measurement unit will also be initialized again and a new measuring process will begin.

This mode is not applicable in the measurement range 2 or in the Resolution Adjust Mode.

2. Details of the GP1

2.1 Foreword

The goal of the main section is to describe to the user all possible settings of the GP1. Every possible function is explained in detail here. The appropriate adjustment of the register is explained as well as the functions of important registers including their complete content. The combination of the single features will be explained in detail as far as possible. This section of the manual is an absolute must for anyone who plans to design-in a GP1 or to write software for.

In order to understand the functions of a GP1 it is important to understand the register structure (please see the principle circuit diagram)

a. Raw Value Registers

2*6 raw value registers (15 bits) per channel. The resulting values of the measured unit are directly stored in this register. With the exception of the Resolution Adjust Mode all values are uncalibrated, meaning they are depending on production loss, voltage and temperature. Two of these 6 registers are reserved for calibration values.

b. Result Registers (read only)

8 result registers with 16 bit. These registers are written on by the sequential ALU according to the set calculation mode. One register is necessary for uncalibrated values which are derived directly from the raw values or from the differences of raw values. Two registers are necessary for calibrated values. The result register is continuously written on in a circular manner, after writing to the 8th register the ALU will continue with writing to register one.

c. Control Registers, Value Registers (write only)

7 control registers, where different process modes and other possibilities can be adjusted, and 4 value registers for the multiplication factor and the PLL adjustment factor.

d. Status Registers (read only)

2 status registers where important status parameters of the GP1 can be read from.

f. Value Register (read only)

The PLL in the Set Parameter Mode stores the evaluated division factor for the PLL in this register. This value is helpful for orientation, when resolution adjust is in use.

2.2 The Read- and Write Registers of GP1

The control registers in tabular form with short explanations

2.2.1 Write registers and addresses

Important remark: The write registers cannot be read.

Control register 0
Address: 0

Bit No.	Name	Description	Default
7	CAL	initializes a separate cal run → updates the cal values in the raw value registers	0
6	CALIBRATE	Instructs the ALU to carry out a calibration calculation	0
5	MULTIPLY	Instructs the ALU to carry out a multiplication	0
4	MESSB2	switches to measurement with predivider, 1= with predivider	0
3	EN_CAL_AUTO	1= automatic calibration after measurement	0
2	EDGE_STP2	selects edge sensitivity Stop2 - 0=rise	0
1	EDGE_STP1	selects edge sensitivity Stop1 - 0=rise	0
0	EDGE_STA	selects edge sensitivity Start - 0=rise	0

Remark: optimum value for ADJ<5:0> = 0x0d

Control register 1
Address: 1

Bit No.	**Name**	**Description**	Default
7	RESO_ADJ	switches to resolution adjust mode	0
6	HIGH_RES	switches to high resolution mode	0
5	ADJ<5>	Adjustbit 5 of HIGH RES Mode	0
4	ADJ<4>	Adjustbit 4 of HIGH RES Mode	0
3	ADJ<3>	Adjustbit 3 of HIGH RES Mode	0
2	ADJ<2>	Adjustbit 2 of HIGH RES Mode	0
1	ADJ<1>	Adjustbit 1 of HIGH RES Mode	0
0	ADJ<0>	Adjustbit 0 of HIGH RES Mode	0

Control register 2 **Instruction register for ALU**
Address: 2 **Calculation Instruction: HIT1_IN - HIT2_IN**

Bit No.	**Name**	**Description**	Default
7	HIT2_IN<3>	Channel Select for upper Nibble: 0= channel1, 1=channel2	0
6	HIT2_IN<2>	#Hit for channel selected in bit 7	1
5	HIT2_IN<1>	#Hit for channel selected in bit 7	0
4	HIT2_IN<0>	#Hit for channel selected in bit 7	1
3	HIT1_IN<3>	Channel Select for lower Nibble: 0= channel1, 1=channel2	0
2	HIT1_IN<2>	#Hit for channel selected in bit 7	1
1	HIT1_IN<1>	#Hit for channel selected in bit 7	0
0	HIT1_IN<0>	#Hit for channel selected in bit 7	1

Control register 3 **Control register for resolution in resolution adjust mode**
Address: 3

Bit No.	**Name**	**Description**	Default
7	FAK_PLL<7>	MSB division factor of PLL	1
6	...	...	0
5	...		0
4	...		0
3	...		0
2	...		0
1	...	...	0
0	FAK_PLL<0>	LSB division factor of PLL	0

Control register 4
Address: 4

Bit No.	**Name**	**Description**	Default
7	SEL_CLK_TDC<2>	Factor for calibrating clock of TDC (Table in 2.11.3)	0
6	SEL_CLK_TDC<1>	...	0
5	SEL_CLK_TDC<0>	...	0
4	NEG_PH_PLL	Negotiation of phase output of PLL (has to be '1'if the recommended circuit is used)	0
3	SET_PAR_PLL	1=Track mode of PLL (Set Par Mode)	0
2	SEL_CLK_PLL<2>	Factor for reference clock of PLL (Table in 2.11.3)	0
1	SEL_CLK_PLL<1>	...	0
0	SEL_CLK_PLL<0>	...	0

Control register 5 **RLC-Configuration register**
Address: 5

Bit No.	**Name**	**Description**	Default
7	RLC_NR<2>	Attitude which one or how many RLC ports will be measured	1
6	RLC_NR<1>	"	0
5	RLC_NR<0>	"	0
4	SINGLE_EN	Measure selected ports = 1, 0= all Ports (1 to RLC_NR)	0
3	C_SEL	Measure capacity ratios = 1	0
2	SEL_CLK_RLC<2>	Factor for clock of RLC unit	0
1	SEL_CLK_RLC<1>	"	0
0	SEL_CLK_RLC<0>	"	0

Control register 6
Address: 6

Bit No.	**Name**	**Description**	Default
7	INT_SEL	Interrupt Select (0= ALU ready, 1= Overflow)	0
6	QUEUING	Enable queuing in measurement range 1	0
5	RETRIG_EN	Enable retrigger mode	0
4	NOISE_EN	Noise enable	0
3	RLC_EN	Starts RLC measurement	0
2	USE_TRANS	1= Use of an external transistor at RLC Unit	0
1	SPEED<1>	Frequency setting BIGALU clock (default: lowest speed)	1
0	SPEED<0>	(see also 2.9.8)	0

Control register 7
Address: 7

Bit No.	**Name**	**Description**	Default
7	HALF_RES	Half resolution of measuring circuit	0
6	EN_SUI	Enable spike suppression RDN	0
5	EN_HIT2<2>	Number of the possible hits on channel 2 (max. 4)	1
4	EN_HIT2<1>	"	0
3	EN_HIT2<0>	"	0
2	EN_HIT1<2>	Number of the possible hits on channel 1 (max. 4)	1
1	EN_HIT1<1>	"	0
0	EN_HIT1<0>	"	0

Registers 8-10
Address:8-10

		Default
Register 8	Multiplication factor <7..0>	0
Register 9	Multiplication factor <15..8>	0
Register 10	Multiplication factor <23..16>	128

Address 11: Special Address for Init

Bit No.	Name	Description
7	POR.	Power On Reset (1)
6	POR.	Power On Reset (0)
5	POR.	Power On Reset (1)
4	POR.	Power On Reset (0)
3	n.c.	
2	CLK_NOISE	Clock for PRBS counter in auto noise unit
1	INIT_BIGALU	Init for Bigalu unit
0	INIT_TDC	Init for TDC unit

2.2.2 Read registers and addresses

The GP1 has the following read registers:

Address	Name	bits	Description	with calibrated data
0	ERG_REG0	16	Result register 1	Fractional portion 0
1	ERG_REG1	16	Result register 2	Integer portion 0
2	ERG_REG2	16	Result register 3	Fractional portion 1
3	ERG_REG3	16	Result register 4	Integer portion 1
4	ERG_REG4	16	Result register 5	Fractional portion 2
5	ERG_REG5	16	Result register 6	Integer portion 2
6	ERG_REG6	16	Result register 7	Fractional portion 3
7	ERG_REG7	16	Result register 8	Integer portion 3
8	STAT1	8	Status register 1	
9	STAT2	8	Status register 2	
A	REF_PLL	8	Register for reference value of the PLL that is won on a SET_PAR run	

Occupancy of status registers:

Status register 1
Address: 8

Bit No.	Name	Description
7	PLL_LOCK	Lock indication of the PLL
6	OFL	Overflow indication of measurement unit
5	HIT2_TDC<2>	Indicates number of present hits in channel 2
4	HIT2_TDC<1>	Indicates number of present hits in channel 2
3	HIT2_TDC<0>	Indicates number of present hits in channel 2
2	HIT1_TDC<2>	Indicates number of present hits in channel 1
1	HIT1_TDC<1>	Indicates number of present hits in channel 1
0	HIT1_TDC<0>	Indicates number of present hits in channel 1

Status register 2
Address: 9

Bit No.	Name	Description
7	N.C.	not used
6	N.C.	not used
5	RLC_END	End of a RLC measurement
4	Multiply	Indication of multiplication (=Bit5 ofRegister0)
3	Calibrate	Indication of calibration (=Bit6 of Register 0)
2	LD_REGS<2>	pointer position in result register
1	LD_REGS<1>	pointer position in result register
0	LD_REGS<0>	pointer position in result register

2.2.3 Explanations of read registers

2.2.3.1Data structure of the result registers

As one can see from the table above the GP1 has 8 result registers (ERG_REG0 ... ERG_REG7) with 16 Bit each.

The data structure and the occupancy of the registers is dependent on whether calibrated or non-calibrated data are stored. For non-calibrated data one result register gets occupied. For calibrated data 2 result registers are needed. In this meaning non-calibrated data include also results that are measured in resolution adjust mode.

Data structure of non-calibrated data

To get non-calibrated data one has to set bit 6 (Calibrate) of control register 0 to '0'.

Non-calibrated data are of the type 'Signed Integer'. The numbers are available in complements of 2.

Examples:

Register content	*resulting value*
0x0ABC	*2748*
0xC002	*-16382*
0x7073	*28787*
0xFF12	*-238*

Data structure of calibrated data

Calibrated data are fixed point numbers with 16 bits integer portion and 16 bits fractional portion.

Any calibrated result covers therefore 2 result registers. The fractional portion is in the lower registers and the integer portion digits in the upper ones.

Examples:

Register contents	*resulting value*	*Integer portion.Fractional portion*
0x0001.ABCD	*1.671096*	*(result of: 1+43981/65536)*
0xFFFE.1234	*-1.071105*	*(only in measurement range 1)*
0x0067.A001	*103.62501*	*(possible only in measurement range 2)*
0xD002.A001	*53250.62501*	*(possible only in measurement range 2)*

From the examples it's obvious that several cases must be distinguished:

- only in measurement range 1 negative results are possible.
- in measurement range 2 only positive results are possible, given as unsigned numbers
- without multiplication, the result in measurement range 1 cannot be bigger than ± 1.99 as it is not possible to calibrate time differences bigger than twice the period of the calibration clock.

2.2.3.2 Reading the result registers

While the status registers and the PLL register are read by standard memory mapping, a quite different procedure is used for the result registers.

The following in principle applies to result registers:

Multiple results can be read by selecting the start address and sequentially reading data. An internal address pointer is increased by one after reading if the external address is held constant. To read a result always two 2 read strobes are necessary (without a change of the address). At the 8-Bit bus first the LSByte appears and afterwards the MSByte.

Examples:
1. Reading of all 8 result registers
Procedure: Put the address 0 and attaching 16 read strobes. Now all result registers will be read from LSByte to MSByte.
2. Reading of result register 1 and 3
Procedure: Put address 1 and two read strobes; then put address 3 and two read strobes.

2.2.3.3 Explanations of status registers

Status register 1

Bit 0-5

The signals HIT1_TDC<2:0> and HIT2_TDC<2:0> show the number hits present on each channel. It is possible for numbers of 0 to 4 respectively. These hit counters increment as soon as the hits are registered by the measuring unit. At the time of the registration these hits cannot be read, they have to be transferred with ALU operations to the result registers.

Bit 6

Bit 6 indicates an overflow of the measuring unit. I. e. This bit is set to '1' if, during a measurement with a fixed number of allowed hits, the maximum time difference is broken.

Bit 7

In resolution adjust mode this bit signals that the PLL has locked and the chosen resolution is set.

Status register 2

Bit 0-2

These bits indicate to which address of the result register the address pointer shows. I.e. if it points to '4' then the addresses 0 -- 3 already contain results, four 16-bit results or two 32-bit results are available.

The value '0' has two meanings: that there is no result or that there are eight 16-bit results. If the interrupt flag (Pin 34) is set to '0' this flag can be used to decide whether there is no result or 8 results. If INTFLAG is '1' there are 8 readable results present.

Bit 3 and 4

These two bits show whether the ALU is prepared for calibration and/or multiplication. They directly reflect the content of bits 5 and 6 of the control register 0. Setting and Reading these bits can be used as a simple test for the microprocessor interface.

Bit 5

Bit 5 indicates the end of an RLC-measurement.

2.2.4 Initialization

Before starting a measurement, independently of the chosen measurement mode, an initialization of the chip is necessary. In the most elementary case this initialization is a Power On Reset. The GP1 has a comfortable Init command that offers several possibilities of the initialization. The Init command is explained by the table following:

Address 11: **Special address for Init**

Bit No.	Name	Description
7	POR.	Power On Reset (1)
6	POR.	Power On Reset (0)
5	POR.	Power On Reset (1)
4	POR.	Power On Reset (0)
3	n.c.	
2	CLK_NOISE	Clock for PRBS counter in auto noise unit
1	INIT_BIGALU	Init for Bigalu unit
0	INIT_TDC	Init for TDC unit

- **Init of the GP1 internal measurement unit**

The internal TDC unit is initialized with the INIT_TDC. The hit counter is set to '0', a possible timeout is deleted. The unit is ready for measurement again with the attitudes chosen before. The TDC unity is ready for measurement 30 ns after the positive edge of WRN.

- **Init of the sequential ALU**

The sequential ALU is initialized with INIT_BIGALU. The write pointer is set to '0' means to the first result register, The unity is ready again with the attitudes chosen before. 30 ns after the positive edge of WRN the BIGALU is ready again for calculation.

- **Init of the Auto Noise Counter**

When bit 2 is set to '1' the random counter of the auto noise unit is incremented, independently of whether this unit is enabled or not.

- **Power On Reset**

The Power On Reset is executed with a hex 'A' on the top nibble of the data bus. The entire chip is then set in it's basic state, all control and value registers will be initialized in their default values.

The raw value register of the TDC measuring unit and the result registers of the BIGALU can generally not be initialized. They also remain unchanged during a Power On Reset.

The Power On Reset can also be activated via the RST_N pin with the same effect. This pin is 'low active' (min. duration 50 ns). In case that a Power On Reset is activated via software, additional commands can not processed within 50 ns after a positive edge of the WRN signal because the GP1 is in reset mode at this time.

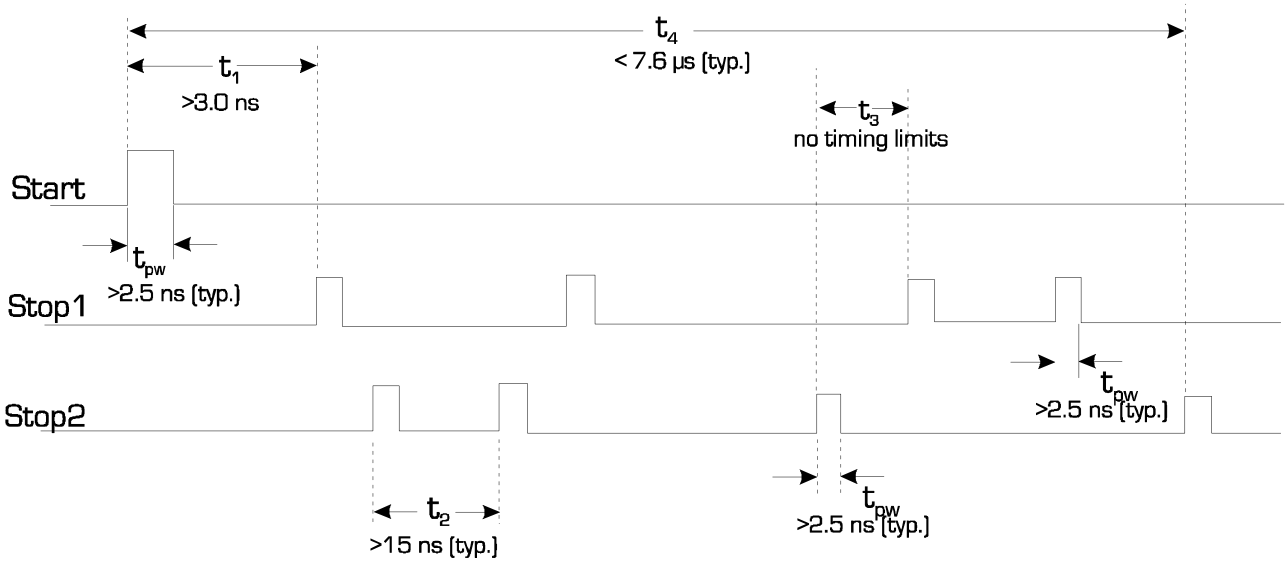
2.3 Measuring in measurement range 1

Adjustment of the measurement range:

Relevant Register:	Control register 0	Address: 0
Relevant Bits:	4	
Effect:	0 = Measurement range 1; 1 = Measurement range 2	
Default:	Measurement range 1	

2.3.1 Possible measuring sequences and timings

Figure 4: Timings measurement range 1



The measurement mode 1 offers a 2 channel TDC with common start and 4-fold multihit capabilities per channel. Figure 4 displays a typical measuring series.

The measuring unit for both channels is started by the sensitive edge of the start pulse. Every channel can receive four independent stops. The times of the events in relation to the common start are stored in 4 raw value registers on each channel. The following timings should be noted (typ.):

- a stop can be received at the earliest 3 ns after the start is activated. Stops that arrive earlier will be ignored → $t_{1\,min} = 3$ ns
- at least 15 ns must lie between 2 events on the same channel (double pulse resolution). If two events are closer, the second event will not be identified because it arrived during the channels recovery time. → $t_{2\,min} = 15$ ns
- there are no restrictions or minimum time differences regarding 2 events on different channels → $t_{3\,min} = 0$ ns
- all measured events must arrive within 30.720 LSBs (2^{15}-2^{11}) after the start → $t_{4\,max} \approx$ 7,6 µs (typ.)

- the minimum pulse width for the start input and the stops inputs is

  → t_{pw}= 2,5 ns (typ.)

  The minimum pulse width is the same for all operation modes and for positive and negative pulses

2.3.2 ALU control in measurement range 1

The detailed description of all the possibilities of the ALU is represented in section 2.9 further behind in this manual. Here a summary for measurement range 1.

In measurement range 1 it is possible to
- measure each stop on both channels against start
- measure the stops against each other
- calibrate and/or multiply the result optionally

The content of register 2 controls which events are measured against each other. It exists of two control values each 4 bit long (Nibbles). The calculation rule

Result = Lower nibble - Upper nibble

is used.
Whether it will be calibrated and multiplied is fixed in control register 0.

Some examples for clarification (for detailed explanations see section 2.9)

Example 1:
Content register 0: 0x60
Content register 2: 0x01

Result: The first hit in channel 1 minus start is calculated, the result is calibrated and multiplied and written to result registers with 32bits. The complete calculation cycle lasts about 4.2 µs. Make sure that the measurement result is not bigger than twice the cycle duration of the calibration clock. Otherwise the ALU will overflow.

Example 2:
Content register 0: 0x00
Content register 2: 0xA3

Result: The 2nd hit of channel 2 is subtracted from the 3rd hit of channel 1. The result is written to the result register with 16 bit. The complete calculation cycle lasts about 180 ns.

2.3.2 Control of the measurements, adjustment possibilities

There are several possibilities of controlling and evaluating a measurement series.

Practically all adjustment possibilities can also be used for the other measuring modes. Please regard following advice:

- **Enable the number of hits**

Relevant register:	Control register 7	Address: 7
Relevant Bits:	5-0	
Effect:	see table	
Default:	4 hits per channel	

The number of possible hits can be adjusted in the control register 7 (address 7). The following adjustments should be made:

EN_HITx<2>	EN_HITx<1>	EN_HITx<0>	Number of possible hits
0	0	0	0 Hits, Software Disable of channel
0	0	1	1 Hit
0	1	0	2 Hits
0	1	1	3 Hits
1	0	0	4 Hits

If both channels are set to 0 hits the entire measuring unit is disabled and a start will be ignored. This is valid for all measurement modes.

- **Adjustment of edge sensitivity**

Relevant Register: Control register 0 Address: 0
Relevant Bits: 2-0
Effect: 0 = rise; 1 = fall
Default: rise

This adjustment can independently be used for all measuring modes.

- **Retrigger Mode**

Relevant Register: Control register 6 Address: 6
Relevant Bits: 5
Effect: 0 = off; 1 = on
Default: off

Every start initializes the measuring unit from the beginning until the first stop arrives. The new start is then considered the beginning of the measurement sequence (a different process happens without retrigger: further starts are ignored after the first start activated the measurement unit). After the first stop is activated on any of the two channels additional starts will be ignored. This enables numerous starts without intervening stops and to measure the last start against the stops.
The retrigger mode makes sense only in measurement range 1. It must be deactivated in measurement range 2 and also has no effect in Resolution Adjust Mode.
In retrigger mode the minimum time from start to a stop is redefined to

→ $t_{1\,min} = 6$ ns

See 5.3 Known problems and solutions: Retrigger

- **Queuing**

Relevant Register: Control register 6 Address: 6
Relevant Bits: 6
Effect: 0 = off; 1 = on
Default: off

Queuing is considered the ability of using the available hits of both channels with only one stop. If queuing is enabled the second stop input is disabled. If the stop 1 input receives more than 4 stops, the stops will be switched to channel 2. The result is a 1 channel TDC with 8-fold multihit capability.

Queuing is also possible in the Resolution Adjust Mode, not in the measurement range 2.

- **Auto Noise**

Relevant Register: Control register 6 Address: 6
Relevant Bits: 4
Effect: 0 = off; 1 = on
Default: off

The Auto Noise Unit adds an offset delay to stop 1 and stop 2, which is controlled via a pseudo-random generator. The delays of the stop inputs are independent of each other so that the delay between the stops is varying.

The meaning of this adjustment possibility:

If you wish to improve your measuring results by averaging as it is possible in numerous measuring series, it is necessary that the averaged values do not always display exactly the same time difference. Instead they should provide some 'noise' so that different steps of the characteristic curve of the GP1 are involved. This can not happen with very constant time differences. One would constantly hit the same LSB.

Example: *While measuring a quartz-accurate clock an increase in accuracy via averaging is not possible without Auto Noise since the measured time difference is practically always the same. As a result the same LSB is constantly hit.*

An auto noise unit which is part of the input circuit enables the use of weighted averaging, even for constant time differences. This auto noise unit adds an offset to the characteristic curve. The alteration is controlled via a 7 bit pseudo-random numerical generator. The length of the alteration is several LSBs.

The clocking of the random generator and - as a result - the generation of a new offset value is initialized setting bit 3 in register 11 to '1'. Otherwise the offset value is kept unchanged. This gives all the flexibility to the user he needs when using this option.
The offset must be kept constant during the calibration cycle that belongs to the measured value. This is automatically guarantied when autocalibration is in use. With a separate calibration it must be controlled directly.

Auto Noise is also applicable in measurement range 2. This option makes no sense in Resolution Adjust Mode and should therefore be turned off.

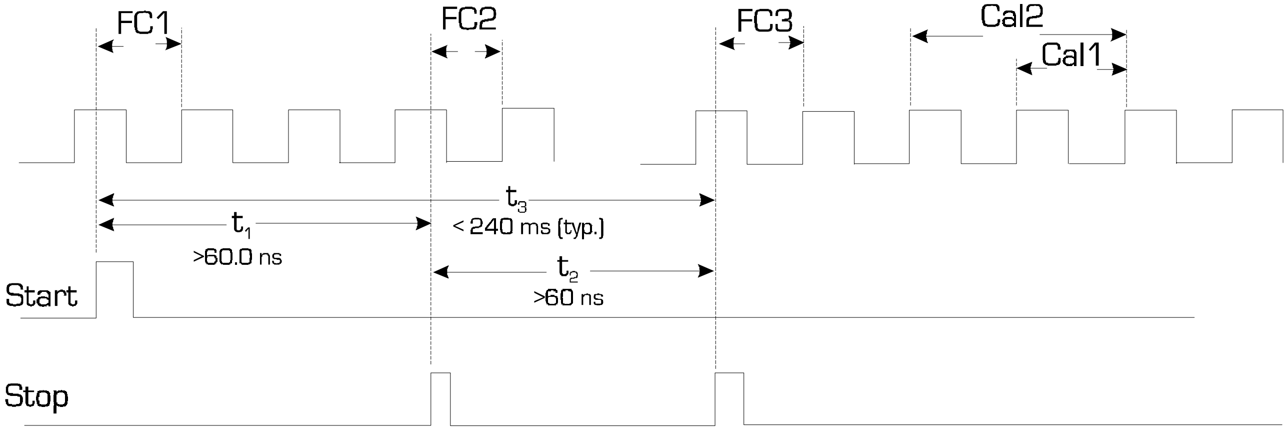
2.4 Measuring in measurement range 2

Adjustments in the measurement range:

Relevant Register:	Control register 0	Address: 0
Relevant Bits:	4	
Effect:	0 = Measurement range 1;	1 = Measurement range 2
Default:	Measurement range 1	

2.4.1Possible measuring sequences and timings

Figure 5: Timings measurement range 2



$$time = period * \left(cc + \frac{FC1 - FC2}{Cal2 - Cal1} \right), \; cc = value\ of\ the\ precounter$$

A predivider principle is of great advantage for measurements of large time intervals. In this mode the time interval isn't measured directly. The TDC measures the time difference between the start pulse and the next rising edge of the calibration clock. This leads to finecount FC1. Now a counter begins to count the periods of the predivider until the stop pulse arrives. The stop edge restarts the measuring unit and the next edge of the calibration clock stops it. This leads to finecount FC2. If more than 1 stop arrive, the following stops will be handled like FC2. According to the formula in Figure 5 the measured time interval can be calculated, using existing calibration values or calibrated values generated after the measuring process. The GP1's predivider is 16 bits wide. This allows to measure large time intervals > 200 ms with the high resolution of the TDC and corresponds to 30 bit dynamic range.

When using measurement range 2 only one channel is available. The stop 1 input is active. This channel has 4-fold multihit capability in normal resolution. No time differences between stops can be calculated, only against the start event.

The following timings should be noted:

- a stop can arrive 1.5 calibration clock periods +25 ns after the start at the earliest. Stops that arrive earlier will be ignored **→ t_{1min} = 1.5 * CAL_CLK + 25ns**
- at least 1.5 calibration clock periods +25 ns must lie between two stops. If 2 stops are closer together, the second stop will not be recognized.
  → t_{2min} = 1.5 * CAL_CLK + 25ns
- all measured stops arrive must within 2^{16} calibration clock periods
  → t_{3max} = 2^{16} * CAL_CLK

The calibration clock is derived from the external reference clock in combination with the calibration clock divider (register 4, bits 5-7).

CAL_CLK = T_{ref}*SEL_CLK_TDC.

The higher the value for the clockdivider, the larger is the measurement range $\mathbf{t_{3max}}$ and the worse is the double pulse resolution $\mathbf{t_{2min}}$.

Example 1:		*Example 2:*	
Reference clock 20MHz: T_{ref}	*= 50ns.*	*Reference clock 20MHz:* T_{ref}	*= 50ns.*
Calibration clock divider	*= 64*	*Calibration clock divider*	*= 1*
$\Delta t_{max} = 50ns*64*2^{16}$	*= 209.7ms*	$\Delta t_{max} = 50ns*1*2^{16}$	*= 3.277ms*
$\Delta t_{max} = 1.5*50ns*64+24ns$	*= 4824ns*	$\Delta t_{max} = 1.5*50ns*1+24ns$	*= 99ns*

A time interval bigger than 200 ms can be measured with undiminished resolution of the GP1 using a lower frequency calibration clock. One should however acknowledge that the absolute precision of the measured time difference is dependent upon the calibration clock.
The upper limit of the measurement range is defined as

2*T_{ref}*SEL_CLK_TDC < 30.720*Resolution (≈7.6µs).

Behavior of the GP1 at too small time intervals: A time difference that is smaller than (1.5*CAL_CLK + 25 ns) cannot be measured with safety. The behavior of the GP1 can be described like this: time intervals between (0.5*CAL_CLK+25 ns) and (1.5*CAL_CLK+ 25ns) may be measured depending on the phase relationship between the start/stop pulses and the calibration clock. The probability that the value still can be measured decreases at sinking time intervals. Below (0.5*CAL_CLK + 25ns) no stop is recognized. It is important to know that no wrong results will occur. If it happens, that a time difference is measured, this will be correct. In case the time difference isn't measured the related stop is ignored an the measuring unit still continuos waiting for stops. If no further stop arrives an overflow of the measuring unit will be indicated.

2.4.2 Occupancy of raw value registers with measured values

In order to fully understand several adjustments in measurement range 2 and to successfully control this measurement mode it is absolutely necessary to be aware of how the raw value registers are occupied with measured values.

Each of the two measuring channels has 4 raw value registers where uncalibrated values of the measuring unit can be stored. These registers are occupied in measurement range 2 as follows:

For completeness the 'High Resolution' Mode is displayed as well.

Channel	Raw Value register	Stored values in measurement range 2	
		Normal	High Resolution
1	1	FC 1	FC 1
1	2	FC 2	FC 2
1	3	FC 3	FC 3
1	4	FC 4	FC 4
2	1	FC 5	FC 1
2	2	n.c.	FC 2
2	3	n.c.	FC 3
2	4	n.c.	FC 4

2.4.3 ALU control in measurement range 2

The detailed description of all the possibilities of the ALU is represented in section 2.9 further behind in this manual. Here a summary for the measurement range 2.

In measurement range 2 it's possible to

- measure the stops against start.

- multiply the result.

It's not possible to measure the stops against each other.

Only calibrated results can be given out. Always the calibrate bit in register 0 must be set.

The control of which event is calculated against start is done in control register 2. It exists of 2 control values each of 4 bit (Nibbles). The calculation rule is

Result = Lower nibble - Upper nibble.

The ALU must be instructed in a way, that for the desired hit the correct finecounts are subtracted according to the formula

$$\boxed{\Delta t = CAL\_CLK * \left(CC + \frac{FC1 - FC2}{Cal2 - Cal1} \right)}$$

Some examples for clarification (For a detailed description see section 2.9)

Example 1:
Content register 0: 0x50
Content register 2: 0x21 → FC1 - FC2

Result: The time difference between the first hit and start is calculated, the result is calibrated and written to the result register with 32 bit. The complete calculation cycle lasts about 2.2 µs.

Example 2:
Content register 0: 0x50
Content register 2: 0x91 → FC1-FC5

Result: The time difference between the 4th hit and start is calculated, the result is calibrated and written to the result register with 32 bit. The complete calculation cycle lasts about 2.2 µs.

2.4.4 Control of the measuring

- **Enable number of hits**

Relevant Register:	Control register 7	Address: 7
Relevant Bits:	5-0	
Effect:	see table	
Default:	4 hits per channel (valid only in measurement range 2)	

EN_HIT1<2..0>	EN_HIT2<2..0>	No. of Hits
2	0	1
3	0	2
4	0	3
4	1	4

The 2 finecount values (FC1 and FC2) are necessary for the generation of the measured values. For every further hit an additional FC value will be generated. The FC1 value is necessary for the start pulse and therefore for every measurement.

- **Adjustments of edge sensitivity**

Adjustments identical with measurement range 1, please see 2.3.4!!!

- **Retrigger Mode**

This mode can not be used in measurement range 2. It is absolutely necessary to turn it off!!!!

- **Queuing**

Queuing has no effect in measurement range 2.

- **Auto Noise**

The Auto Noise Unit functions like in measurement range 1. The only difference is that while using the Auto Noise Unit no 4-fold multihit capability but only 3-fold multihit is given.

ATTENTION: The fourth hit is permitted and will also be accepted. However, since the FC 5 value is found in the second channel, a different offset value is valid. The ALU doesn't take this into account. The results errors are even greater than measuring errors.

The Stop-Enables (pins 37, 42) must be activated for the duration of the measurement.

Please note:
Auto Noise only makes sense in measurement range 2 when the start pulse is rigid in phase to the calibration clock. If the start pulse and calibration clock have no specific phase relation the Auto Noise becomes unnecessary. It practically occurs by itself.

2.5 Measuring in the Resolution Adjust Mode

Adjustments of the measuring mode

Relevant Register: Control register 1 Address: 1
Relevant Bits: 7
Effect: 0 = off 1 = on
Default: off

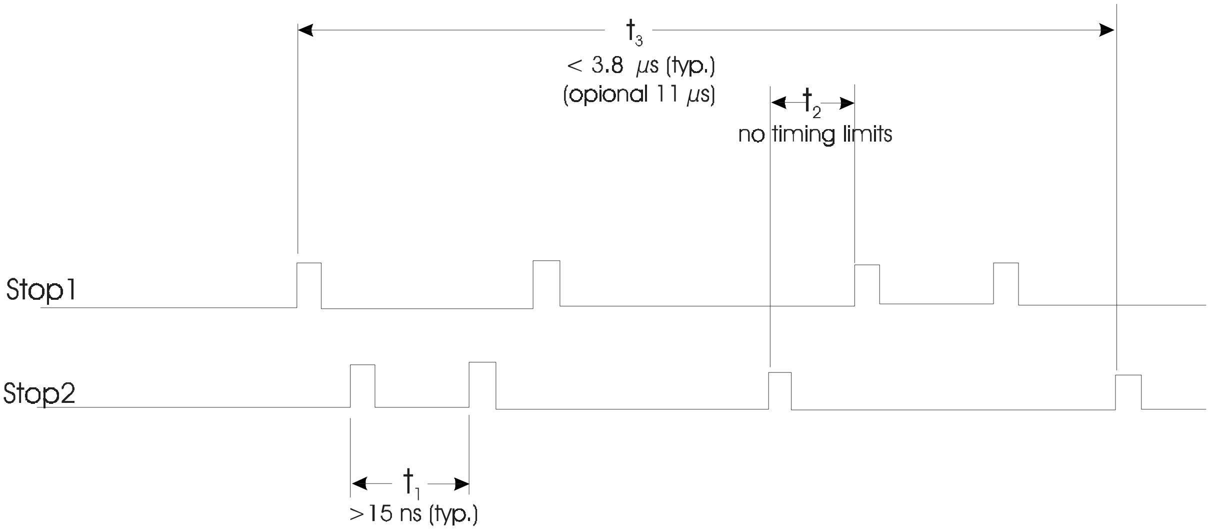
In principle the high resolution of the GP1 is derived from the internal 'gate propagation times'. The gate propagation time is dependent upon voltage, temperature and the manufacturing process. Due to this dependency the resolution of the GP1 is not known and must first be calculated via calibration measurements. In addition, the resolution is not stable, it sways with voltage and temperature. This does not apply in the Resolution Adjust Mode of the GP1. In this mode the resolution of the GP1 can be adjusted quartz-accurately and absolutely temperature stable via Phase Locked Loop. The Phase Locked Loop regulates the core voltage of the GP1 so that the resolution is set exactly to the value programmed.

The Resolution Adjust Mode can be used in measurement range 1 during normal resolution as well as with High Resolution (Please see the limits given in the following section).

2.5.1 Possible measuring sequences and timings

The Resolution Adjust Mode works without the start input. The reason is that the measuring core can principally be found in a different operating mode. The measurement core is working all the time. The first stop pulse that arrives, whether on channel one or two, will be interpreted as start.

Figure 6: Timings resolution adjust mode



The following timings must be noted:

- there must be at least 15 ns time difference between 2 events on the same channel (double pulse resolution). If the events are closer, the second event won't be recognized because it arrives during the recovery time of the channel

  Measurement range1: $t_{1\,min}$ = 15 ns (typ.)
- no minimum time difference is required between 2 events on different channels

  Measurement range1: $t_{2\,min}$ = 0 ns (typ.)
- all measured events must arrive within 15.360 LSBs (2^{14}-2^{11}) after the first event on one of the stop inputs

  Measurement range1: $t_{3\,max} \approx$ 3,8 µs (typ.)

2.5.2 ALU control in Resolution Adjust Mode

A detailed description of all the possibilities of the ALU is represented in section 2.9 further behind in this manual. Here a summary for the resolution adjust mode.
In resolution adjust mode it's possible to measure all stop events of both channels against each other.
It's not possible to calibrate or multiply.

The control of which events are measured against each other is done in register 2. It exists of two adjustment values each 4 bit long (Nibbles). The calculation rule is:

Result = Lower nibble - Upper nibble.

Some examples for clarification (For details see section 2.9)

Example 1:
Content register 0: 0x00
Content register 2: 0x21

Result: The 2nd hit on channel 1 is subtracted from the first hit on channel 1, the result is written to the result register with 16 bit. The complete calculation cycle lasts about 180ns.

Example 2:
Content register 0: 0x00
Content register 2: 0xA3

Result: The 2nd hit of channel 2 is subtracted from the 3rd hit on channel 1, the result is written to the result register with 16 bit. The complete calculation cycle lasts about 180 ns.

2.5.3 Limits in Resolution Adjust Mode

For Resolution Adjust Mode the following restrictions apply. Please note:

- **Measurement range 2 is not allowed**

The Resolution Adjust Mode can only be used in measurement range 1. No effective measurements are possible in measurement range 2. Since the construction of the measurements in measurement range 2 always demands a normalization (i.e. a calibration), a similar calculation also becomes necessary in the Resolution Adjust Mode, which would dissolve the positive effect of this mode.

- **No calibration value generation possible**

In the Resolution Adjust Mode a calibration value generation is not possible and also not necessary.

- **No calibrate or multiply of the ALU**

In this mode it is not possible for the ALU to perform a calibration. Multiplication can be done if the calculated value is positive.

- **The measurement range is only half as large as without Resolution Adjust (15.360 LSBs)**

Interpreting the results in a correct way it is possible to extend the measurement range to the triple (not possible in high resolution mode). See section 2.5.8.

- **No negative results at ' High Resolution '**

In the High Resolution mode it isn't possible to calculate negative times. In fact this isn't necessary, because in this mode only multiple hits of one channel are measured and it is known before calculation which event is the first. The hit with the lower hit number can be subtracted from the hit with the higher hit number, not vice versa.

2.5.4 External circuit of the PLL

In case the Resolution Adjust mode should be used, an external circuit for the core supply voltage becomes necessary.

Figure 7: PLL external circuit

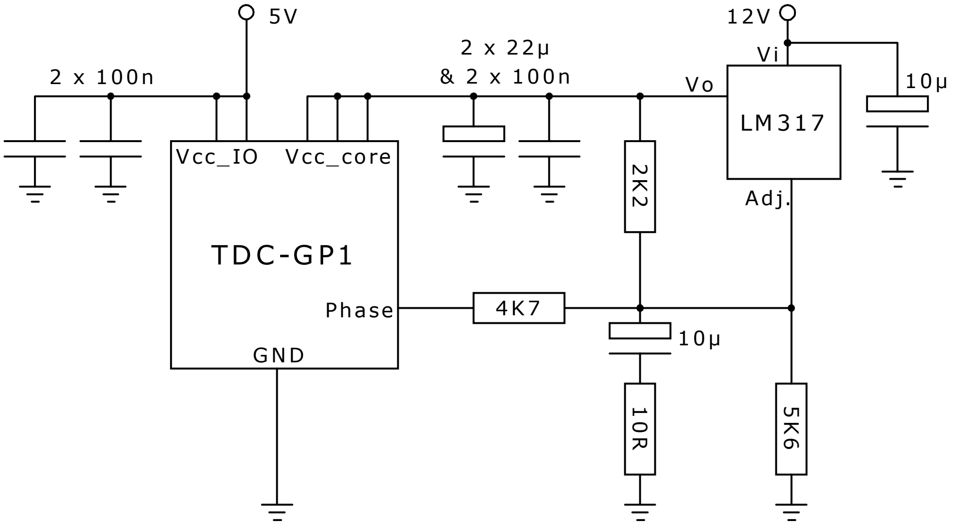


Figure 7 displays an example of an inexpensive external circuit for the core supply voltage of the GP1 running in resolution adjust mode. It should be noted that the core voltage is regulated and not the I/O voltage of the module. The I/O voltage remains at 5 V. Otherwise the input protection diodes will be overdriven due to the too small voltage caused by the regulation.

Power consumption: The power consumption of the GP1 is higher in the Resolution Adjust mode. It is approx. 25 mA and is practically independent of the measuring rate.

2.5.5 Control of the measuring, Adjustment possibilities

- **Adjustments of the measurement mode**

Relevant Register: Control register 1 Address: 1
Relevant Bits: 7
Effect: 0 = off; 1 = on ;Default: off

- **Enable the number of hits**

Relevant Register: Control register 7 Address: 7
Relevant Bits: 5-0
Effect: see table
Default: 4 hits per channel

The number of hits is given by the following table:

EN_HITx<2..0>	No. of hits
1	1
2	2
3	3
4	4

- **Adjustments of edge sensitivity**

Adjustments identical with measurement range 1. Please see section 2.3.4!!!

- **Identification of the adjust mode**

Whether the PLL was capable to tune to the selected resolution can be queried from status register 1 bit 7. This bit is set to '1' approx. 10 ms after the PLL locked. For laboratory tests the output phase of the

GP1 is a good observation point. In it's locked mode a digital clock with varying duty cycle is sent off from the phase output. It's mean current is responsible for the control voltage of the voltage regulator.

- **Reactions on exceeding the adjustment range**

If a resolution is selected too close to the adjustment limits, it may happen that strong temperature changes cause a failure of the regulation loop, indicated by PLL_LOCK (register 1) changing from '1' to '0'. The control loop can not regulate anymore. The GP1 is now in floating resolution mode. The module switches back to the resolution adjust mode automatically as soon as the adjusted parameters and the operating conditions allow. The GP1 shows the same reaction if the resolution cannot be adjusted after initialization after initialization.

2.5.6 Specialties of the Resolution Adjust Mode

As already mentioned the Resolution Adjust Mode has no start. As a consequence only stops can be measured against each other. An absolute measurement of the stops against a specific reference point is not possible. It can however be arranged that the ALU reveals the absolute value of a hit. This value does not make any sense though. The measured time difference can only be revealed in the difference of the single hits.

RLC measurements can be done in the Resolution Adjust Mode too. However, it does not make sense to use the Resolution Adjust Mode if only the RLC ports shall be measured. This option was originally designed to offer the possibility of a RLC measurement without leaving the Resolution Adjust Mode (e g a temperature measurement).

The PLL offers a SET_PAR Mode (register 4 bit 3). The control loop is not closed in this mode. A clock with a 50% duty cycle is sent out at PHASE, the regulation range is symmetrical. The PLL determines an adjustment value of the PLL control register (register 3) that fits to this duty cycle. This is a good opportunity to get a proposal for the FAK_PLL value.

If you set the value of the PLL control register (address 3) to 225 and switch the SET_PAR mode off the calculated value will automatically be used.

Timeout: Also in the Resolution Adjust Modus a timeout is generated. But this has no influence on regular measurements however unlike for the other modes. Only the timeout flag gets set. The measuring isn't interrupted. After a timeout hits are furthermore accepted until the selected number of hits is reached.

2.5.7 Extension of measurement range up to 11 µs

If the measurement range of 3.8 µs is not enough, there are possibilities to extend the range up to the triple by correct interpretation of the results. It is made use of the fact, that in resolution adjust mode the GP1 does not stop to measure after a timeout but measures also correctly beyond. Merely the ALU isn't able to calculate the results correctly.

The ALU reacts as follows:

If a calculated value of the ALU exceeds 15.360 LSB the ALU subtracts a constant offset of 30.720 LSB. The result is correct except for this offset. This reveals a very simple possibility to double the measurement range. Because corrected results are negative it is necessary to know definitively the order of the stops. Only positive results can be corrected this way.

2.5.7.1 Correction rules for doubling the measurement range:

If negative results are read out, 30.720 LSB have to be added to the results. The range of the corrected values is 0 to 30.720 LSB, approx. 7.8 µs (typ.).

Therefore after 30.720s LSBs the results again are positive. To triple the possible measurement range the overflow bit can be used (status register 1, bit 6).

2.5.7.2 Correction rules to triple the measurement range:

If the selected measurement result is positive and the Overflow Flag = 0, then we are actually in the standard measurement range, the result is so correct.

If the selected measurement result is positive and the Overflow Flag = 1, then we are above the 30.720 LSB. The result has to be increased by 30.720 to get the correct value.

To get the right value of the overflow bit, external circuitry is necessary. The overflow bit has to made visible via the INT Pin of the GP1 (set Bit #7 of Reg 6 to 1) and for every hit the overflow flag has to be saved and the corresponding INT Bit has to be used for the correction of the result.

2.5.8 Calculation of the resolution of the GP1

3 parameters are necessary for the destination of the resolution.

- the length of the period of the reference clock
- the divider of the reference clock (register 4: bits 2..0)
- the adjusted value of the PLL division register FAK_PLL (register 3: all bits)

The adjusted resolution of the GP1can be calculated according to the following formula

$$\boxed{Resolution = \frac{T_{ref} * 2^{nref}}{120 * PLL\_L}}$$

Example: Reference clock = 10 MHz → clock period = 100 ns
Division factor of the reference clock: 2^5 = 32
PLL-adjustment value = 100 (default)
These adjustments result in a resolution of 266,66 ps

2.6 Add on the High Resolution Mode

The two channels of the GP1 correlate with each other very strongly. This becomes apparent due to their identical resolution for example. The close coupling gives both channels the possibility of being connected with each other so that a 1 channel TDC with twice the resolution is the result. This can be realized with the High Resolution Mode. The stop 2 input is disabled in this mode. Stop pulses on stop 2 have no effect.

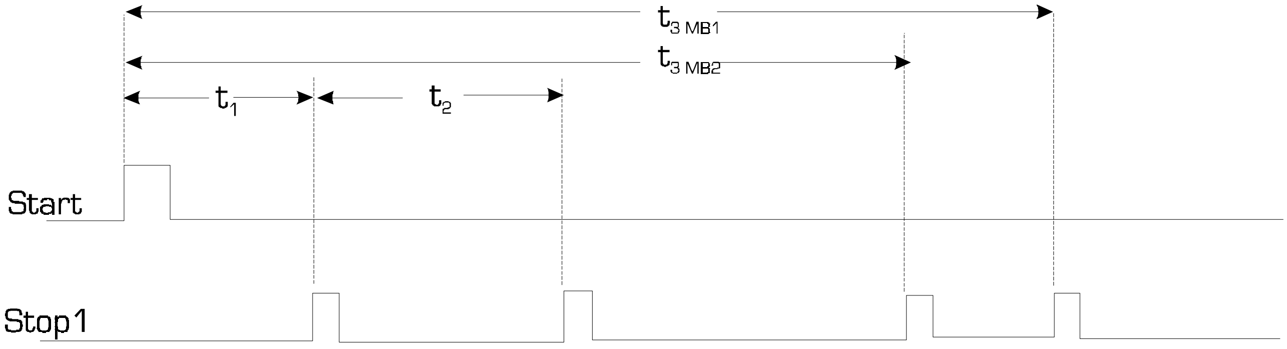
The high resolution mode can be used in

- Measurement range 1
- Measurement range 2
- Resolution adjust mode

2.6.1 Possible measuring sequences and timings

a. Measurement range 1and measurement range 2

Figure 8: Timings high resolution MB1, MB2



The following times should be noted (typ.):

- a stop may occur at the earliest 3 ns channels after a start. Stops that arrive earlier will be ignored.

→ Measurement range1: $t_{1\ min}$ = 3 ns
→ Measurement range2: $t_{1\ min}$ = 1.5*CAL_CLK + 25ns

- double pulse resolution: there must be at least 15 ns between 2 events (measurement range 2: 1.5*CAL_CLK+25ns). If the events are closer than the minimum the second event will not be recognized due to the recovery time of the channel

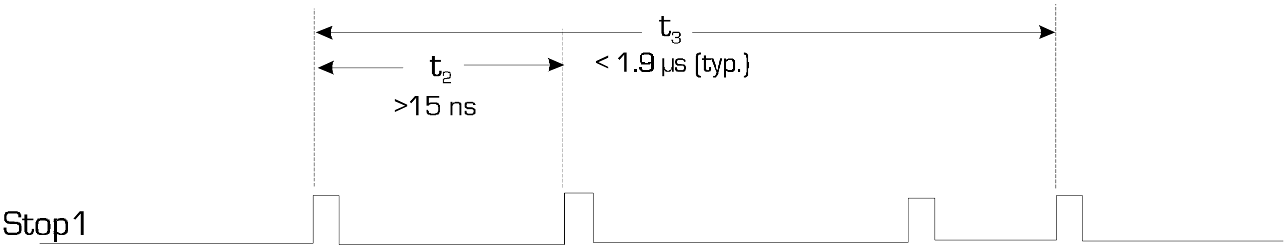
→ Measurement range1: $t_{2\ min}$ = 15 ns
→ Measurement range2: $t_{2\ min}$ = 1.5*CAL-CLK +25ns

- all the hits must arrive within 30.720 LSBs (2^{15}-2^{11}) form the start event (measurement range2: 2^{16}*CAL_CLK)

→ **Measurement range1: $t_{3\ max} \approx$ 3,8 µs (typ.)**
→ **Measurement range2: $t_{3\ max} = 2^{16}$*CAL-CLK**

b. Resolution Adjust Mode

Figure 9: Timings High resolution



Only hits arriving at STOP1 can be measured against each other.
The following times should be noted (typ.):

- there must be at least 15 ns time between 2 events (double pulse resolution). If the events are closer than the minimum the second event will not be recognized due to the recovery time of the channel

→ **Measurement range 1: $t_{2\ min} = 15$ ns**

- all of the measured events must arrive within 15.360 LSBs (2^{14}-2^{11}) of the start event

→ **Measurement range 1: $t_{3\ max} \approx$ 1,9 µs (typ.)**

- In high resolution mode no extension of the measurement range according to section 2.5.8 is possible.

2.6.2 Control of the measurements, Adjustment possibilities

- **Adjustments in this mode:**

Relevant Register: Control register 1 Address: 1
Relevant Bits: 6-0
Effect: Bit 6 = activation, 0=off, 1=on, Default=off
Bit 5-0 Adjustment bits, default=0

The value of ADJ is dependent on the production lot. The results are best with

Bit < 5 .. 0 > : 001011

- **Measurement range 1**

In measurement range 1 the GP1 is a 1-channel TDC with 4-fold multihit capability.

Enable the number of hits

Relevant Register: Control register 7 Address: 7
Relevant Bits: 2-0
Effect: see table
Default: 4 hits per channel
In register 7 (address 7) the number of hits per channel is adjusted. The following adjustments apply:

EN_HIT1<2>	EN_HIT1<1>	EN_HIT1<0>	Number of possible hits
0	0	0	0 Hits, Software Disable of channel
0	0	1	1 Hit
0	1	0	2 Hits
0	1	1	3 Hits
1	0	0	4 Hits

The bits EN_HIT2<2..0> will not be evaluated. The adjustments of the edge sensitivity, retrigger mode and auto noise remain identical to normal resolution. Queuing is not possible.

- **Measurement range 2**

In measurement range 2 the GP1 is a 1-channel TDC with 3-fold multihit capability in. Together with the start the 3 hits already occupy all raw value registers.

Enable the number of hits:

Relevant Register:	Control register 7	Address: 7
Relevant Bits:	2-0	
Effect:	see table	
Default:	3 hits	

The number of hits per channel are adjusted in register 7 (address 7).

The following adjustments apply:

EN_HIT1<2..0>	EN_HIT2<2..0>	number of hits
2	x	1
3	x	2
4	x	3

The bits EN_HIT2<2..0> are not evaluated. The adjustments of the edge sensitivity, retrigger mode and auto noise remain identical to normal resolution.

2.7 RLC-Measurements

2.7.1 Principle operation

The measurement of several basic physical dimensions can easily be traced back to time interval measurements. This also applies for the 3 basic dimensions of electronics

- R (resistor)
- L (induction)
- C (capacitor)

The GP1 permits this measurements using a very simple external circuits at the related pins. The determination of the quantities is done by ratio measurements (as with most other measurement instruments). The ratio of time differences leads to the ratio of the physical quantities i.e. $\Delta t_1 / \Delta t_2 \propto \Delta R_1 / \Delta R_2$.

Example: Resistor determination
A known capacitor is first discharged through an unknown resistor. A start pulse is generated with the beginning of the discharge. If the voltage at the capacitor is lower than the threshold of the comparator at the SENSE input, a stop pulse is generated. The time difference between start and stop is measured by the TDC.
The entire process is then repeated with a reference resistor of familiar value. The ratio of the two time intervals is the same as the ratio of the two resistors provided that the same capacitor and comparator are used for both measurements.
The same process is used for the determination of the inductors and capacitors.

Due to the high resolution of the TDC this type of measurement happens within few microseconds. The advantage is that short-term changes can be registered quickly. Another advantage is the small energy consumption of such a measuring procedure. For the complete determination of a resistor less than 1 µAs are necessary. As a result with only a few measurements per second the current consumption is in the range of only a few µA. The circuit expenditure is very small and - as a result - also inexpensive. Very exact measurements can be done.

2.7.2 Possible Measuring Sequences and Timings

Measurement Sequences

RLC measurements can be done in 2 different ways

- as a complete measurement from port 1-n (n_{max}= 4).
- as a single measurement. Only a selected port is measured here

Measurable Times

The RLC measurements can be executed in measurement range 1 as well as in measurement range 2. The maximum measurable time depends on the measurement mode.

Measuring Process

The measurement starts with a 0 -> 1 transition at bit 3 of control register 6. After a port is measured, it is optimally calibrated. After that, the calculation of the ALU defined in register 2 will be carried out. After the calculation, the results are stored in the result register of the ALU. At multiport measurements the address is automatically increased. After a measurement cycle has ended, the RLC_END flag is set so that it can be queried via status register. The entire cycle needs approx. 1000 R-L-C clock cycles plus the measuring time for a measurement with 4 ports. A 1 port measurement needs approx. 250 R-L-C clock cycles plus measuring time.

Example: An RLC-measurement with 4 ports and 10 MHz RLC clock and a measuring time of approx. 10 µs per port needs approx. 140 µs. If the ALU is set for calibration the results of the 4 measurements become visible as 32 bit values in a rising sequence in the result registers 1-8. Every value occupies two 16 bit registers.

2.7.3 Control of the Measurements, Adjustment Possibilities

- **Adjustment of the mode:**

Relevant Register:	Control register 6	Address: 6
Relevant Bits:	3, 2	
Effect:	Bit 3 = activation, 0=off, 1=on, Default=off Bit 2 = Use of external transistors 0= no, 1= yes , default=no	

Relevant Register:	Control register 5	Address: 5
Relevant Bits:	7-0	
Effect:	see further explanations	

- **Adjustments in register 5**

Register 5 **Address: 5**

Bit No.	Name	Explanation	Default
7	RLC_NR<2>	Choice as to which and how many ports should be measured	1
6	RLC_NR<1>	"	0
5	RLC_NR<0>	"	0
4	SINGLE_EN	Measure selected ports = 1, 0= all ports from 1 through RLC_NR	0
3	C_SEL	Measuring capacity ratios = 1	0
2	SEL_CLK_RLC<2>	Selection of clock for RLC unit	0
1	SEL_CLK_RLC<1>	"	0
0	SEL_CLK_RLC<0>	"	0

In Bit 5-7 the number of ports will be adjusted (provided that SINGLE_EN='0'), If SINGLE_EN='1' the ports that need to be measured will be selected. The following table applies.

RLC_NR<2..0>	SINGLE_EN=0	SINGLE_EN=1
	Number of ports	Port Number
0	-	-
1	1	1
2	2	2
3	3	3
4	4	4

C_SEL

The control of the ports is identical for R and L measurements. For C measurements however the ports must be controlled in a different way. It is therefore necessary to inform the chip if a C measurement will be done. Bit 3 (C_SEL) is responsible for this. If a '1' is set the ports will be controlled accordingly to C-measurements.

SEL_CLK_RLC
The controlling unit which regulates the RLC measurements is clocked by the reference clock. This clock can be adjusted according to the requirements through an internal clock divider. The division factor is adjusted with SEL_CLK_RLC.
The following table applies.

SEL_CLK_RLC<2..0>	Division factor
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	64

- **Adjustments in Register 6**

Bit 2 and 3 in register 6 are additional control bits for RLC measurements:

USE_TRANS
It is recommended not to use the internal chip port drivers during low-value resistivity and inductivity measuring but to use external transistors like a NPN transistor instead. If this possibility is applied, the GP1 must be informed to adjust the driving procedure. If the bit is set to '1' the application of an external transistor is assumed. The necessity of external transistors depends on the resistance and the required accuracy. Typically the internal port drivers have an R_{DS}-ON of approx. 15 Ω at 5 V / 25 °C and the matching is about 1.5 Ω. The measurement task determines whether this accuracy is sufficient.

RLC_EN
If the bit is set to '1' the RLC measurement begins. The bit must hold at '1' during the entire measurement. At the end of the measurement the TDC stops automatically. The RLC_END flag is issued by the status register.

The RLC_EN bit is not automatically set to '0' at the end of the measurement. If a new RLC measurement shall be started the bit must first be set to '0' and then to '1' again. The bit must remain at '0' for at least 6 RLC clock periods.

2.7.4 External Connection of the Ports

The following 3 diagrams show the external connection of ports for R, L and C measurements with and without external transistors.

Figure 10: Resistance measurement with external transistors

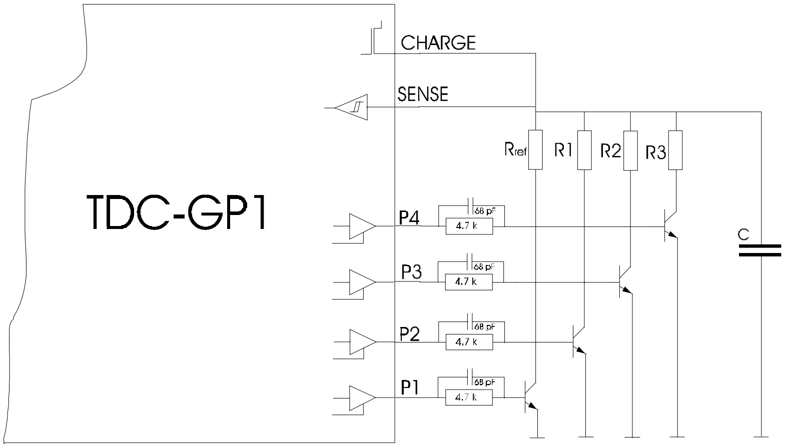

CHARGE
SENSE
TDC-GP1
Rref
R1
R2
R3
P4
P3
P2
P1
68 pF
4.7 k
C

Figure 11: Inductance measurement without external transistors

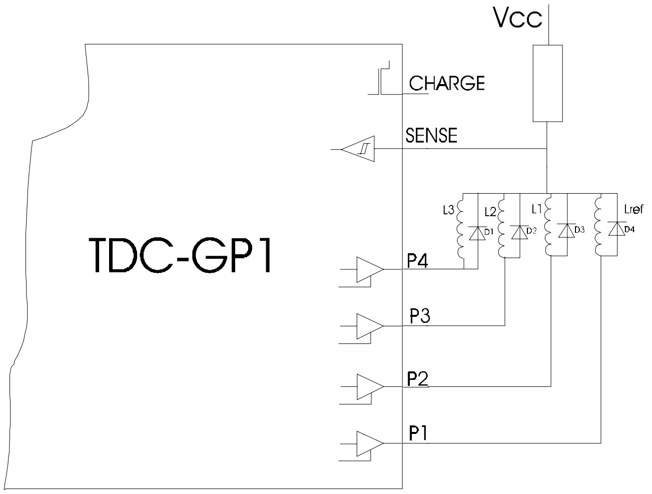
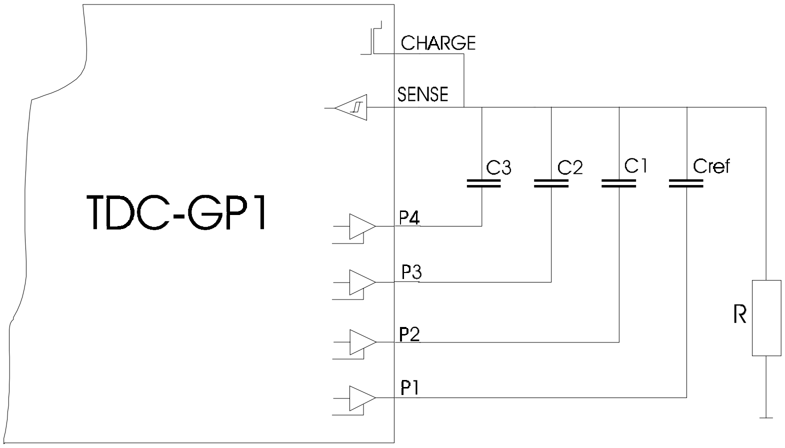

Vcc
CHARGE
SENSE
TDC-GP1
L3
L2
L1
Lref
D1
D2
D3
D4
P4
P3
P2
P1

Figure 12: Capacity measurement without external transistors


CHARGE
SENSE
TDC-GP1
C3
C2
C1
Cref
R
P4
P3
P2
P1

2.7.5 Accuracy of RLC-Measurements

Using the RLC-measurement the ratios of component's values can be determined with a precision about 50ppm in single measurement. Averaging over a set of measurements reduces the standard deviation to <10ppm. To achieve this precision some points should be noted. The achievable precision doesn't depend on the TDC-unit but mainly on a low-noise threshold of the Schmitt trigger and switching transistors with low Rds(on). Therefore note:

- during measurements no I/O-operations on the bus are allowed (i.e. polling of status registers). This heavily disturbs the threshold level of the intrinsic Schmitt trigger. As an alternative an external Schmitt trigger at the SENSE-input can be used to cover this problem.
- if low-ohmic resistors have to be measured (i.e. PT500), external transistors, preferably MOSFETs with low Rds(on), should be used. The Rds(on) of the internal port transistors is too high to achieve highest precision.

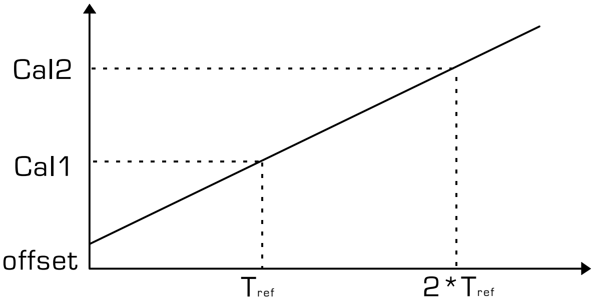
2.8 Calibration of the GP1

(see also chapter 5 'Known Problems and solutions')
There are 2 different ways to calibrate the GP1

- via command
- automatically after a start/stop event

During a calibration process one and two clock periods of the calibration clock will be measured in a multihit process. The results are stored in special calibration value registers which restore up-to-date values during every calibration process. A separate calibration process is automatically triggered by setting bit 7 in register 0. The bit is automatically set to '0' after the calibration finished. If automatically calibration is selected, the calibration is triggered after reaching the selected number of hits on both channels.

Figure 13



2.8.1 Control of the Measurement, Adjustment Possibilities

- **Separate calibration**

Relevant Register:	Control register 0	Address: 0
Relevant Bits:	7	
Effect:	1 = calibration in process	
Default:	0	

- **Auto calibration**

Relevant Register:	Control register 0	Address: 0
Relevant Bits:	3	
Effect:	1 = Auto calibration is enabled	

2.8.2 Effects of the Adjustments

Separate Calibration

After setting this bit start and stop signals are derived from the calibration clock with the period of the calibration clock. In a multihit process 2 hits are generated which represent one and two calibration clock periods. After a separate calibration run the CAL bit is automatically reset to '0' after the run has finished. For a separate calibration only the register 0 must be rewritten.

Auto Calibration

If only a few measurements occur or if there is plenty of time between the measurements the automatic calibration is an effective alternative. This option starts an automatic calibration after the number of selected hits has been reached. The process is the same as for separate calibration.

In general the calibrated values can be read out for control reasons. This option is described in the section 'Calculation possibilities of the GP1'

2.9 Calculation Possibilities of the GP1

The past sections spent most of their time with the measuring possibilities of the GP1. The next sections are dedicated to the calculation possibilities of the GP1 and the control of the micro-controller interface.

As already mentioned, only the 8 result registers of the GP1 and the status registers are accessible. The sequential ALU takes the data from the raw value registers and transfers them to the result register. The handling of the measured values by the sequential ALU can be controlled in very broad ranges by the control register 0, 1 and 2.

2.9.1 ALU Control

The elementary control register for the selection of the hits is register 2. Two words 4 bits each are available here which serve the selection of the hits.

Register 2 **Address: 2**

Bit No.	Name	Explanation	Default
7	HIT2_IN<3>	channel select for upper nibble 0=chan.1, 1=chan.2	0
6	HIT2_IN<2>	hit-no. for channel selected in bit 7	1
5	HIT2_IN<1>	hit-no. for channel selected in bit 7	0
4	HIT2_IN<0>	hit-no. for channel selected in bit 7	1
3	HIT1_IN<3>	channel select for lower nibble 0=chan.1, 1=chan.2	0
2	HIT1_IN<2>	hit-no. for channel selected in bit 3	1
1	HIT1_IN<1>	hit-no. for channel selected in bit	0
0	HIT1_IN<0>	hit-no. for channel selected in bit	1

Every calculation in the sequential ALU begins with the following function

HIT1_IN - HIT2_IN

The hit selected in the higher nibble is subtracted from the hit selected in the lower nibble.

Nibble format:
The top bit of the appropriate nibble selects the channel number.
Nomenclature: 0 = channel 1; 1= channel 2

The lower 3 bits display the hit numbers of the respective channel.

Examples:				
Content of Reg. 2: Oxa4	*Effect:*	*4th Hit channel 1*	*minus*	*2nd Hit of channel 2*
Content of Reg. 2: Ox13	*Effect:*	*3rd Hit channel 1*	*minus*	*1st Hit of channel 1*
Content of Reg. 2: Ox3b	*Effect:*	*3rd Hit channel 2*	*minus*	*3rd Hit of channel 1*

If the top nibble's content is set to '0' the time difference between start and stop is written to the result register (MB1).

Examples:		
Content of Reg. 2: 0x04	*Effect*	*4th Hit channel 1*
Content of Reg. 2: 0x0c	*Effect:*	*4th Hit channel 2*

Calibration values
The calibration values can also be accessed via selection in register 2. The following applies for the lower 3 bits of a nibble: 6 = CAL 1; 7 = CAL2. The top bit selects the channel.

Examples
Content of Reg. 2: 0x0f Effect: CAL 2 of channel 2
Content of Reg. 2: 0x06 Effect: CAL 1 of channel 1
Content of Reg. 2: 0x67 Effect: CAL 2 of channel 1 minus CAL 1 of channel 1

Register 0

After the mathematical operations defined in register 2 the selected operations selected in bits 5 and 6 of register 0 will be processed. If bit 6 of register 0 is set to '1' the result of the prior operation will be calibrated. In addition, if bit 5 of register 0 is set at '1' the result will be multiplied with the value of the 24 bit multiplication register.

Attention: It is not permitted that a value is multiplied without a previous calibration. This normally makes little sense since it involves uncalibrated values. It is however possible if one can guarantee that the value to be multiplied is smaller than 15,360. In this case be aware that the result will be 32 bit long again.

2.9.2 The Multiplication Register

The multiplication factor is stored in a 24 bit multiplication register which can be accessed via micro-controller interface. The following addresses apply:

Register 8-10
Address:8-10

		Default
Register 7, Address 7	Multiplication factor<7..0>	0
Register 8, Address 8	Multiplication factor<15..8>	0
Register 9, Address 9	Multiplication factor<23..16>	128

The MSB of the 24 bit value has the value 2^0. Multiplication factors 0 through 2 can be set. The default value after Power On Reset is '1'.

2.9.3 Calculation Rules in Measurement Range 1

The following calculation rules apply for measurement range 1

$$\boxed{\mathrm{ERG} = \mathrm{MULT} * \frac{(\mathrm{VAL}(\mathrm{HIT2\_IN}) - \mathrm{VAL}(\mathrm{HIT1\_IN})) - (2 * \mathrm{CA} - \mathrm{CAL2})}{\mathrm{CAL2} - \mathrm{CAL1}}}$$

Definitions:

1. *VAL[HIT2_IN] - VAL[HIT1_IN]* : Calculation instruction of register 2
2. *2*CAL1-CAL2*: Offset correction
3. *CAL2-CAL1*: Gradient of the calibration line
4. *MULT*: Multiplication factor
5. *ERG*: Result which is stored into result register

If the calibrate and multiply bits in register 0 are set to '0', only operation 1 will happen. If the calibrate is set at '1' the division will be carried out. If the multiply is set at '1' the entire mathematical instruction will be carried out.

2.9.4 Calculation Rules in Measurement Range 2

The following calculation rules apply for measurement range 2

$$\boxed{\mathrm{ERG} = \mathrm{MULT} * \left(\mathrm{CC} + \frac{(\mathrm{VAL}(\mathrm{HIT1\_I}) - \mathrm{VAL}(\mathrm{HIT2\_I}))}{\mathrm{CAL2} - \mathrm{CAL1}}\right)}$$

Definitions:

1. *VAL[HIT1_IN] - VAL[HIT2_IN]* : Calculation instruction of register 2
2. *CAL2-CAL1*: Gradient of the calibration line
3. *CC:* Value of the predivider (Coarse Count)
4. *MULT*: Multiplication factor
5. *ERG*: Result which is written into result register

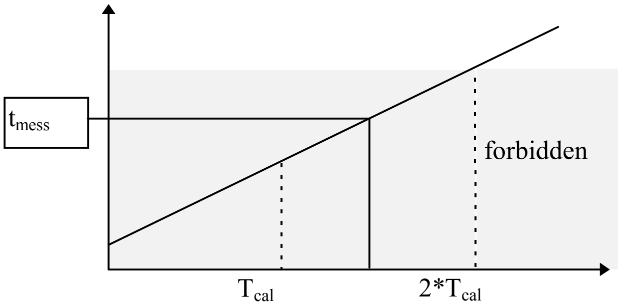
The CALIBRATE bit (bit 6 register 0) should always be set to '1' in measurement range 2 so that the result makes sense.

The result is written into the result register as a multiple of the calibration clock period.

2.9.5 Specialties of Measurement Range 1

Due to the internal structure of the ALU, a calibrated value (without multiplication) must be smaller than 2. This requires that the measured time intervals must be smaller than twice the calibration clock period (=T_{ref}/clock divider).

Figure 14



This makes sense as for higher values the influence of the gradient's accuracy would be to immense.

It is important that the period of the calibration clock (= Tref/clock divider) measures at least half of the maximum time interval.

The ALU has an overflow indicator in order to prevent misuse. If the ALU overflow occurs during the calculation the bit with the value 2^7 is set to '1' in the result register. Normal results never exceed 128 because even with the multiplication by 2 a correct result will never be larger than 4.

2.9.6 Specialties of measurement range 2

Measuring mode 2 is completely different in the way of measurement. This is reflected in the calculation possibilities. We have 2 finecounts that are generated with the measuring unit and one coarse count that displays the number of periods of the calibration clock:
Hits can't be calculated against each other in measurement range 2. Only the differences to the start event can be calculated.

The adjustments in register 2 have to follow the placement of the finecounts in the raw value registers. (see 2.4.2).

Channel	**Raw value register**	**Stored values in measurement range 2**	
		Normal	**High Resolution**
1	1	FC 1	FC 1
1	2	FC 2	FC 2
1	3	FC 3	FC 3
1	4	FC 4	FC 4
2	1	FC 5	FC 1
2	2	n.c.	FC 2
2	3	n.c.	FC 3
2	4	n.c.	FC 4

Only the finecounts of interest must be set in register 2. The ALU itself generates the address for the coarse count.

Example: Hit 3 shall be calculated. Therefore FC1 - FC4 must be calculated. Therefore the value 'h41' must be written into register 2.

Attention: If finecounts are generated that don't make any sense the ALU will nonetheless accept them without failure message and a (senseless) result will be generated. The result does not automatically appear to be false. Be careful!

2.9.7 Specials of Resolution Adjust Mode

In Resolution Adjust Mode one can measure only the time differences between stop events (there is no start). The read out of the raw values makes no sense. The ALU accepts the addressing of absolute values ('0' in top nibble) in register 2 without any failure message and will store a senseless value in the result register. The Resolution Adjust Mode permits the calibration value register to be read out at any time. But no calibration run can de performed and the registers can not be written.

2.9.8 Calculating Times of the ALU

The calculating times of the ALU depend on the used mode, the selected value of the speed parameter of the BIGALU clock in control register 6 (SPEED<1:0>) and the operating voltage of the core. For the speed control use register 6 with the following table:

SPEED<1:0>	speed factor	remark
0	-	not allowed
1	1	middle attitude
2	1,37	slowest attitude (default)
3	1,37	redundant with adjustment 2

Multiply the following times with this factor.

When using speed=1, a core supply voltage of 5 V, 25 °C ambient temperature and assuming typical process parameters following table for calculation times is valid:.

Table: time1

Mode of calculation	**High Res**	**Calculation time**
HITx to Start	no	140 ns
HITx - HITy	no	180 ns
HITx to Start	yes	182 ns
HITx-HITy	yes	263 ns
+ Calibration	-	+ 2000ns
+Multiplication	-	+ 2000 ns

Remarks:

- for calibration and multiplication the given values have to be added to the previous times
- in Resolution Adjust mode only HITx-HITy is possible

Under acceptance of the worst case production process above times are 1.4 (Kp) times longer, in best case they are 0.61 shorter.

For different core voltages use following table

Table: Kv

VDD	Kv
5.5 V	0.94
5.0 V	1.00
4.5 V	1.07
3.3 V	1.39
3.0 V	1.54
2.7 V	1.74

For different temperatures use following table

Table: Kt

Temp	Kt
125 °C	1.26
85 °C	1.15
70 °C	1.11
25 °C	1.00
-25 °C	0.87
-40 °C	0.82
-55 °C	0.79

The following formula applies to the calculation of the resulting ALU calculation time

$$\boxed{Time=time1*Kp*Kv*Kt}$$

2.10 The micro-controller interface

The GP1 offers a 8 bit micro-controller interface that is designed in accordance with common standards. It offers a

- 8-bit bi-directional data bus
- 4-bit unidirectional address bus

and the following control signals

- WRN (writing in the GP1, low active)
- RDN (reading from the GP1, low active)
- CSN (Chip Select, low active)
- ALE (Address Latch Enable, '1': the Address Latch is transparent)

2.10.1 Timing - Writing into the GP1

While writing in the GP1 two situations should be differentiated

- with ALE, necessary for common data / address bus
- without ALE, for separated data / address bus, the ALE signal can constantly be set to '1'. Naturally it is possible to work with ALE for separated data/address buses as well.

The following diagrams show the necessary timings.

Figure 15: Writing with ALE and common data/address bus

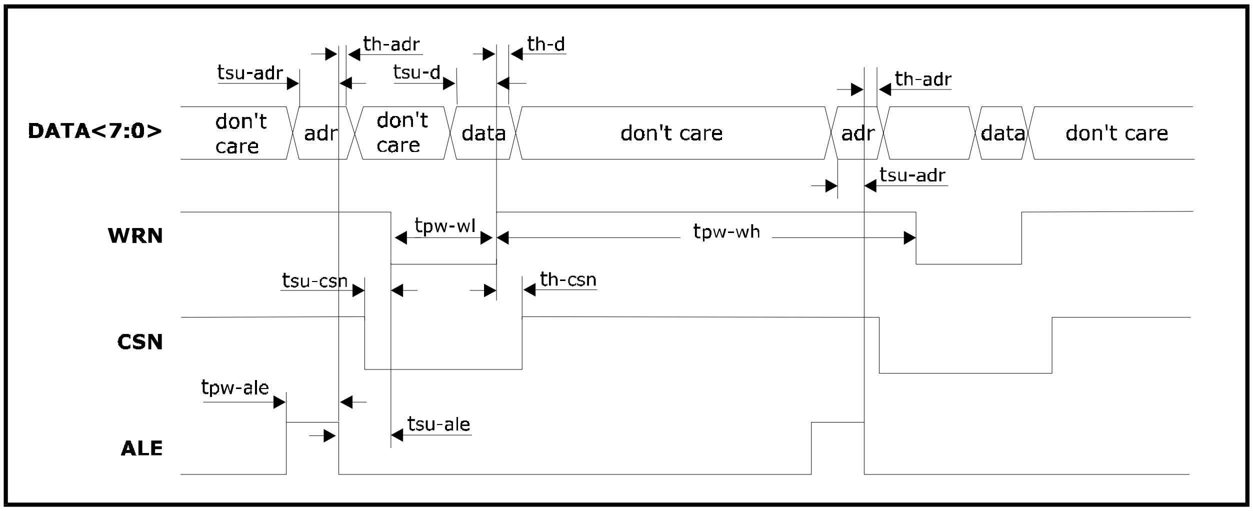
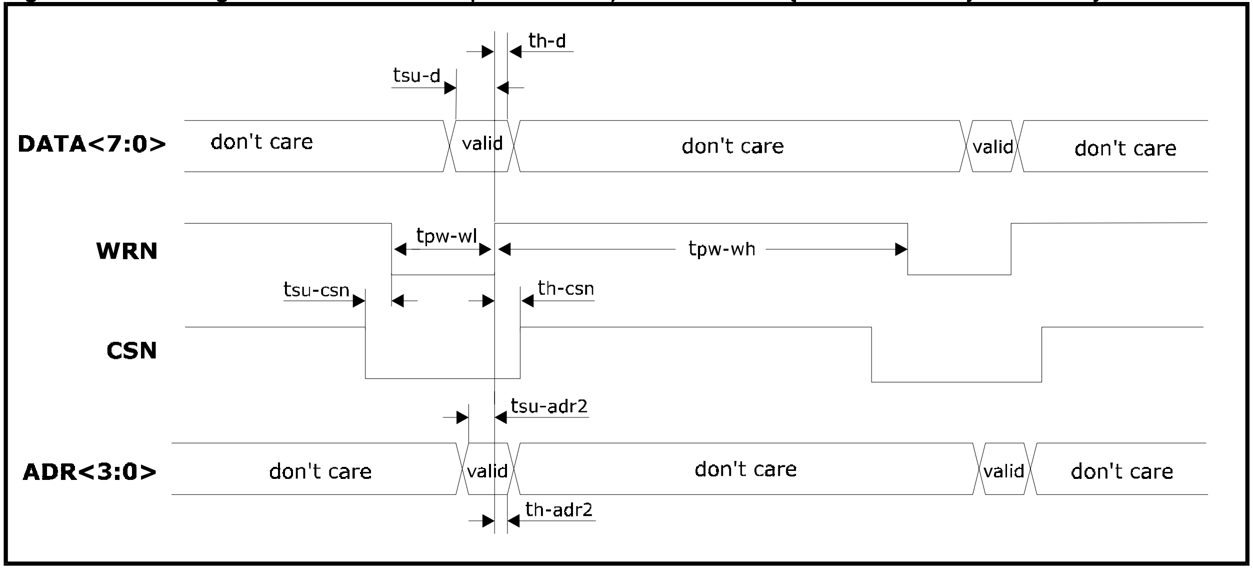

th-adr
th-d
tsu-adr
tsu-d
th-adr
DATA<7:0>
don't care
adr
don't care
data
don't care
adr
data
don't care
tsu-adr
WRN
tpw-wl
tpw-wh
tsu-csn
th-csn
CSN
tpw-ale
tsu-ale
ALE

Figure 16: Writing without ALE and separate data/address bus (ALE constantly set at '1')


th-d
tsu-d
DATA<7:0>
don't care
valid
don't care
valid
don't care
WRN
tpw-wl
tpw-wh
tsu-csn
th-csn
CSN
tsu-adr2
ADR<3:0>
don't care
valid
don't care
valid
don't care
th-adr2

The following timings apply:

Name	Definition	Values without SUI (default)	Value with SUI
tsu-d	Setup-time dates to positive edge WRN	> 10 ns	no change
th-d	Hold-time dates to positive edge WRN	> 0 ns	no change
tsu-csn	Setup-time neg. edge CSN to neg. edge WRN	> 0 ns	no change
th-csn	Hold-time pos. edge CSN to pos. edge WRN	> 0 ns	no change
tsu-adr	Setup-time address to negative edge ALE	> 10 ns	no change
th-adr	Hold-time address to negative edge ALE	> 3 ns	no change
tpw-wl	Pulse-width of negative WRN pulse	> 25 ns	> 40 ns
tpw-wh	Pulse-width positive phase WRN	> 25 ns	> 40 ns
tsu-ale	Setup-time neg. edge ALE to neg. edge WRN	> 0 ns	no change
tpw-ale	Pulse-width ALE	> 20 ns	no change
tsu-adr2	Setup-time address to positive edge WRN, case 2	> 10 ns	no change
th-adr2	Hold-time address to positive edge WRN, case 2	> 3 ns	no change

Attention:

These times apply in the standard mode of the micro-controller interface at 5V ± 10 % supply voltage.

- When using spike suppression interface (SUI) look at the right column.
- When using a lower supply voltage for the core the selected values will become larger. Taking the times above and multiplying them by 2.5 will result in times valid for the whole supply voltage range.

2.10.2 Timing - Reading from the GP1

The same basic requirements apply for the reading from the GP1 as do for the storing. It is necessary again to differentiate between the different modes:

Figure 17: Read with ALE and common data/address bus

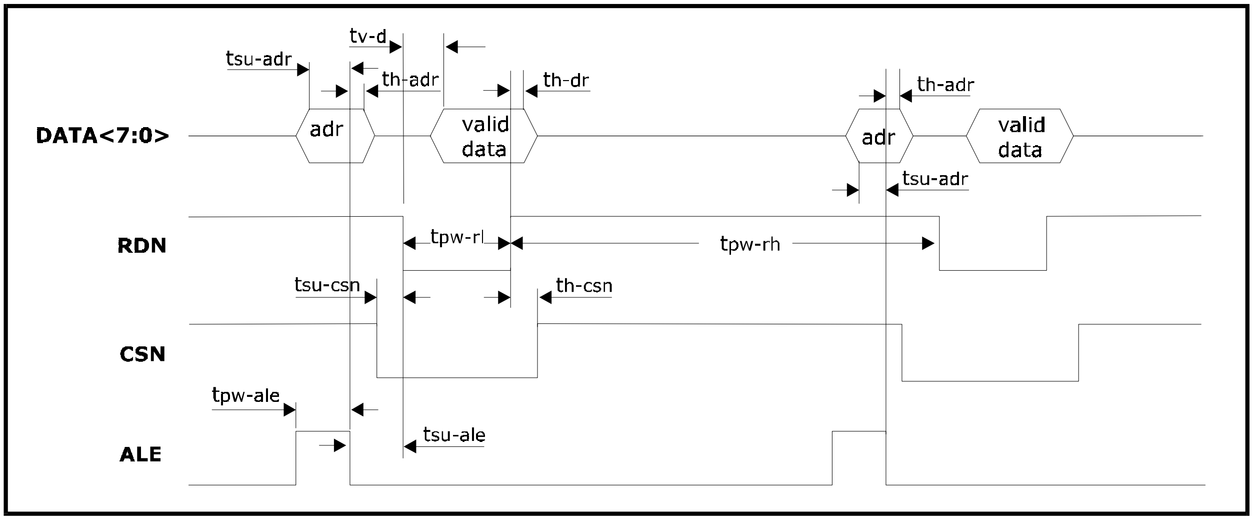
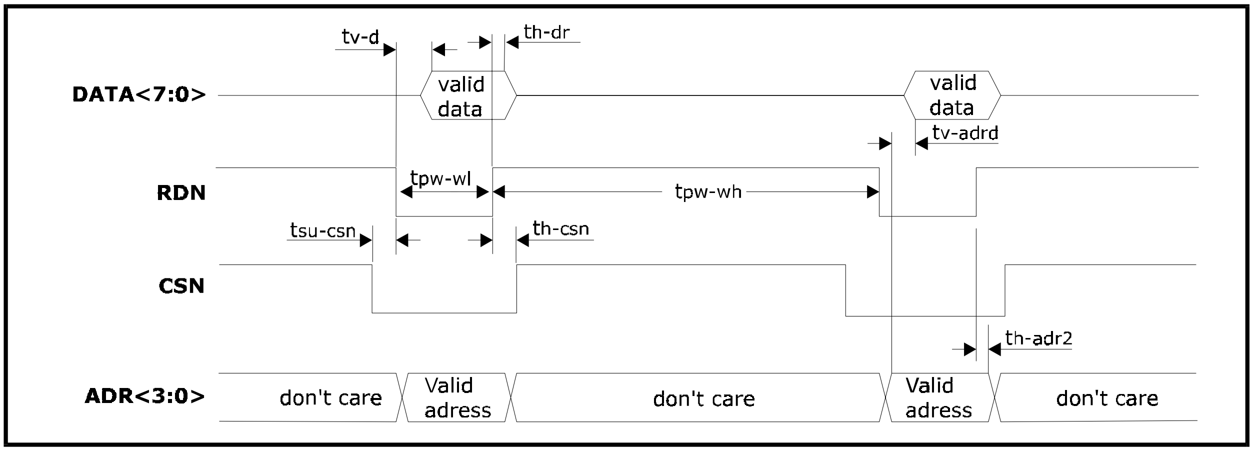


Figure 18: Read without ALE and separate data/address bus (ALE constantly set at '1')



The following timings apply

Name	Definition	Values without SUI (Default)	Values with SUI
tv-d	Time till data is stable from negative edge RDN	< 18 ns	< 30 ns
th-d	Hold-time data at positive edge RDN	> 2 ns	> 5 ns
tsu-csn	Setup-time neg. edge CSN to neg. edge RDN	> 0 ns	no change
th-csn	Hold-time pos. edge CSN to pos. edge RDN	> 0 ns	no change
tsu-adr	Setup-time address to negative edge ALE	> 10 ns	no change
th-adr	Hold-time address to negative edge ALE	> 3 ns	no change
tpw-wl	Pulse-width of negative RDN pulse	> 25 ns	> 25 ns
tpw-wh	Pulse-width positive phase RDN	> 25 ns	> 25 ns
tpw-ale	Pulse-Width ALE	> 20 ns	no change
tsu-ale	Setup-time neg. edge ALE to neg. edge RDN	> 0 ns	no change
tv-adrd	Setup-Time Address to stable data	> 20 ns	no change
th-adr2	Hold-Time Address to positive edge RDN, case 2	> 3 ns	no change

Attention

These times apply in the standard mode of the computer interface at 5 V ± 10 % supply voltage

- When using the spike suppression unit (SUI) look at the right column.
- When using a lower supply voltage for the core the selected values will become larger. Taking the times above and multiplying them by 2.5 will result in times valid for the whole supply voltage range.

2.10.3 Testing Communication

A simple method to test the communication between TDC-GP1 and microcontroller is to write 0x60 into register 0 and toread from status register 9. The calibrate and multiplicate bits have an image in bits 3 and 4 of this status register.

2.11 Additional Functions of the GP1

2.11.1 Enable Measuring Channels

Every channel offers an enable pin (EN_STOP1, EN_STOP2). These pins allow to enable/disable the stop inputs of both channels independently at any time. A '1' at these pins enables the stop inputs. The pins do not affect the start input. The pins can be used in a way that single stops can be faded in or out via external hardware.

Attention: In measurement range 2 the stop enables must be '1' for the duration of the measurement.

In measurement range 1 and resolution adjust mode the enable inputs show the following timings:

Table: Setup/Hold enable timing

	min.	typ.	max
Setup Time	1.4 ns	2.2 ns	4 ns
Hold Time	4 ns	6 ns	11 ns

Typically the enable input must be activated 2.2 ns before the active edge of the stop pulse of interest and last for min. 6ns. Injuries of these times may lead to wrong measurement results.

2.11.2 Interrupt Flag

At pin 34 the GP1 offers an interrupt signal. Two interrupt sources are available which can be selected:

- at least one of the result registers has been written on (default)
- overflow of the measuring unit

The selection of the interrupt source is done in **control register 6 bit 7**. The default setting makes possible a very fast read out via external hardware. This can be started by the positive edge of the interrupt flag. Using this possibility measuring rates of approx. 4 million measurements per second can be achieved.

2.11.3 Division Factors for Internal Clocks

The 3 internal clocks can be derived from the reference clock connected to pin 3

- the calibration clock for the measuring unit
- the reference clock for the PLL
- the clock for the control of the RLC unit

Each of these clocks can be adjusted independently. There are division factors up to 64. They permit the flexible adjustment of the GP1 to the appropriate conditions and measurement tasks.

The division factors are adjusted in registers 4 and 5. The following adjustments apply for the division factors

SEL_CLK	Division factor	Comment
0	1	
1	2	
2	4	
3	8	
4	16	
5	32	
6	64	at SEL_CLK_RLC = 32
7	64	

2.12 Further Details

2.12.1 Recommended Operating Conditions

Outside of this range a smooth function of the circuits cannot be guaranteed.

Parameter	Symbol	minimum	maximum	Unit
Supply Voltage	VDD	2.7	5.5	V
Input Signal Voltage	Vi	0	VDD	V
Ambient temperature	Ta	-40	+85	C
HI input voltage	VIH	0.7 * VDD	VDD	V
LOW input voltage	VIL	0	0.3 * VDD	V
pos. Trigger spg	Vp		0,8*VDD	V
neg. trigger spg	Vn	0,2*VDD		V
Hysteresis	Vh	1.0		V
Input rise/fall time	tr, tf	0	200	ns
Input Schmitt rise/fall	tr, tf	0	10	ms

2.12.2 Absolute Maximum Ratings

An exceeding of these values may directly result in the immediate destruction of the circuit or the impairment of it's long-time reliability.

Parameter	Symbol	Minimum	Maximum	Unit
Supply voltage	VDD	-0.3	7.0	V
Input signal voltage	Vi	-0.3	VDD+0.3V	V
Input pin current		-10.0	+10.0	mA
Storage temperature	Tst	-55	+125	°C
Lead temperature			300	°C for 10 sec.

2.12.4 Current Consumption

The current consumption depends on the measurement mode. Following values can be expected (@5V/25°C)

- Quiescent current

The circuits typical quiescent current is ap. 1.5µA.

- Current consumption without resolution adjust

In this case the current consumption is dependent in a strongly linear manner on the active measuring time of the highspeed TDC-core. During measurements this unit needs about 20mA.
There is an additional amount coming from the ALU2 and the reference clock.
Typical values for currents are
- TDC-core ap. 20mA in active state
- ALU2 ap. 5mA during calculation
- reference clock unit ap. 90µA/MHz

Example: 1000 measurements per second, measuring time 1µs, measurement range 1, calibration and multiplication, 10MHz reference clock
current consumption TDC-core: the unit is 1ms/s active → 20µA
*current consumption reference clock:: 10MHz → 10*90µA = 0,9mA*
*current consumption ALU: 1000 calculations/s with 4µs/calculation = 40ms active time → 5mA*0,04 = 200µA*
In this mode the GP1 has a total current consumption of 1.2mA

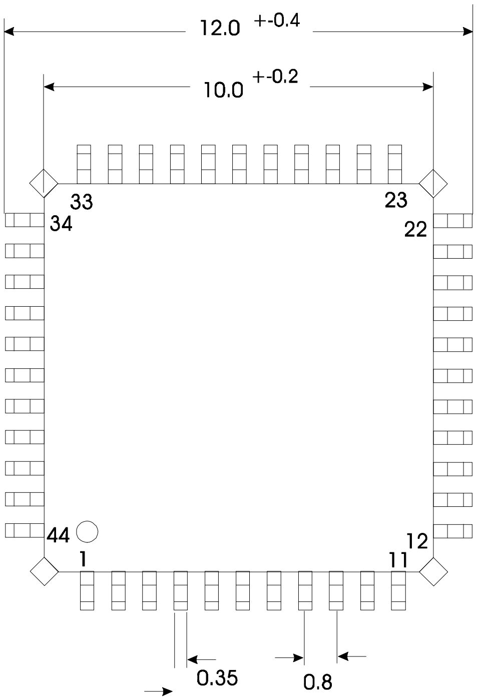
- Current consumption with resolution adjust

In this mode the current consumption of the reference clock and the ALU2 remain the same. The current consumption of the TDC-core and additionally the PLL increases to 25mA and dominates the total consumption. It should be noted that the consumption decreases linearly with the core voltage, so that it will depend on the adjusted resolution.

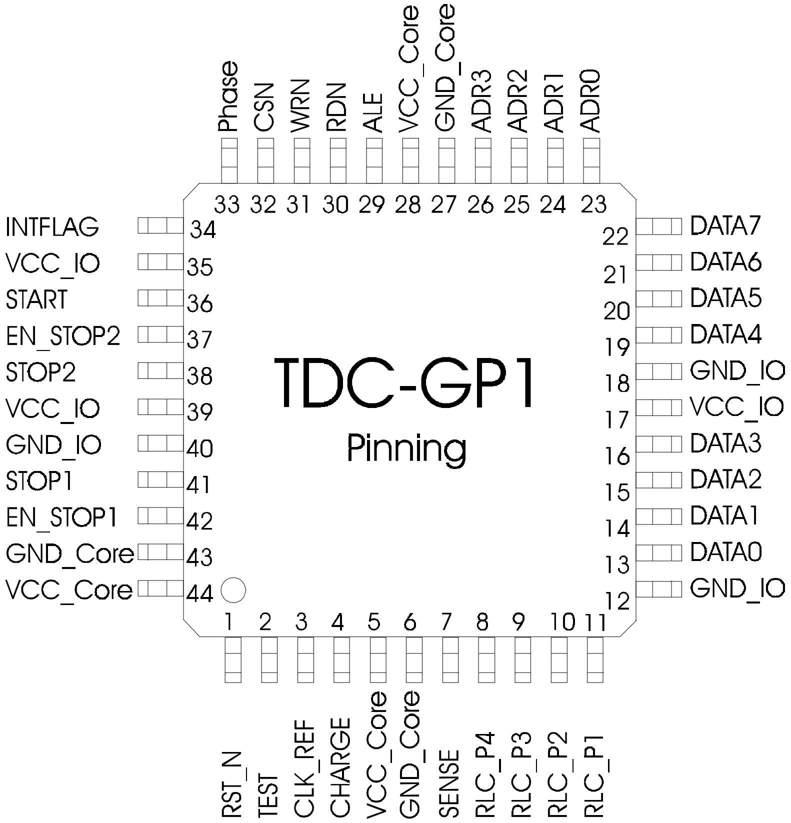
2.12.4 Package 44-TQFP

Available sockets:

Yamaichi
IC51-467.KS-11787
IC149-044-*52-55


12.0 +-0.4
10.0 +-0.2
33
23
34
22
44
12
1
11
0.35
0.8

2.12.5 Pinout


Phase
CSN
WRN
RDN
ALE
VCC_Core
GND_Core
ADR3
ADR2
ADR1
ADR0
33 32 31 30 29 28 27 26 25 24 23
INTFLAG 34
VCC_IO 35
START 36
EN_STOP2 37
STOP2 38
VCC_IO 39
GND_IO 40
STOP1 41
EN_STOP1 42
GND_Core 43
VCC_Core 44
22 DATA7
21 DATA6
20 DATA5
19 DATA4
18 GND_IO
17 VCC_IO
16 DATA3
15 DATA2
14 DATA1
13 DATA0
12 GND_IO
TDC-GP1
Pinning
1 2 3 4 5 6 7 8 9 10 11
RST_N
TEST
CLK_REF
CHARGE
VCC_Core
GND_Core
SENSE
RLC_P4
RLC_P3
RLC_P2
RLC_P1

2.12.6 I/O Buffer Types

The following buffer types were used for the I/O signals.

Names	**Direction**	**Buffer type**
RLC_P1 ... RLC_P4, CHARGE	OUTPUT	16 mA CMOS Tri State
SENSE	INPUT	CMOS Schmitt-Trigger
STOP1, STOP2, EN_STOP1, EN_STOP2 START, WRN, RDN, CSN, ALE, ADR0-3 RST_N, CLK_REF	INPUT	CMOS
PHASE	OUTPUT	4 mA CMOS
INTFLAG	OUTPUT	8 mA CMOS Slew Rate controlled
DATA 0 .. DATA 7	BIDIR	8 mA CMOS Slew Rate controlled

Attention:
None of the input buffers and I/O buffers has an internal pull up or pull down. All signals must therefore be connected and the data bus is not allowed to float for longer periods of time. Otherwise there may be danger that the buffer will oscillate. This may result in higher energy consumption and the loss of all functions of the GP1.

2.12.7 Design of the Power Supply

The TDC-GP1 is a fully digital device without analogous components. Because it uses the analogous gate delay for it's functioning, such analogous values as a good power supply are essential for a good measuring quality. At the beginning of a measurement current climbs from practical 0 within a few nanoseconds to a value of approx. 25 mA. This short-term current rise cannot be compensated by voltage regulators. A high capacitive and poorly inductive power supply is necessary. The size of the blocking capacities must primarily be brought into line with the maximum measurement time in the application. The maximum measurement time is the sum of all singles times of a measurement.

A good reference value for the blocking capacities is 30 µF per 1 µs measurement time.

Example: Suppose a 2 MHz precounter clock in measurement range 2. The absolute length of the time difference isn't important in measurement range 2. When adding all runtimes of the high speed measuring unit including calibration, we'll have 4 calibration clock cycles = 2 µs. Therefore a blocking capacity of 60 µF is useful.

It is recommended to divide these capacities into several components (e.q. 3*22µF) and to use capacities with low self-impedance and low serial resistance. The use of additional ceramic capacitors (e.q. 100 nF) may also be good, but no considerable effects could be observed. One has to take care of a good voltage distribution with low self-impedance on the PCB. Multilayer PCBs with separate layers for Vcc and GND give good results, but a careful layout on a 2 layer PCB is sufficient also.

2.12.8 MIN/MAX Timings

The times of the chip, and this includes resolution also, are subject to 3 different parameters

- tolerances in manufacturing process
- supply voltage variations
- temperature variations

The resulting times can be derived from

$$\mathbf{Tpd = T_{pd}(typ.) * K_p * K_v * K_T}$$

Kp = Prozesscoefficient
Kv = Voltagecoefficient
KT = Temperaturecoefficient

The following table applies to the process coefficient

Table: Kp

Process condition	Value
Best-Case	0,61
Typical	1.0
Worst-Case	1.4

The following table applies to the voltage

Table: Kv

VDD	Kv
5.5 V	0.94
5.0 V	1.00
4.5 V	1.07
3.3 V	1.39
3.0 V	1.54
2.7 V	1.74

The following table applies to the temperature

Table: Kt

Temp	Kt
125 °C	1.26
85 °C	1.15
70 °C	1.11
25 °C	1.00
-25 °C	0.87
-40 °C	0.82
-55 °C	0.79

Considering all parameters we have the following possible resolutions of the TDC-GP1

Best-Case	(-40 C, 5.5 V, Best-Case Process):	120 ps
Typical	(25 C, 5 V , typical process):	220 ps *
Worst-Case	(85 C, 4,5 V, Worst-Case Process):	380 ps

* The resolution mentioned in this manual as typical 250ps is a result of averaging over the last production lots (this is not identical to the typical process value).

With the help of above tables it's possible to calculate the resolution for any application and the expected operating conditions.

Example: the core voltage may be 4V at 25 °C. Regarding the process variations the following resolution values can be expected

*Best-Case: Tpd= 220ps * 0,61 * 1.20 * 1,0 = 161 ps*
*Typical: Tpd= 220ps * 1.0 * 1,20 * 1.0 = 264 ps*
*Worst-Case: Tpd= 220ps * 1.4 * 1,20 * 1.0 = 369 ps*

Remark: The Kv Factor of 1.20 at 4 Volts is interpolated from the data in the tables.

Such a big tolerance over the lots however is possible but very improbable. The resolution sways (out of experience) due to process changes between - 10 % and + 25 %.

Chips from one production lot sway about +- 5% around the lot's typical value.

3. Applications

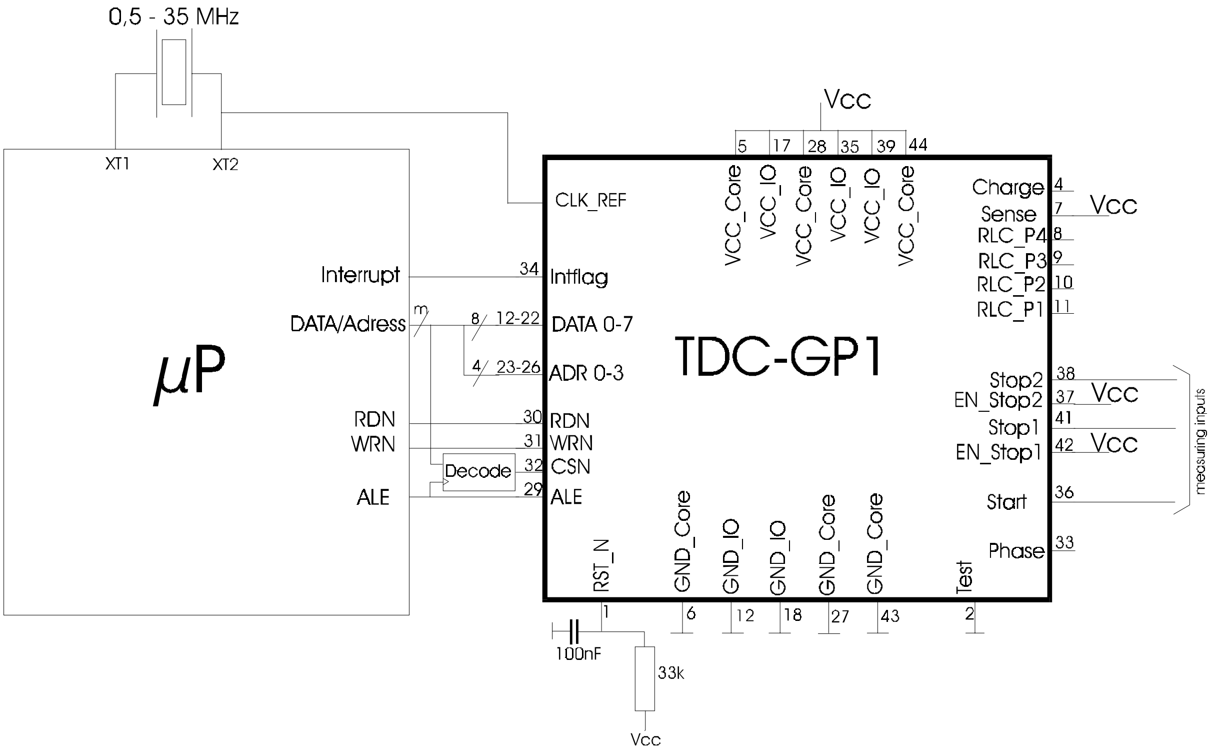
On the following pages you'll find some applications for the external circuitry of the TDC-GP1 and some software routines for typical examples. In this section no really new information is given. The aim is to enable the user to deepen the previous information.

3.1 Application 1

In this simple working example following parameters are used

- µP interface with common Data/Address bus
- no RLC measurement
- no Resolution Adjust

Figure 19: Principle circuit


0,5 - 35 MHz
XT1
XT2
µP
Interrupt
DATA/Adress
RDN
WRN
ALE
Decode
m
8
4
CLK_REF
34 Intflag
12-22 DATA 0-7
23-26 ADR 0-3
30 RDN
31 WRN
32 CSN
29 ALE
TDC-GP1
Vcc
5 17 28 35 39 44
VCC_Core
VCC_IO
VCC_Core
VCC_IO
VCC_IO
VCC_Core
Charge 4
Sense 7
Vcc
RLC_P4 8
RLC_P3 9
RLC_P2 10
RLC_P1 11
Stop2 38
EN_Stop2 37
Vcc
Stop1 41
EN_Stop1 42
Vcc
Start 36
Phase 33
measuring inputs
RST_N
GND_Core
GND_IO
GND_IO
GND_Core
GND_Core
Test
1 6 12 18 27 43 2
100nF
33k
Vcc

Additional remarks:

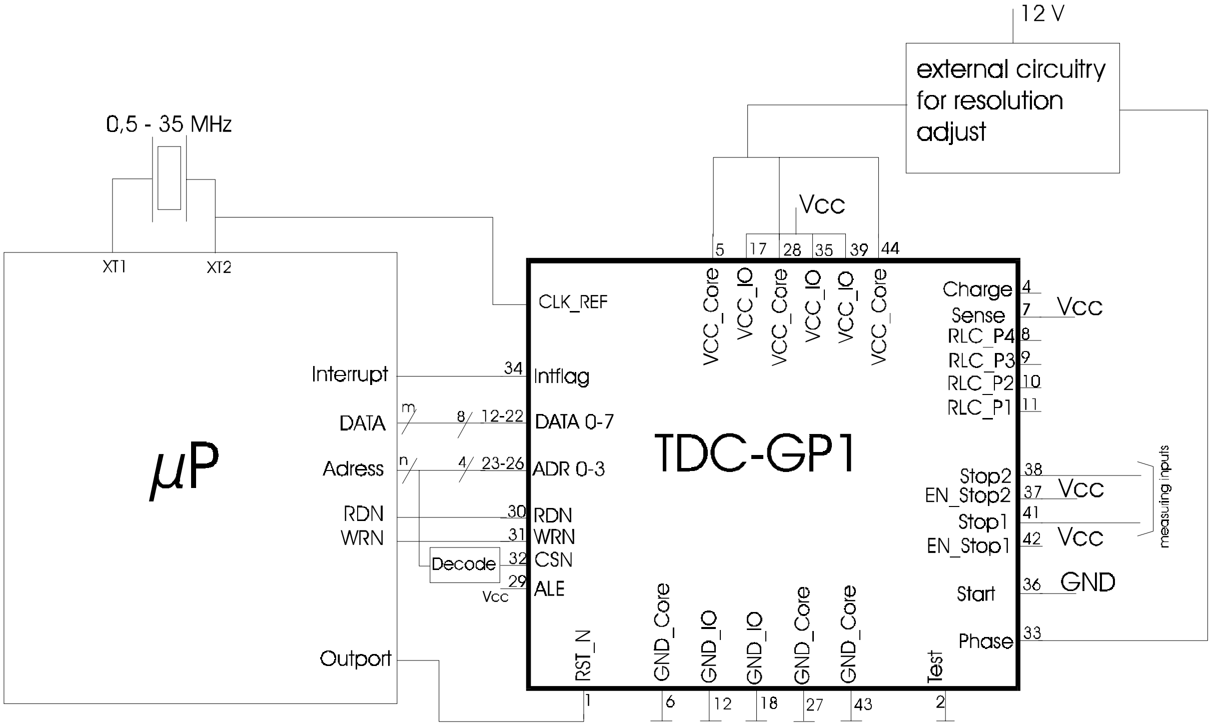
- without Resolution Adjust Vcc and GND Pins of the Core and the I/O Buffers can be connected together.
- the possible operating voltage is 2,7 V ... 5,5 V
- if the RLC is not used, Sense (Pin 7) must be driven by Vcc
- RST_N (low active) can also be driven directly by Vcc. Power on Reset via software possible.
- not connected pins may float

3.2 Application 2

In this simple working example following parameters are used

- µP interface with separated Data/Address bus
- no RLC measurement
- Resolution Adjust Modus is active

Figure 20: Principle circuit


12 V
external circuitry for resolution adjust
0,5 - 35 MHz
Vcc
5
17
28
35
39
44
XT1
XT2
µP
Interrupt
DATA
Adress
RDN
WRN
Outport
m
n
34
8
12-22
4
23-26
30
31
32
29
Decode
Vcc
CLK_REF
Intflag
DATA 0-7
ADR 0-3
RDN
WRN
CSN
ALE
TDC-GP1
VCC_Core
VCC_IO
VCC_Core
VCC_IO
VCC_IO
VCC_Core
Charge 4
Sense 7
Vcc
RLC_P4 8
RLC_P3 9
RLC_P2 10
RLC_P1 11
Stop2 38
EN_Stop2 37
Vcc
Stop1 41
EN_Stop1 42
Vcc
measuring inputs
Start 36
GND
Phase 33
RST_N 1
GND_Core 6
GND_IO 12
GND_IO 18
GND_Core 27
GND_Core 43
Test 2

Additional Remarks:

- In the Resolution Adjust mode Vcc of the Core and the I/Os must be separated
- for detailed schematic of the external resolution adjust circuit please refer 2.6.2 (page 24)
- Start Input (pin 36) without any function; must be connected to ground
- the core voltage can be driven from 2.7 V.... 5.5 V
- If the RLC is not used, Sense (Pin 7) must be driven by Vcc
- not connected pins may float

3.3 Single Measurement MB2

The following C-routine will give an example how to setup the TDC-GP1 for single measurements in measurement mode 2:

```
Configuration:                                Comment:

output_byte(Reg7,0x00);                       Disable of stop inputs
output_byte(Reg11,0x07);                      Init TDC and ALU
output_byte(Reg0,0x78);                       Measurement range 2
                                              autocalibration + multiplication
output_byte(Reg2,0x21);                       FC1-FC2 -> Stop1 Chan.1 - Start
output_byte(Reg4,0xC0);                       SEL_CLK_TDC = 6
                                              Range = 2^16*50ns*64 = 209ms
output_byte(Reg7,0x02);                       enable 2 hits on channel 1
```

Measurement:

```
while(!quit)
{
    output_byte(Reg11,0x07);                  Init TDC and ALU
    valid = 0;
    while(valid==0)
    {
        valid=input(INTFLAG);                 Check Interrupt Flag
    }
    nk0=input_byte(Reg0);                     Lower byte  xxxx.xxXX
    nk1=input_byte(Reg0);                     Higher byte xxxx.XXxx
    vk0=input_byte(Reg0);                     Lower byte  xxXX.xxxx
    vk1=input_byte(Reg0);                     Higher byte XXxx.xxxx

    vk1=vk1*256;                              shift left
    vk1=vk1|vk0                                           XXXX.xxxx
    nk1=nk1*256;                              shift left
    nk1=nk1|nk0                                           xxxx.XXXX

    result = 50.0*((float)(vk1)+(float)(nk1)/65536.0);
                                              20MHz reference clock -> 50ns
    printf("result=%6.3fns\n",result);        Print result
}                                             end while
```

3.4 Reading multihits

When writing software for multihit applications this should be regarded:

As soon as a measurement is finished, the ALU is starting the calculation defined in Register 2. The result is written to the output register.
Afterwards, as soon as a new value is written to Register 2, the ALU starts for the new calculation. The result is written to the next result register address.
The timing could be as follows:

```
Enable 3 hits on channel1
Reg2: 0x01 Hit 1 - Start
Init TDC
Check INT_FLAG (wait until the measurement is finished)
Reg2: 0x02 Hit 2 - Start
Wait for 3us (time, the ALU needs for calculation)
Reg2: 0x03 Hit 3 - Start
Wait for 3us (time, the ALU needs for calculation)
Set address pointer to zero
With calibrated values read 12 times (4 Bytes each value, the addresses are
automatically incremented)
```

More information on writing software can be found in the ATMD-manual.

4. Measurement Results and Diagrams

The following pages show the real performance of the TDC-GP1. The power and the limits of the device are pointed out. All results presented here are evaluated with the prototypes of the GP1 implemented in the ATMD measurement system.

4.1 Meanings of the Terms 'Precision' and 'Resolution'

At first, we want to make some remarks on the meaning of the two terms.
When talking about resolution, we mean the smallest digital unit or LSB of the time-to-digital converter (in analogy to ADCs). This is in conformity with electronics' usage and different to scientific usage.
The precision of a measuring is defined by different parameters, in detail:

4.1.1 Standard Deviation

The standard deviation is the standard square fault about a row of measurement results to the arithmetical mean average value of these measurement results. It is a good value for the noise which is caused by quantization effects and other randomly distributed sources of inaccuracy. If the assumption of statistically distributed results is fulfilled, the standard deviation can be decreased by averaging with the square root of the number of samples.

For example: If it is possible to take the average value of 100 measurements, the standard deviation of these value will be 1/10th (square root of 100) of the standard deviation of a single value.

4.1.2 Systematic Errors

Systematic errors belong to measured values that appear at the same point of the characteristic curve for all the time. When measuring the same time interval, also the measuring errors have the same quantity.
Values with systematic errors aren't distributed around the averaged value by chance. Therefore these errors can't be eliminated by averaging. They are the 'more unpleasant' faults which are very heavy to remove.

4.1.2 Offset Errors

The offset error is a constant error value which is added/subtracted from the measuring value over the complete measurement range. Offset errors belong to the systematic errors but nevertheless they are described separately here.

4.2 Attainable Standard Deviations of the TDC-GP1

The attainable results for the standard deviation are dependent on the used measuring mode.
It can be calculated with the following standard deviations of the measurement results in the different modes.

■ Measurement range 1 without Resolution Adjust normal resolution:	ca. 0,5 - 0,6 LSBs
■ Measurement range 1 without Resolution Adjust high resolution:	ca. 0,6 - 0,7 LSBs
■ Measurement range 2 without Resolution Adjust normal resolution:	ca. 0,7 - 0,8 LSBs
■ Measurement range 2 without Resolution Adjust high resolution:	ca. 0,8 - 0,9 LSBs
■ Measurement range 1 with Resolution Adjust normal resolution:	ca. 0,7 - 0,8 LSBs
■ Measurement range 1 with Resolution Adjust high resolution:	ca. 0,8 - 0,9 LSBs

Please note:

These values can be drastically improved using averaging. (as mentioned above)

When working without Resolution Adjust it is necessary that the measured time difference has a jitter of several LSBs to enable this effect.

If this is not the case, the auto noise unit can be used to get a pseudo jitter. With this method an improvement of the result in the range of factor 5-10 can be achieved. Beyond this, systematic errors of the Auto Noise unit themselves are noticeably and prevent an increase of the measuring precision.

Optimal stochastic prerequisites are available with Resolution Adjust. In this mode it is possible by averaging to increase the precision of the result considerably. **A standard deviation of less than 1 ps can be achieved**. As well it isn't necessary that the incoming signal is noisy. The GP1 produces the necessary statistics by itself in this mode.

4.3 Offset Errors of the GP1

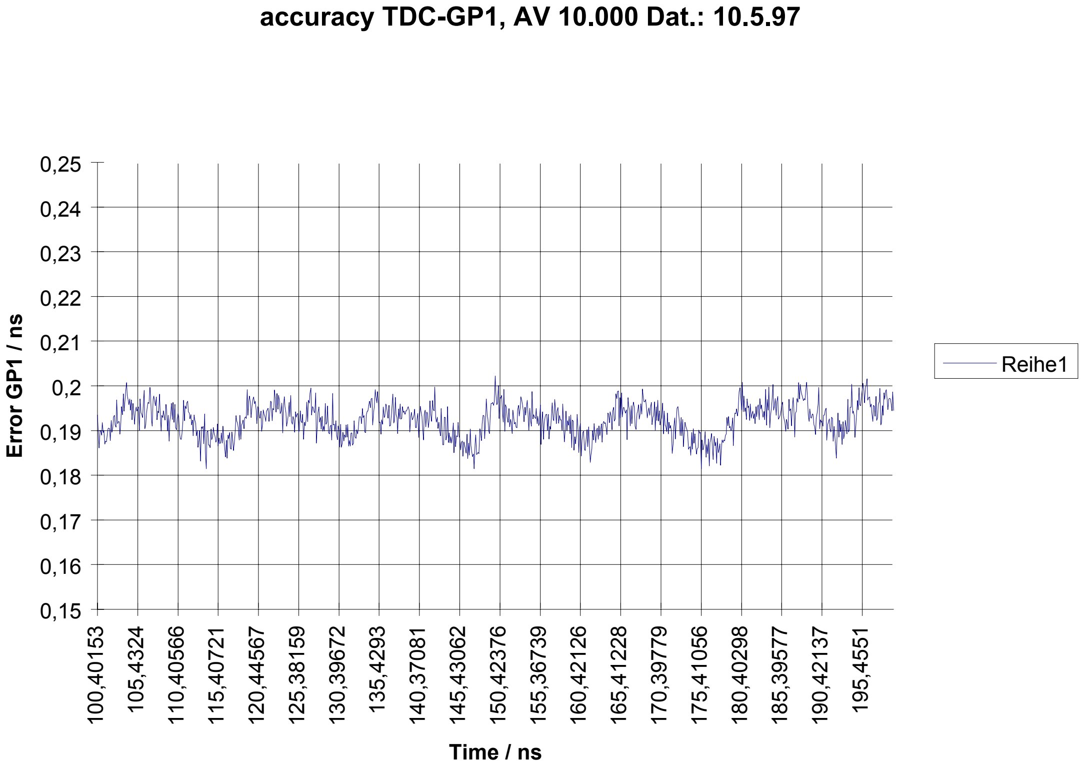
Also for the offset errors one must precisely distinguish between the measuring modes. It can be calculated with following offsets depending on the operating mode

- Measurement range 1 without Resolution Adjust normal resolution: < 1,2 LSB
- Measurement range 1 without Resolution Adjust high resolution: < 2,0 LSB
- Measurement range 2 without Resolution Adjust normal resolution: < 0,5 LSB
- Measurement range 2 without Resolution Adjust high resolution: < 0,8 LSB
- Measurement range 1 with Resolution Adjust normal resolution: < 0,3 LSB
- Measurement range 1 with Resolution Adjust high resolution: < 0,1 LSB

Pay attention to the principle difference here between the modes using or not using Resolution Adjust operation. Without Resolution Adjust the offset is temperature-dependent and is held within the mentioned ranges by calibration. With Resolution Adjust the offset is much more stable and less sensitive to temperature fluctuations. The temperature drift is less than approx. 0.1 LSB in normal resolution over the whole temperature range and with high resolution even less than approx. 0.03s LSB. The offset then is nearly independent of temperature fluctuations!!

4.4 Systematic Errors of the GP1

Figure 21



Above diagram shows the measured deviation of the GP1 in comparison to a reference device in the time domain of 100 -- 200 ns. The GP1 was driven with Resolution Adjust and normal resolution. To be able to recognize systematical errors, high averaging rates are necessary to filter out the effects of quantization noise. An averaging rate of 10.000 was chosen. Note the subdivision of the Y-axis into 10ps/Div. There are systematic deviations in the characteristic of the curve of approx. 10 ps peak-to-peak.

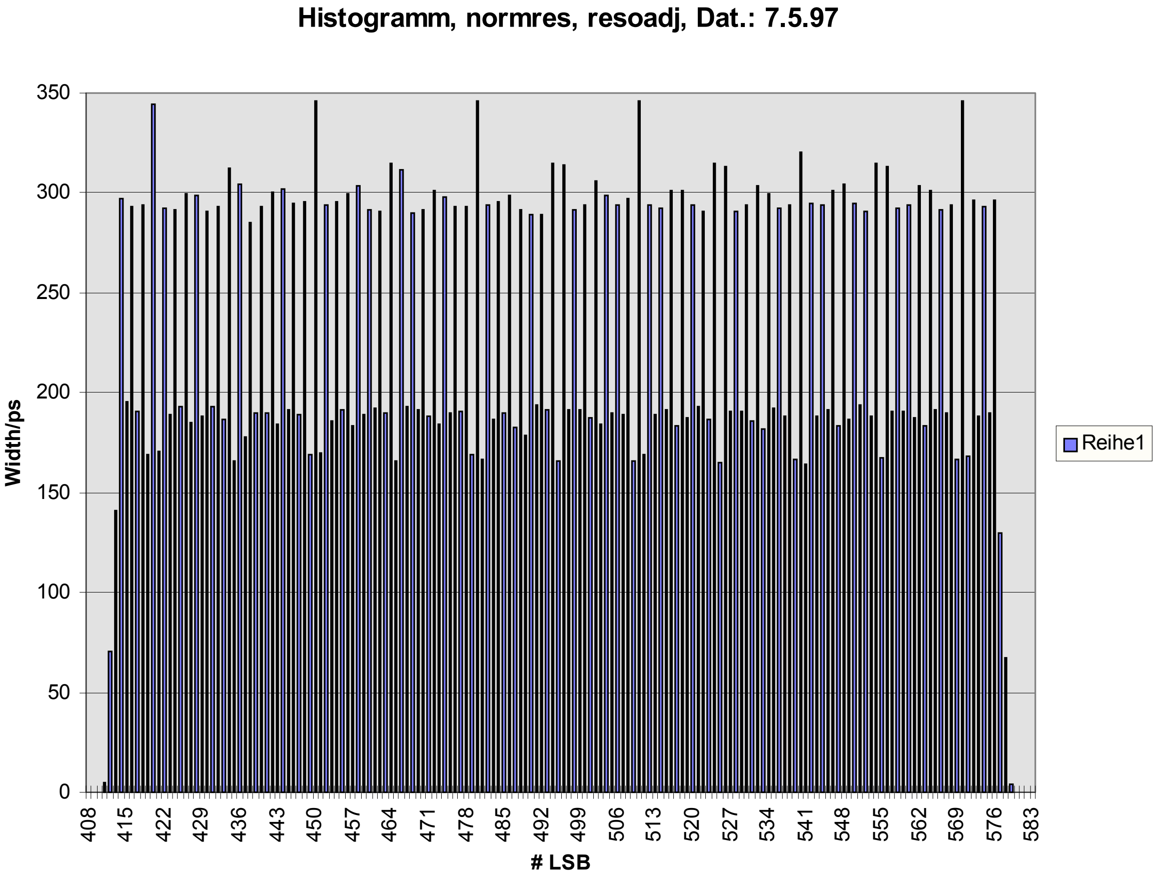
Detailed examinations have turned out that these small faults don't come from the GP1 but from the reference device obviously. We can state therefore, that the systematic errors of the GP1 can't be measured because they are lower than the achievable precision of our reference equipment. In any case they are clearly smaller than 10 ps. Therefore it makes sense to increase the accuracy of the result by averaging when working with the GP1.

4.5 Histograms

For some applications in research and industry the GP1 is used for the building histograms. In this case the differential non-linearity is primarily of great importance. It is recommended to use the Resolution Adjust mode. The better results will be achieved.

Diagram 1 shows a histogram with normal resolution and resolution adjust. Clearly the periodicity of the width of the single LSBs can be recognized. A narrow LSB follows a broad LSB and vice versa. Also further periodical deviations are seen, recurring all 30 LSBs. The differential nonlinearity in this mode is approx. 50 %.

Figure 22:



If a very good differential nonlinearity is needed, the half resolution mode with resolution adjust should be used. This mode adds 2 neighboring LSB inside the GP1. This mode is selectable via the control registers.

The result is shown in Figure 23. The differential nonlinearity goes down to approx. 2 %. The disadvantage is the doubling of the resolution, in this case on 485 ps. The quality of the histogram is very good now and no wishes should remain.

Anyway, high resolution mode and half resolution mode can be combined. The result can be seen in Figure 25: it's a 1-channel TDC with typ. 250ps LSB and a differential non-linearity better than 10%.

Figure 23: Histogram, halfres, resadj.

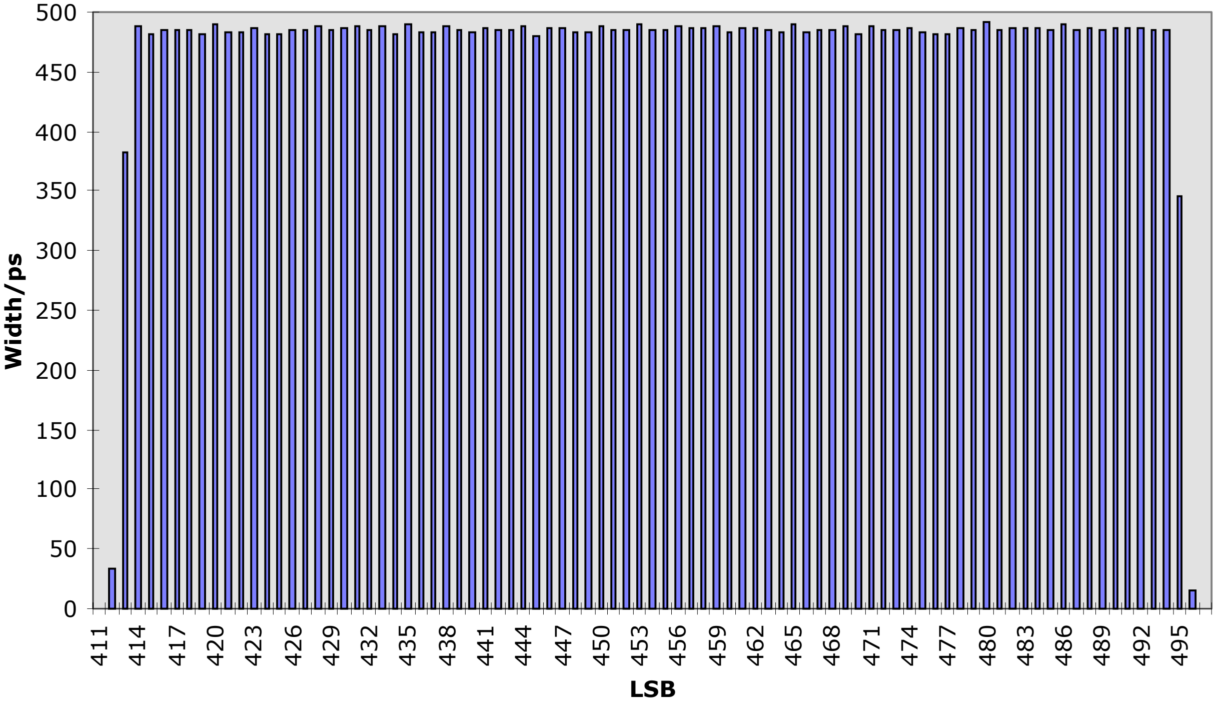
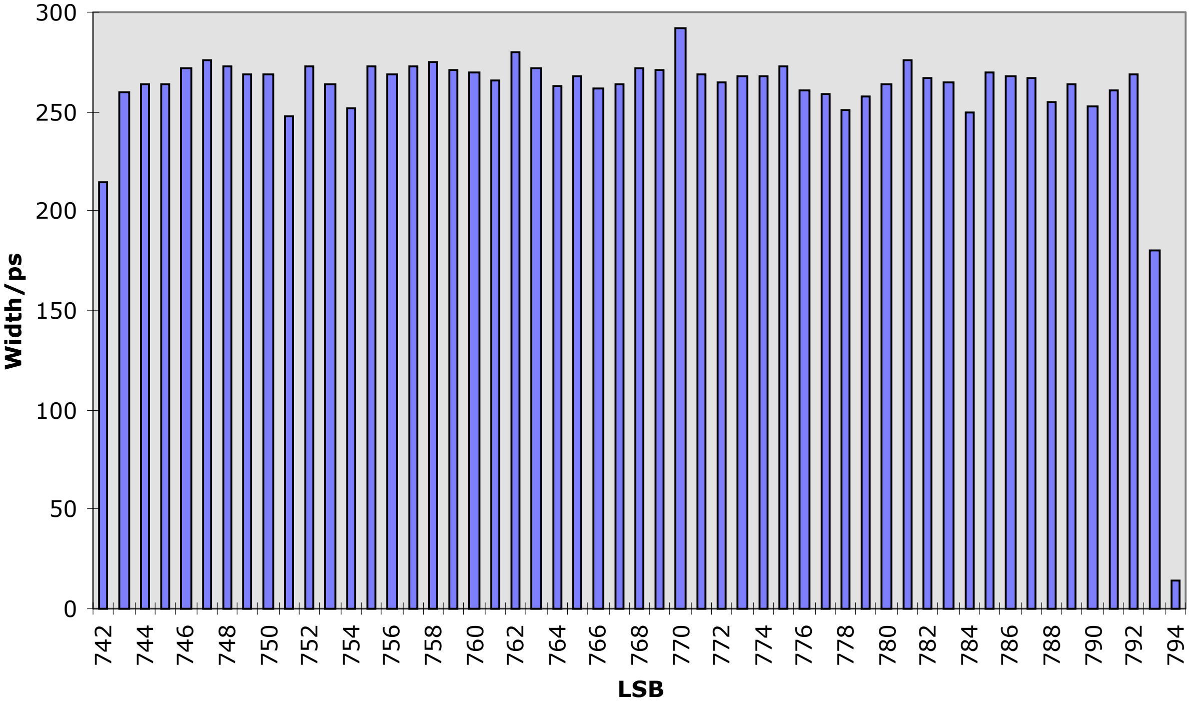


Figure 24: Histogram, half+high res, resoadj.



5. Known Problems and Solutions

5.1 Generation of the Calibration Values

Concerns: - separate calibration with control register 0 Bit 7
- automatic calibration with control register 0 Bit 3

Description:

If a calibration run is finished and there is a new start pulse before the TDC is initialized, the measurement unit will start measuring again. Stop hits eventually appearing now won't be limited by time out or hit enable(register 7). If the number of stop pulses is high enough even the calibration values will be overwritten.

This happens only for a further start pulse. If only stop pulses come after a calibration, they will be ignored.

This problem doesn't concern the Resolution Adjust mode.

Example:
A typical case where this leads to considerable problems, is the measuring of a frequency with the TDC-GP1. In this case normally the clock to measure is given on start and stop inputs simultaneously. If separate calibration or autocalibration is in use, further start pulses and stops pulses will hit the TDC after calibration. These events generate values which overwrite the correct values in the value registers and calibration value registers

Solution of the problem:

In the case mentioned above where you cannot control the start pulses, do not use auto calibration.

A secure method to get correct calibration values is:

1. Set hit enables in control register 7 to 0
2. Do separate calibration with control register 0
3. after end of calibration initialize the TDC with Address 11
4. set hit enables to required values

Program example in Borland C from the application software of the ATMD

```
// secure calibration of the TDC-GP1
outport(adr_cntrl2,7);    // disable Hits
outport(adr_tdc,0x00);
outport(adr_cntrl2,11);   // Reset
outport(adr_tdc,0x03);
outport(adr_cntrl2,0);    // doing separate calibration
outport(adr_tdc,0x80):
wait a minimum of 3 calibration clock cycles
outport(adr_cntrl2,7);    // enable Hits
outport(adr_tdc,0x09);
wait a minimum of 20 calibration clock cycles
// end of calibration
```

5.2 Calculation Errors in Resolution Adjust Mode

Concerns: half resolution in the Resolution Adjust mode
high resolution in the Resolution Adjust mode
high resolution with half resolution in the Resolution Adjust mode

There are no errors with normal resolution.

Description:

If in resolution adjust mode the half resolution bit or the high resolution bit is set (control register 7 bit 7 or control register 1 bit 6), in some cases errors may occur in the ALU.

Half Resolution
The failure has the effect that the result is 15.360 LSBs too big. Only some of the results are wrong. The failure can be recognized as no results bigger as 7.680 LSBs are possible. The wrong results are all in the range of 7.680 to 15.360 LSBs. The error occurs with a probability of approx. 0.03 % .

Example:
Select value: 6.500 → Result correct
Select value: - 3.000 → Result correct
Select value: 8.500 → error; Correct result: 8.500-15.360= - 6.860

High Resolution:
The failure appears inform of results that are 15.360 LSBs too small. Only some of the results are wrong. The fault can be recognized as no results less than 0 are possible. All wrong results are in the negative range. The error occurs with a probability of approx. 0.03 % .

Example:
Selected value: 6.500 → Result correct
Selected value: -1.000 → error; Correct result: -1.000+15.360 = 14.360

High Resolution with Half Resolution:
The failure is seen as the result is 7.680 LSBs too big. Only some of the results are wrong.
The failure can be recognized as no results bigger 7.680 are possible. All wrong results are in the range from 7.680 LSBs to 15.360 LSBs. The error occurs with a probability of approx. 0.03 % .

Example:
Selected value: 6.500 → Result correct
Selected value: 8.500 → error; correct result: 8.500-7.680 = 820

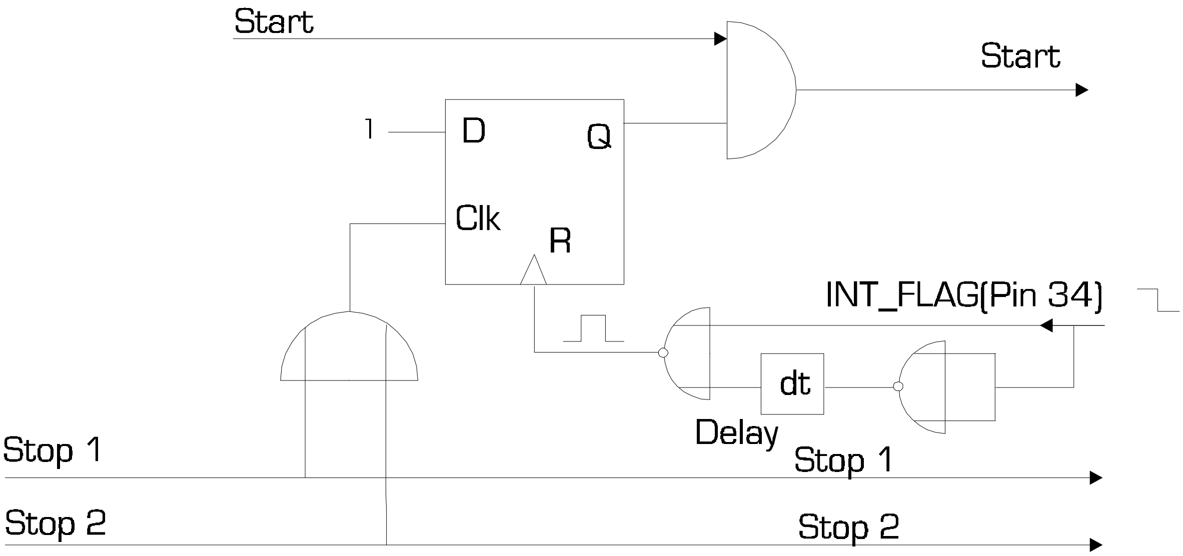
Solution:
Check results on retention of above ranges and use the according rules for correction.

5.3 Retrigger

Description:
In retrigger mode a start pulse (no. 2) coming after a stop pulse will be ignored. If there is a further stop pulse after the start pulse (no. 2), the next start pulse (no. 3) will also be ignored, but by mistake the status registers will be reset. This will bother in multihit applications because the number of measured hits is not available.

Solution:
An external circuit is necessary that disables the start input as soon as a stop pulse arrives. The start input must be enabled with the next TDC-INIT.

Figure 25



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7 Quick Reference

7.1 Elec. Characteristics

Recommended Operating conditions

Parameter	Symbol	min.	max.	Unit
Supply Voltage	VDD	2.7	5.5	
Input Signal Voltage	Vi	0	VDD	V
Ambient Temperature	Ta	-40	+85	C
HI Input Voltage	VIH	0.7 * VDD	VDD	V
LOW Input Voltage	VIL	0	0.3 * VDD	V
Pos. trigger Spg	Vp		0,8*VDD	V
Neg. trigger Spg	Vn	0,2*VDD		V
Hysteresis	Vh	1.0		V
Input Rise/Fall Time	Tr, tf	0	200	ns
Input Schmitt Rise/Fall	Tr, tf	0	10	ms

Absolute Maximum Ratings

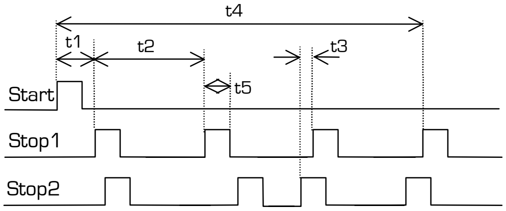
Parameter	Symbol	min.	max.	Unit
Supply Voltage	VDD	-0.3	7.0	V
Input Signal Voltage	Vi	-0.3	VDD+0.3V	V
Input Pin Current		-10.0	+10.0	mA
Storage Temperature	Tst	-55	+125	C
Lead Temperature			300 (10s)	C

7.2 Pin Description

Pin	Symbol	Description
1	RST_N	Reset (low active)
2	TEST	Test pin, must be connected to GND
3	CLK_REF	Input external reference clock
4	CHARGE	Charge pin for RLC measurements
5	VCC_CORE	Core supply voltage
6	GND_CORE	Core Ground
7	SENSE	Schmitt trigger input for RLC-measurements
8	RLC_P4	Port 4 for RLC-measurement
9	RLC_P3	Port 3 for RLC-measurement
10	RLC_P2	Port 2 for RLC-measurement
11	RLC_P1	Port 1 for RLC-measurement (Reference)
12	GND_IO	Ground of IO Ports
13-16	DATA0- DATA3	Data bus
17	VCC_IO	Supply voltage IO ports
18	GND_IO	Ground IO ports
19-22	DATA4-DATA7	Data bus
23-26	ADR0-ADR3	Address bus
27	GND_Core	Core Ground
28	VCC_CORE	Core supply voltage
29	ALE	Address latch enable (high active)
30	RDN	Read (low active)
31	WRN	Write (low active)
32	CSN	Chip select (low active)
33	Phase	Phase out for regulation in res. Adj. mode
34	INTFLAG	Interrupt flag (high active)
35	VCC_IO	Supply voltage IO ports
36	START	Start input
37	EN_STOP2	enable stop input 2 (high active)
38	STOP2	Stop input 2
39	VCC_IO	Supply voltage IO ports
40	GND_IO	Ground IO ports
41	STOP1	Stop 1 input
42	EN_STOP1	enable stop input 1 (high active)
43	GND_Core	Ground core
44	VCC_Core	Supply voltage core

7.3 Timings

Timings (@ 25°C, 5V):	min.	typ.	Max.	Unit
Resolution (LSB)	134	250	308	ps
Standard deviation				
MB1, normal resolution		0.6		LSB
MB1, high resolution		0.7		LSB
MB2, normal resolution		0.8		LSB
MB2, highresolution		0.9		LSB
Resolution adjust, normal res.		0.9		LSB
Resolution adjust, high resolution		0.9		LSB
Offset				
MB1, normal resolution			1.2	LSB
MB1, high resolution			2.0	LSB
MB2, normal resolution			0.5	LSB
MB2, highresolution			0.8	LSB
Resolution adjust, normal res.			0.3	LSB
Resolution adjust, high resolution			0.1	LSB
Integral non-linearity		0		LSB
Differential non-linearity				LSB
MB1, normal resolution				LSB
MB1, high + half resolution				LSB
Resolution adjust, normal res.		.25		LSB
Resolution adjust, normal res.		,03		LSB
INIT TDC	18	30	42	ns
INIT ALU	18	30	42	ns
Power On Reset	30	50	70	ns



Measurement range 1, normal resolution:

Timings (@ 25°C, 5V):		min.	typ.	Max.
t1	Minimum time difference		3ns	4.2ns
t2	Double pulse resolution one channel		15ns	21ns
t3	Double pulse resolution between 2 channels		0ns	
t4	Maximum time interval (30,720*Resolution)		7.6us	
t5	Minimum pulse width		2.5ns	4ns
	Number of channels		2	
	Number of hits per channel		4	
	start available		yes	

Measurement range 1, high resolution:

Timings (@ 25°C, 5V):		min.	typ.	Max.
t1	Minimum time difference		3ns	4.2ns
t2	Double pulse resolution one channel		15ns	21ns
t4	Maximum time interval (15,360*Resolution)		3.8us	
t5	Minimum pulse width		2.5ns	4ns
	Number of channels		1	
	Number of hits per channel		4	
	Start available		yes	

Measurement range 2, normal resolution:

Timings (@ 25°C, 5V):		min.	typ.	max.
t1	Minimum time difference	1.5*CAL_CLK+25ns		
t2	Double pulse resolution one channel	1.5*CAL_CLK+25ns		
t4	Maximum time difference	2^16*CAL_CLK		
t5	Minimum pulse width		2.5ns	4ns
	Number of channels		1	
	Number of hits per channel		4	
	Start available		yes	

Measurement range 2, high resolution:

Timings (@ 25°C, 5V):		min.	typ.	max.
t1	Minimum time difference	1.5*CAL_CLK+25ns		
t2	Double pulse resolution one channel	1.5*CAL_CLK+25ns		
t4	Maximum time difference	2^16*CAL_CLK		
t5	Minimum pulse width		2.5ns	4ns
	Number of channels		1	
	Number of hits per channel		3	
	Start available		yes	

CAL_CLK = Tref * SEL_CLK_TDC (control register 4)

Resolution Adjust Mode, normal resolution:

Timings (@ 25°C, 5V):		min.	typ.	max.
t2	Double pulse resolution one channel		15ns	21ns
t3	Double pulse resolution between 2 channels		0ns	
t4	Maximum time interval (15,360*Resolution)		3.8us	
t5	Minimum pulse width		2.5ns	4ns
	Number of channels		2	
	Number of hits per channel		4	
	Start available		no	

Resolution Adjust Mode, high resolution:

Timings (@ 25°C, 5V):		min.	typ.	Max.
t2	Double pulse resolution one channel		15ns	21ns
t3	Double pulse resolution between 2 channels		0ns	
t4	Maximum time interval (7.680*Resolution)		1.9us	
t5	Minimum pulse width		2.5ns	4ns
	Number of channels		1	
	Number of hits per channel		4	
	Start available		no	

6.4 Registers

Write Registers and Addresses

Register 0		Address: 0
Bit	**Name**	**Description**
7	CAL	initializes a separate CAL run→ Update of CAL-values in the calibration value registers
6	CALIBRATE	instructs the ALU to do a calibration calculation
5	MULTIPLICATE	instructs the ALU to do a multiplication
4	MESSB2	'1' switches to measurement with predivider
3	EN_CAL_AUTO	1= automatic calibration after measurement
2	EDGE_STP2	selects slope sensitivity Stop2-Input 0=rise
1	EDGE_STP1	selects slope sensitivity Stop1-Input 0=rise
0	EDGE_STA	selects slope sensitivity Start-Input 0=rise

Register 1		Address: 1
Bit	**Name**	**Description (Remark: optimum value for ADJ<5:0> = 0x0d)**
7	RESO_ADJ	switches to resolution adjust mode
6	HIGH_RES	switches to high resolution mode
5	ADJ<5>	adjustment bit 5 of high resolution mode
4	ADJ<4>	adjustment bit 4 of high resolution mode
3	ADJ<3>	adjustment bit 3 of high resolution mode
2	ADJ<2>	adjustment bit 2 of high resolution mode
1	ADJ<1>	adjustment bit 1 of high resolution mode
0	ADJ<0>	adjustment bit 0 of high resolution mode

Register 2		Address: 2
Bit	**Name**	**Description**
7	HIT2_IN<3>	channel select for upper Nibble: 0= channel1, 1=channel2
6	HIT2_IN<2>	hit-no. for channel selected in bit 7
5	HIT2_IN<1>	hit-no. for channel selected in bit 7
4	HIT2_IN<0>	hit-no. for channel selected in bit 7
3	HIT1_IN<3>	channel select for lower Nibble: 0= channel1, 1=channel2
2	HIT1_IN<2>	hit-no. for channel selected in bit 3
1	HIT1_IN<1>	hit-no. for channel selected in bit 3
0	HIT1_IN<0>	hit-no. for channel selected in bit 3

Description of nibbles in detail

HITx_IN<3>	HITx_IN<2>	HITx_IN<1>	HITx_IN<0>	Number of Hits
0	0	0	0	Start
0 or 1	0	0	1	1. Hit of channel 1 or 2
0 or 1	0	1	0	2. Hit of channel 1 or 2
0 or 1	0	1	1	3. Hit of channel 1 or 2
0 or 1	1	0	0	4. Hit of channel 1 or 2
0 or 1	1	1	0	Cal 1 of channel 1 or 2
0 or 1	1	1	1	Cal 2 of channel 1 or 2

Register 3		Address: 3
Bit	**Name**	**Description**
7	FAK_PLL<7>	MSB adjustment of PLL
6	...	...
5	...	
4	...	
3	...	
2	...	
1	...	...
0	FAK_PLL<0>	LSB adjustment of PLL

Register 4		Address: 4
Bit	**Name**	**Description**
7	SEL_CLK_TDC<2>	divider for calibration clock of TDC
6	SEL_CLK_TDC<1>	...
5	SEL_CLK_TDC<0>	...
4	NEG_PH_PLL	Negotiation of phase outputs of PLL (has to be '1' if the recommended circuit is used)
3	SET_PAR_PLL	1=Track mode of PLL (Set Par Modus)
2	SEL_CLK_PLL<2>	divider for reference clock of PLL
1	SEL_CLK_PLL<1>	...
0	SEL_CLK_PLL<0>	...

Register 5		Address: 5
Bit	**Name**	**Description**
7	RLC_NR<2>	sets the number of RLC-ports to be measured
6	RLC_NR<1>	or the number of the port
5	RLC_NR<0>	"
4	SINGLE_EN	single port measur. = 1, 0= all ports 1 to n
3	C_SEL	measure capacitors = 1
2	SEL_CLK_RLC<2>	clock divider for RLC-unit
1	SEL_CLK_RLC<1>	"
0	SEL_CLK_RLC<0>	"

Register 6		Address: 6
Bit	**Name**	**Description**
7	INT_SEL	Interrupt Select (0= ALU ready, 1= Overflow)
6	QUEUING	Enable Queuing in measurement range 1
5	RETRIG_EN	Enable retrigger mode
4	NOISE_EN	Noise Enable
3	RLC_EN	starts RLC measurement
2	USE_TRANS	1= RLC-unit uses external transistor
1	SPEED<1>	sets frequency of BIGALU (default: lowest speed)
0	SPEED<0>	"

Register 7		Address: 7
Bit	**Name**	**Description**
7	HALF_RES	Half resolution
6	EN_SUI	Enable spike suppression at RDN
5	EN_HIT2<2>	number of allowed hits on channel 2 (max. 4)
4	EN_HIT2<1>	"
3	EN_HIT2<0>	"
2	EN_HIT1<2>	number of allowed hits on channel 1 (max. 4)
1	EN_HIT1<1>	"
0	EN_HIT1<0>	"

Register 8-10	Address:8-10
Register 8	multiplication factor<7..0>
Register 9	multiplication factor <15..8>
Register 10	multiplication factor <23..16>

Register 11		Address 11:
Bit	**Name**	**Description**
7	POR.	Power On Reset (1)
6	POR.	Power On Reset (0)
5	POR.	Power On Reset (1)
4	POR.	Power On Reset (0)
3	n.c.	
2	CLK_NOISE	Clock for PRBS counter in auto noise unit
1	INIT_BIGALU	Init for Bigalu unit
0	INIT_TDC	Init for TDC unit

Read registers and addresses

	Name	No.Bits	Description	calibrated data
0	ERG_REG0	16	Result register 1	after-decimal 0
1	ERG_REG1	16	Result register 2	pre-decimal 0
2	ERG_REG2	16	Result register 3	after-decimal 1
3	ERG_REG3	16	Result register 4	pre-decimal 1
4	ERG_REG4	16	Result register 5	after-decimal 2
5	ERG_REG5	16	Result register 6	pre-decimal 2
6	ERG_REG6	16	Result register 7	after-decimal 3
7	ERG_REG7	16	Result register 8	pre-decimal 3
8	STAT1	8	Status register 1	
9	STAT2	8	Status register 2	
A	REF_PLL	8	Reference value of the PLL that is won in a SET_PAR run	

Statusregister 1		Address: 8
Bit	**Name**	**Description**
7	PLL_LOCK	Indicates whether PLL has locked
6	OFL	Overflow of measuring unit
5	HIT2_TDC<2>	Indicates number of present hit on channel 2
4	HIT2_TDC<1>	Indicates number of present hit on channel 2
3	HIT2_TDC<0>	Indicates number of present hit on channel 2
2	HIT1_TDC<2>	Indicates number of present hit on channel 1
1	HIT1_TDC<1>	Indicates number of present hit on channel 1
0	HIT1_TDC<0>	Indicates number of present hit on channel 1

Statusregister 2		Address: 9
Bit	**Name**	**Description**
7	N.C.	not used
6	N.C.	not used
5	RLC_END	End of RLC-measurement
4	Multiply	Indication of multiplication (=Bit5 of register0)
3	Calibrate	Indication of calibration (=Bit6 of register 0)
2	LD_REGS<2>	pointer position in result register
1	LD_REGS<1>	pointer position in result register
0	LD_REGS<0>	pointer position in result register

Clock/PLL divider factors

SEL_CLK_x	division by	Description
0	1	
1	2	
2	4	
3	8	
4	16	
5	32	
6	64	with SEL_CLK_RLC = 32
7	64	