

MOSFET – N-Channel, POWERTRENCH®

60 V, 50 A, 13 mΩ

FDD13AN06A0

Features

- $R_{DS(on)} = 11.5 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$
- $Q_{G(tot)} = 22 \text{ nC}$ (Typ.) @ $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- Consumer Appliances
- LED TV
- Synchronous Rectification
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

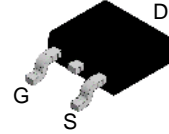
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		A
	Continuous ($T_C < 80^\circ\text{C}$, $V_{GS} = 10 \text{ V}$)	50	
	Continuous ($T_A = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $R_{\theta JA} = 52^\circ\text{C/W}$)	9.9	
	Pulsed	Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	56	mJ
P_D	Power Dissipation	115	W
	Derate above 25°C	0.77	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

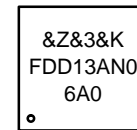
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case, Max. D-PAK	1.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. D-PAK	100	
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. D-PAK, 1 in ² Copper Pad Area	52	$^\circ\text{C/W}$

V_{DSS}	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	13.5 mΩ @ 10 V	50 A

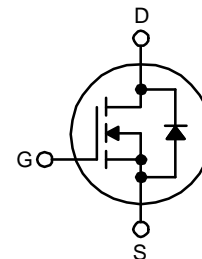


**DPAK3 (TO-252 3 LD)
CASE 369AS**

MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = 3-Digit Date Code
 &K = 2-Digits Lot Run Traceability Code
 FDD13AN06A0 = Device Code



N-Channel

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

FDD13AN06A0

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B _{VDSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	60	–	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 50 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 50 V, V _{GS} = 0 V, T _C = 150°C	–	–	250	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(TH)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2	–	4	V
R _{DS(on)}	Drain to Source On Resistance	I _D = 50 A, V _{GS} = 10 V	–	0.0115	0.0135	Ω
		I _D = 25 A, V _{GS} = 6 V	–	0.022	0.034	
		I _D = 50 A, V _{GS} = 10 V, T _J = 175°C	–	0.026	0.030	

DYNAMIC CHARACTERISTICS

C _{ISS}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	1350	–	pF
C _{OSS}	Output Capacitance		–	260	–	pF
C _{RSS}	Reverse Transfer Capacitance		–	90	–	pF
Q _{g(TOT)}	Total Gate Charge at 10 V	V _{GS} = 0 V to 10 V, V _{DD} = 30 V, I _D = 50 A, I _g = 1.0 mA	–	22	29	nC
Q _{g(TH)}	Threshold Gate Charge	V _{GS} = 0 V to 2 V, V _{DD} = 30 V, I _D = 50 A, I _g = 1.0 mA	–	2.6	3.4	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 30 V, I _D = 50 A, I _g = 1.0 mA	–	8.2	–	nC
Q _{gs2}	Gate Charge Threshold to Plateau		–	5.6	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	6.4	–	nC

SWITCHING CHARACTERISTICS (V_{GS} = 10 V)

t _{ON}	Turn-On Time	V _{DD} = 30 V, I _D = 50 A V _{GS} = 10 V, R _{GS} = 12 Ω	–	–	130	ns
t _{d(ON)}	Turn-On Delay Time		–	9	–	ns
t _r	Rise Time		–	77	–	ns
t _{d(OFF)}	Turn-Off Delay Time		–	26	–	ns
t _f	Fall Time		–	25	–	ns
t _{OFF}	Turn-Off Time		–	–	77	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 50 A	–	–	1.25	V
		I _{SD} = 25 A	–	–	1.0	V
t _{rr}	Reverse Recovery Time	I _{SD} = 50 A, dI _{SD} /dt = 100 A/μs	–	–	24	ns
Q _{RR}	Reverse Recovered Charge	I _{SD} = 50 A, dI _{SD} /dt = 100 A/μs	–	–	15	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Starting T_J = 25°C, L = 45 μH, I_{AS} = 50 A.

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TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

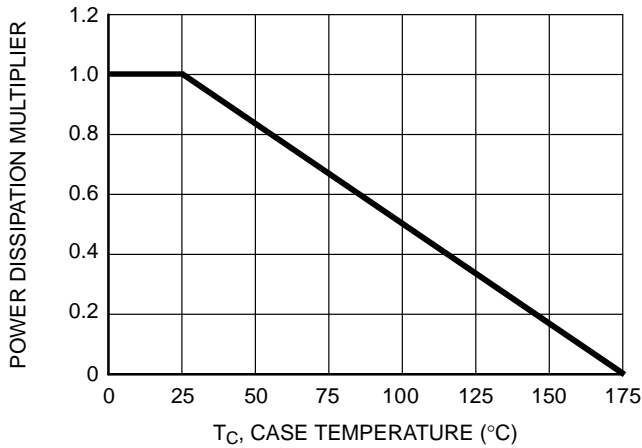


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

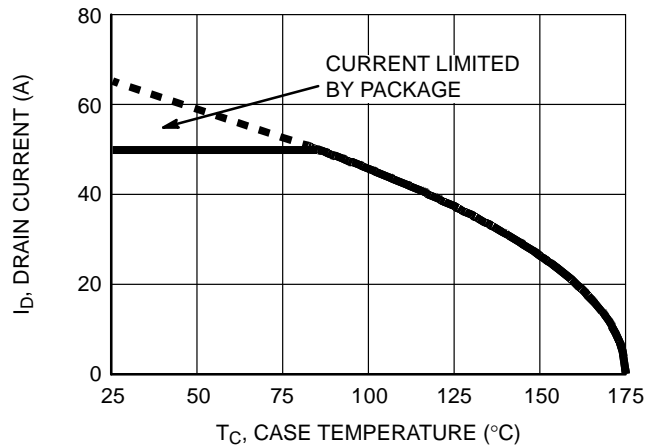


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

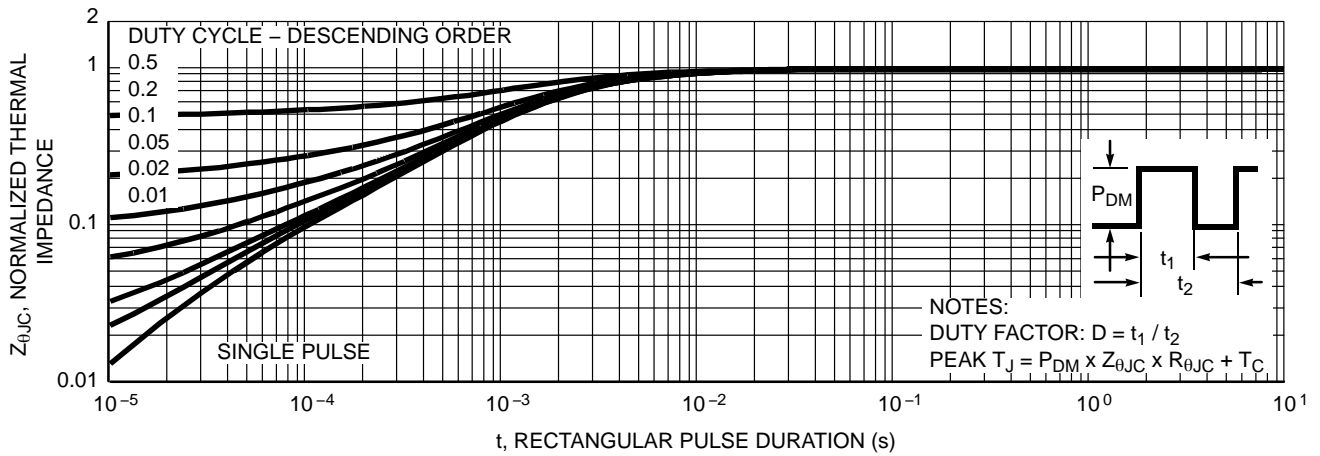


Figure 3. Normalized Maximum Transient Thermal Impedance

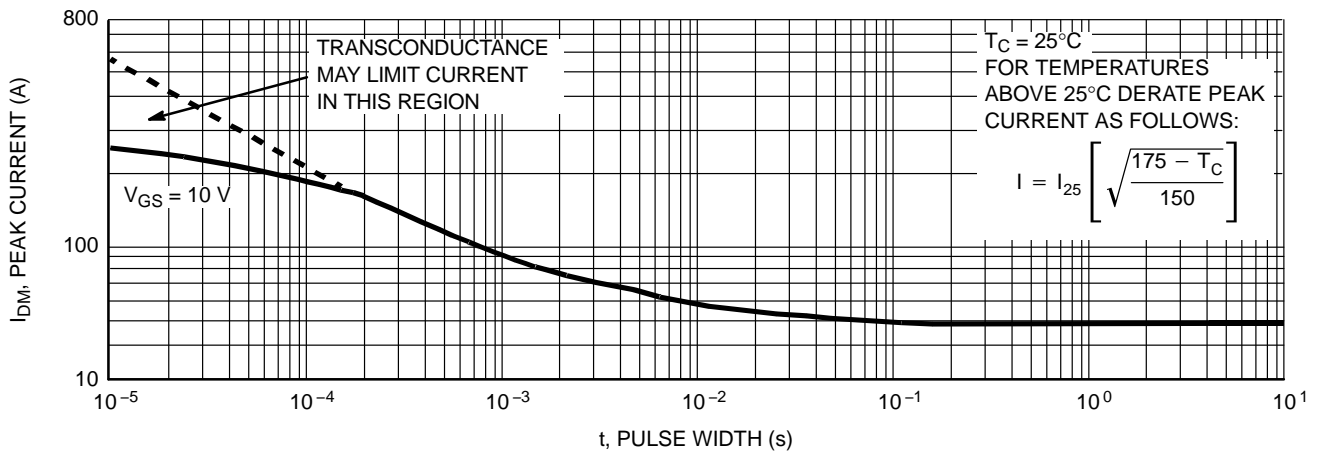


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted) (continued)

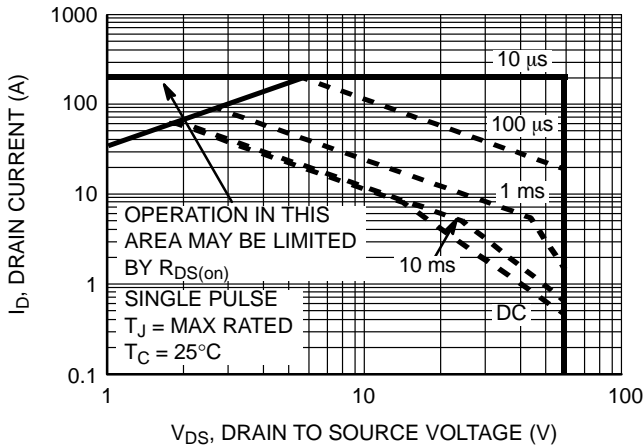
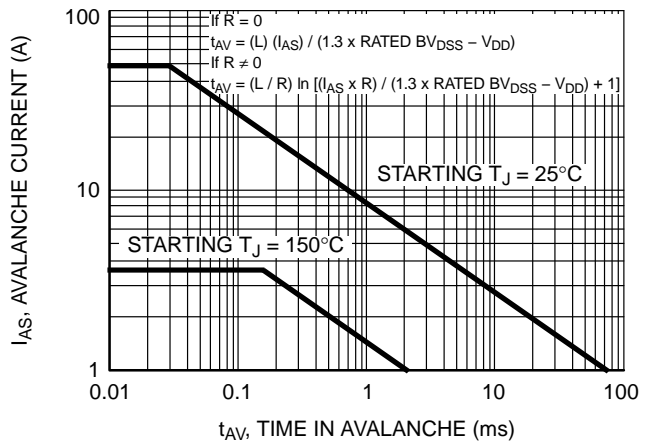


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to onsemi Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

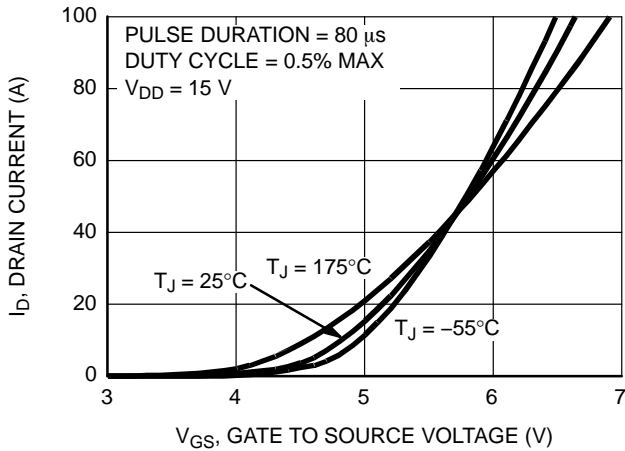


Figure 7. Transfer Characteristics

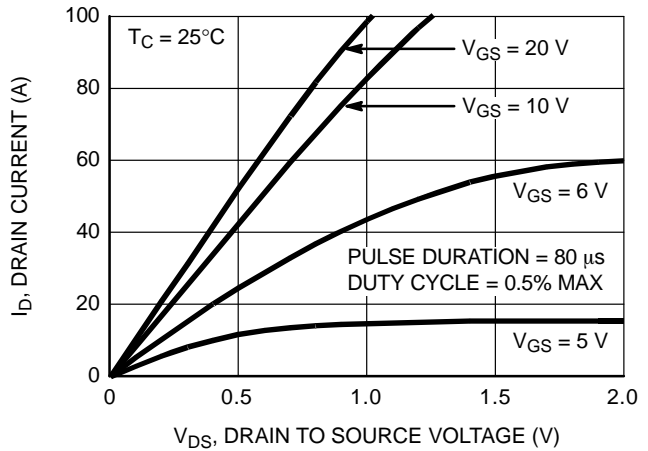


Figure 8. Saturation Characteristics

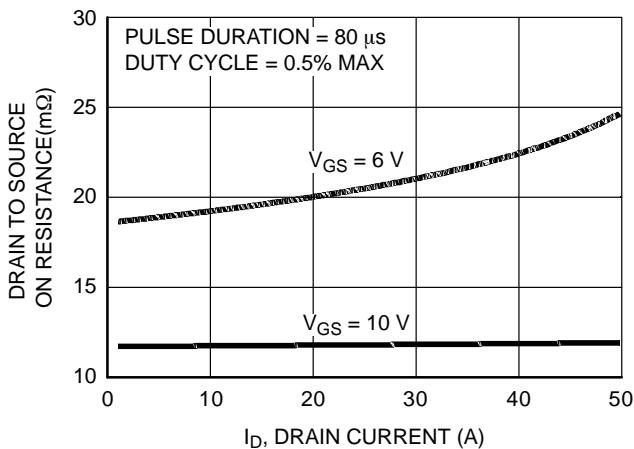


Figure 9. Drain to Source On Resistance vs. Drain Current

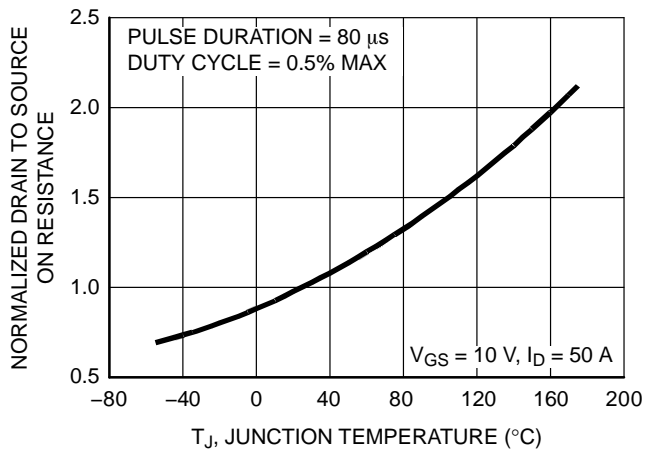


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

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TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted) (continued)

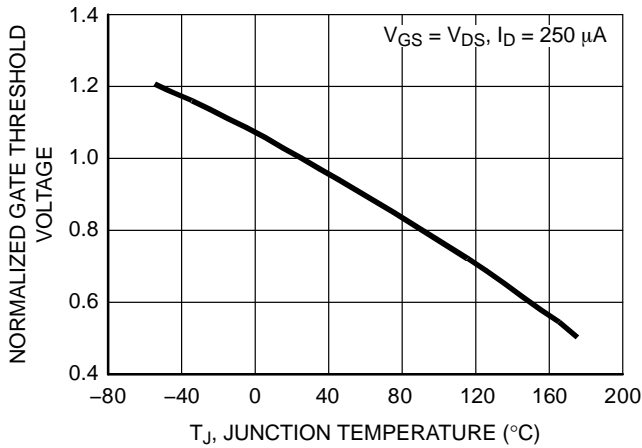


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

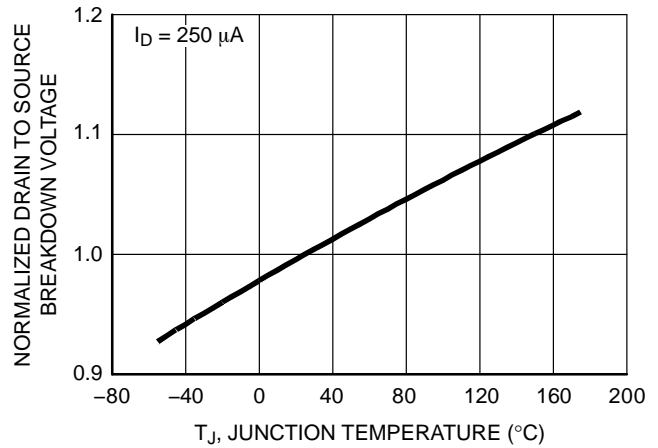


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

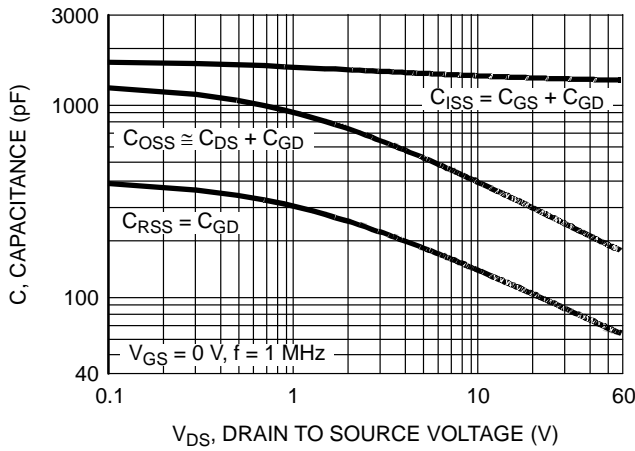


Figure 13. Capacitance vs. Drain to Source Voltage

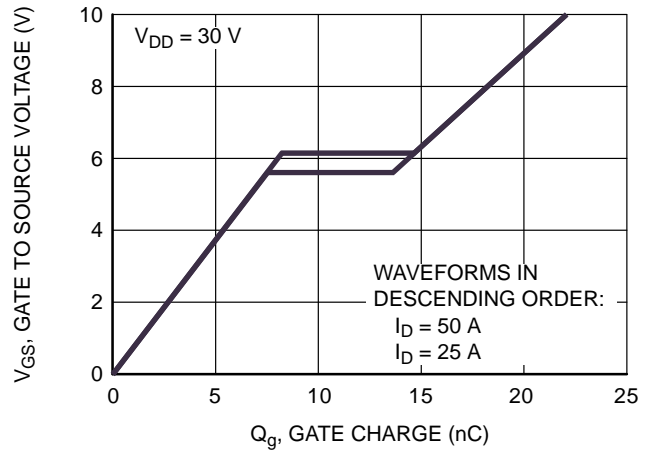


Figure 14. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS AND WAVEFORMS

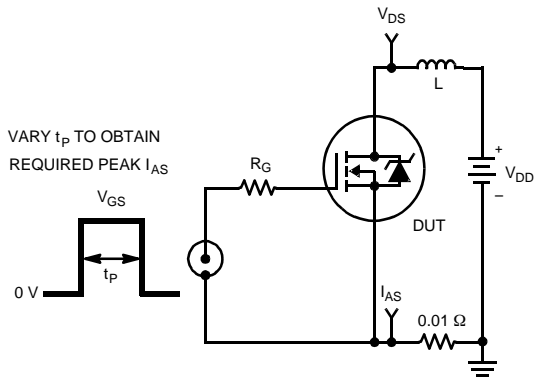


Figure 15. Unclamped Energy Test Circuit

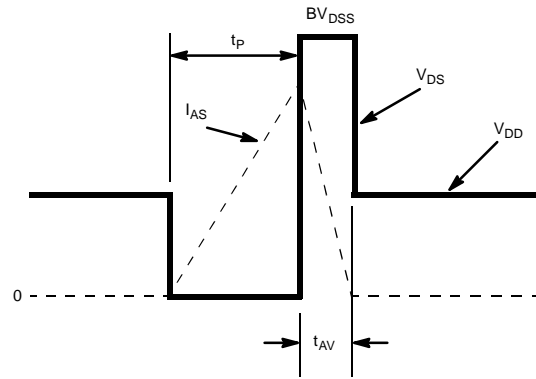


Figure 16. Unclamped Energy Waveforms

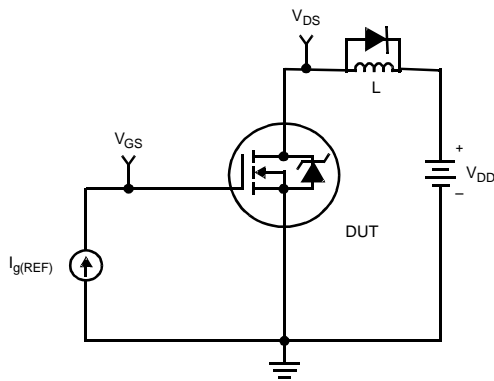


Figure 17. Gate Charge Test Circuit

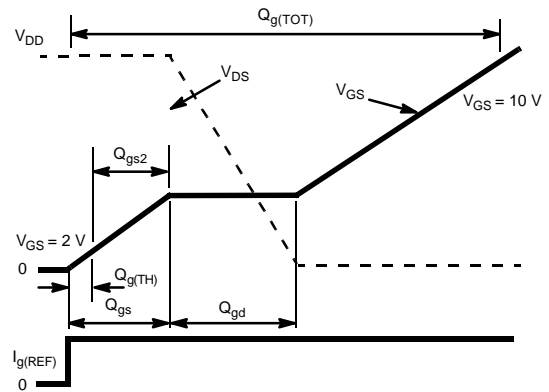


Figure 18. Gate Charge Waveforms

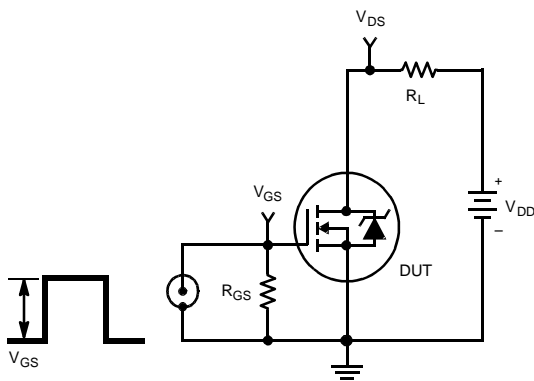


Figure 19. Switching Time Test Circuit

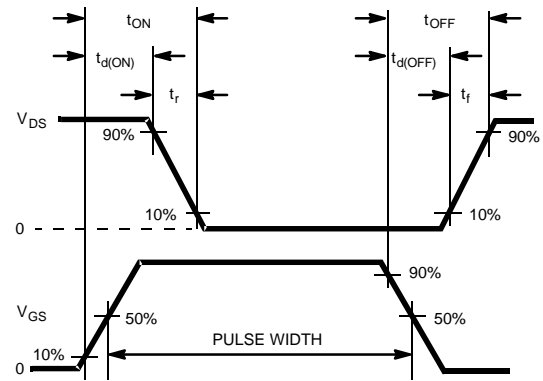


Figure 20. Switching Time Waveforms

THERMAL RESISTANCE VS. MOUNTING PAD AREA

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application’s ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad \text{(eq. 1)}$$

In using surface mount devices such as the TO–252 package, the environment in which it is applied will have a significant influence on the part’s current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

onsemi provides thermal information to assist the designer’s preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR–4 board with 1 oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications

can be evaluated using the **onsemi** device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and Equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + \text{Area})} \quad \text{(eq. 2)}$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + \text{Area})} \quad \text{(eq. 3)}$$

Area in Centimeters Squared

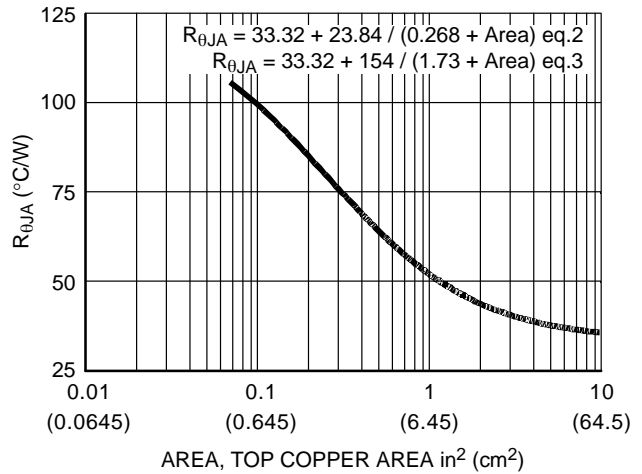


Figure 21. Thermal Resistance vs. Mounting Pad Area

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PSPICE ELECTRICAL MODEL

.SUBCKT FDD13AN06A0 2 1 3 ; rev August 2002

Ca 12 8 5.1e-10
Cb 15 14 5.8e-10
Cin 6 8 1.3e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 65.40
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Etemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.2e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 2.14e-9

RLgate 1 9 52
RLdrain 2 5 10
RLsource 3 7 21.4

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 3.1e-3
Rgate 9 20 3.71
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 5.5e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*160),6))}}

.MODEL DbodyMOD D (IS=1.0E-11 N=1.08 RS=3.5e-3 TRS1=2.2e-3 TRS2=2.5e-9
+ CJO=.9e-9 M=5.1e-1 TT=1e-9 XTI=3.9)

.MODEL DbreakMOD D (RS=1.5e-1 TRS1=1e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=4.1e-10 IS=1e-30 N=10 M=0.45)

.MODEL MmedMOD NMOS (VTO=3.5 KP=6 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.71)

.MODEL MstroMOD NMOS (VTO=4.3 KP=50 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=2.91 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.71e+1 RS=0.1)

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SABER ELECTRICAL MODEL

```
rev August 2002
template FDD13AN06A0 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=1.0e-11,nl=1.08,rs=3.5e-3,trs1=2.2e-3,trs2=2.5e-9,cjo=.9e-9,m=5.1e-1,tt=1e-9,xti=3.9)
dp..model dbreakmod = (rs=1.5e-1,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=4.1e-10,isl=10e-30,nl=10,m=0.45)
m..model mmedmod = (type=_n,vto=3.5,kp=6,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=4.3,kp=50,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=2.91,kp=0.05,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-5,voff=-2)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2,voff=-5)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1.5,voff=.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=.5,voff=-1.5)
c.ca n12 n8 = 5.1e-10
c.cb n15 n14 = 5.8e-10
c.cin n6 n8 = 1.3e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 65.40
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.2e-9
l.l drain n2 n5 = 1.0e-9
l.l source n3 n7 = 2.14e-9

res.rlgate n1 n9 = 52
res.rl drain n2 n5 = 10
res.rl source n3 n7 = 21.4

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=9e-4,tc2=-5e-7
res.r drain n50 n16 = 3.1e-3, tc1=1.3e-2,tc2=5.2e-5
res.r gate n9 n20 = 3.71
res.rslc1 n5 n51 = 1e-6, tc1=1.8e-3,tc2=1.7e-5
res.rslc2 n5 n50 = 1e3
res.r source n8 n7 = 5.5e-3, tc1=1e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-5.3e-3,tc2=-1.0e-5
res.rvtemp n18 n19 = 1, tc1=-2.5e-3,tc2=1e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
```

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sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/160))*6))

}}

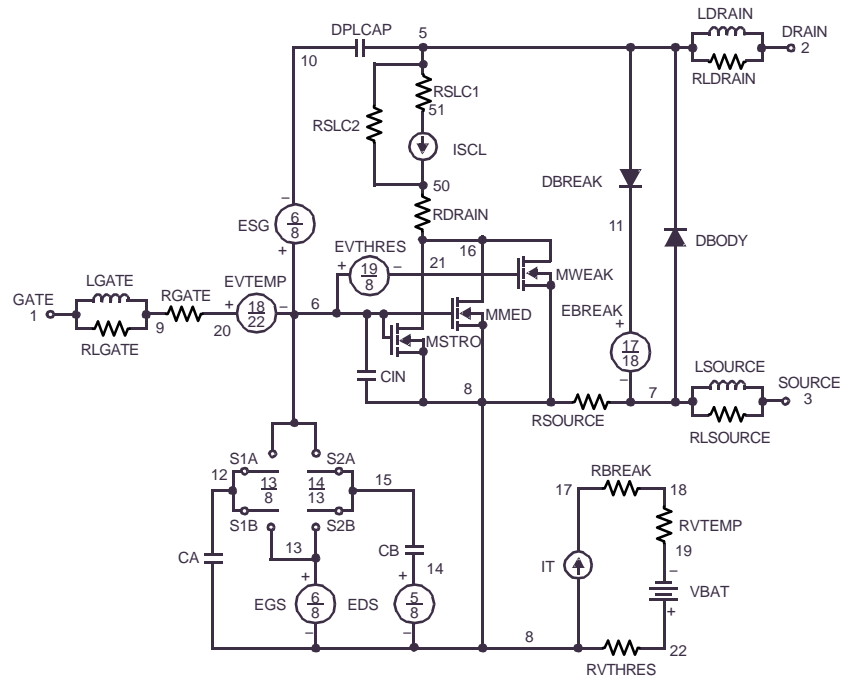


Figure 23.

FDD13AN06A0

PSPICE ELECTRICAL MODEL

REV 22 August 2002

FDD13AN06A0T

CTHERM1 TH 6 9.7e-4
 CTHERM2 6 5 6.2e-3
 CTHERM3 5 4 4.6e-3
 CTHERM4 4 3 4.9e-3
 CTHERM5 3 2 8e-3
 CTHERM6 2 TL 4.2e-2

RTHERM1 TH 6 5.24e-2
 RTHERM2 6 5 10.08e-2
 RTHERM3 5 4 4.28e-1
 RTHERM4 4 3 1.8e-1
 RTHERM5 3 2 1.9e-1
 RTHERM6 2 TL 2.1e-1

SABER ELECTRICAL MODEL

SABER thermal model FDD13AN06A0T

template thermal_model th tl
 thermal_c th, tl

```
{
ctherm.ctherm1 th 6 =9.7e-4
ctherm.ctherm2 6 5 =6.2e-3
ctherm.ctherm3 5 4 =4.6e-3
ctherm.ctherm4 4 3 =4.9e-3
ctherm.ctherm5 3 2 =8e-3
ctherm.ctherm6 2 tl =4.2e-2
```

```
rtherm.rtherm1 th 6 =5.24e-2
rtherm.rtherm2 6 5 =10.08e-2
rtherm.rtherm3 5 4 =4.28e-1
rtherm.rtherm4 4 3 =1.8e-1
rtherm.rtherm5 3 2 =1.9e-1
rtherm.rtherm6 2 tl =2.1e-1
}
```

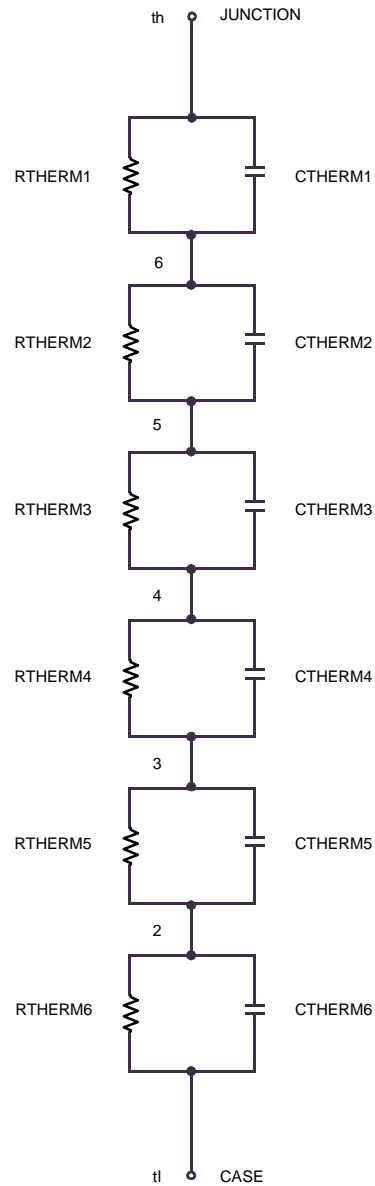


Figure 24.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDD13AN06A0	FDD13AN06A0	DPAK3 (TO-252 3 LD) (Pb-Free, Halide Free)	330 mm	16 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

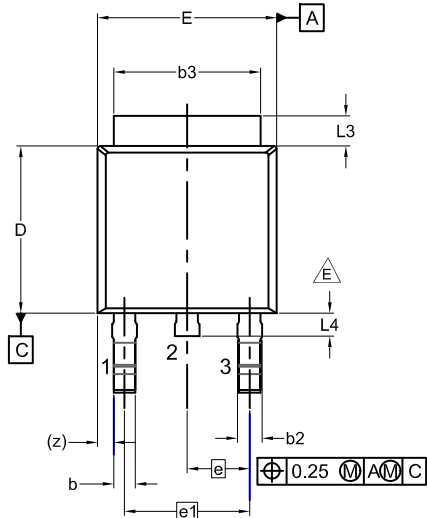
POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

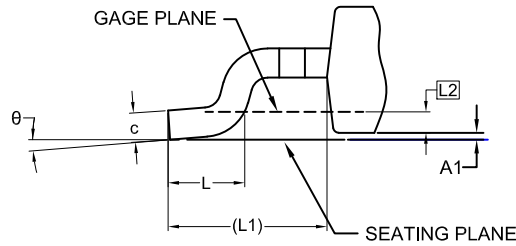


DPAK3 (TO-252 3 LD) CASE 369AS ISSUE A

DATE 28 SEP 2022

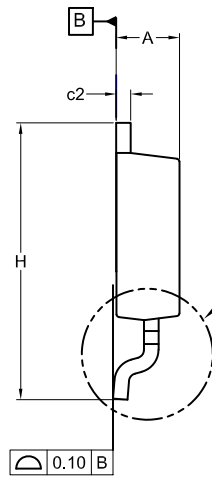
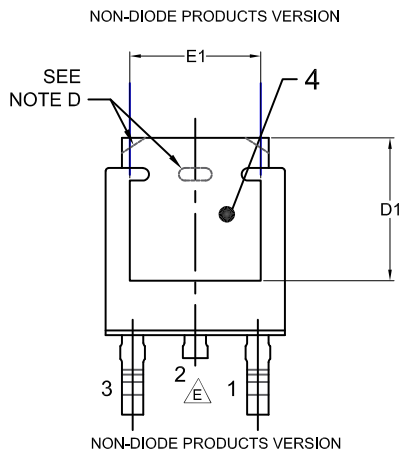


- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	-	-
E	6.35	6.54	6.73
E1	4.32	-	-
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	-	-	1.02
θ	0°	--	10°

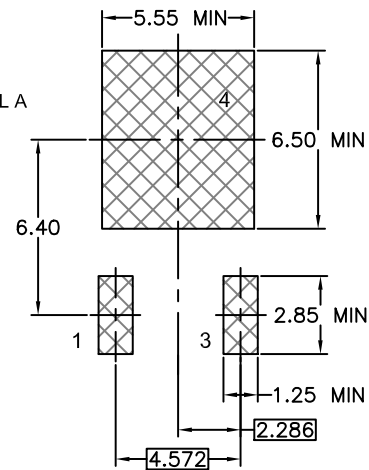


GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	DPAK3 (TO-252 3 LD)	PAGE 1 OF 1

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