

THCX222R05

High Performance Re-driver with Linear Equalization

General Description

THCX222R05 is a high performance bi-directional active re-driver for serial links with data rates up to 5Gbps.

THCX222R05 features a continuous time linear equalizer (CTLE) to provide a boost up to +11.6dB at 2.5 GHz. It opens an input eye completely closed due to inter-symbol interference (ISI) induced by the inter-connect mediums.

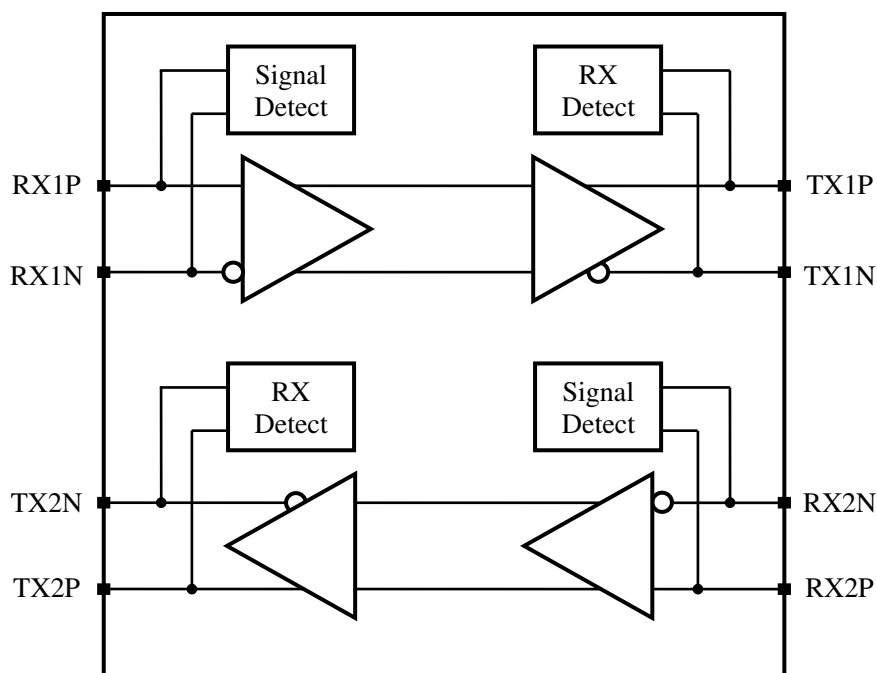
Features

- Signal Conditioning with Linear Equalizer
- Linear Equalization up to +11.6dB@2.5GHz
- Adjustable Voltage Output Swing Linear Range
- Adjustable Receiver Equalization and DC Gain
- Support USB 3.1 Gen1
 - Receiver and LFPS Detect
- Single Supply Voltage (3.3V)
- Package : QFN30 (2.5mm x 4.5mm)

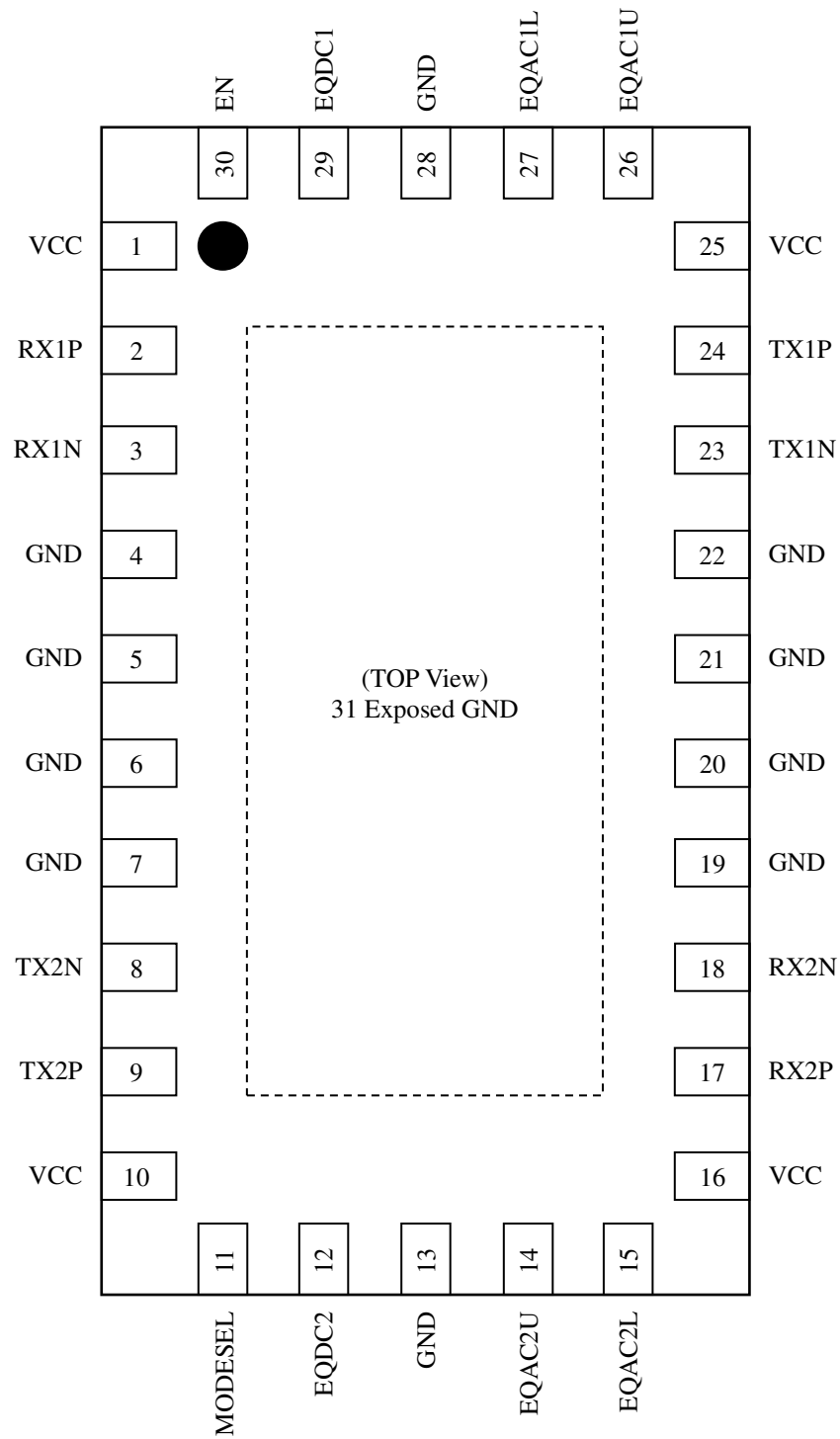
Applications

- USB 3.1 Gen1
- USB Host and Devices
- Docking Stations
- Active Cable
- CML Interface

Block Diagram



Pin Configuration





Pin Description

| Pin Name | Pin No | Type | Description |
|----------|--------------------------------------|------|---|
| RX1P | 2 | CI | Super-Speed CML Signal Input of Channel1(CH1) |
| RX1N | 3 | CI | Super-Speed CML Signal Input of CH1 |
| TX1P | 24 | CO | Super-Speed CML Signal Output of CH1 |
| TX1N | 23 | CO | Super-Speed CML Signal Output of CH1 |
| RX2P | 17 | CI | Super-Speed CML Signal Input of Channel2(CH2) |
| RX2N | 18 | CI | Super-Speed CML Signal Input of CH2 |
| TX2P | 9 | CO | Super-Speed CML Signal Output of CH2 |
| TX2N | 8 | CO | Super-Speed CML Signal Output of CH2 |
| EN | 30 | I | Channel Enable 0 : Power Down 1 : Normal Operation |
| EQAC1U | 26 | 4LI | CH1 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC1L allows for up to 16 settings. |
| EQAC1L | 27 | 4LI | CH1 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC1U allows for up to 16 settings. |
| EQAC2U | 14 | 4LI | CH2 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC2L allows for up to 16 settings. |
| EQAC2L | 15 | 4LI | CH2 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC2U allows for up to 16 settings. |
| EQDC1 | 29 | 4LI | CH1 Equalizer DC Gain Setting |
| EQDC2 | 12 | 4LI | CH2 Equalizer DC Gain Setting |
| MODESEL | 11 | 4LI | Chip Operation Mode Select, if EN=1 0 : CH1/2 enable, RxDetect/SignalDetect enable R : CH1/2 enable, RxDetect enable, SignalDetect disable F : CH1/2 enable, RxDetect/SignalDetect disable 1 : CH1 enable, CH2 disable, RxDetect/SignalDetect disable |
| VCC | 1, 10, 16, 25 | PWR | Power Supply Pin for On-chip Regulator. |
| GND | 4,5,6,7,13, 19,20,21, 22,28,31 | GND | Ground. Must be tied to the PCB ground plane through an array of vias. Pin#31 is exposed pad ground. |

CI: CML Input Buffer, CO: CML Output Buffer
 I: LVCMOS Input Buffer, 4LI: 4-Level LVCMOS Input Buffer,
 PWR: Power Supply, GND: Ground

Operation Mode Settings

Table 1. Operation Mode Setting

| Pin Settings | | Operation Mode |
|--------------|---------|---|
| EN | MODESEL | |
| 1 | 0(*1) | CH1/2 Enable, RxDetect Enable, SignalDetect Enable |
| | R(*2) | CH1/2 Enable, RxDetect Enable, SignalDetect Disable |
| | F(*3) | CH1/2 Enable, RxDetect Disable, SignalDetect Disable |
| | 1(*4) | CH1 Enable, CH2 Disable, RxDetect Disable, SignalDetect Disable |
| 0 | Ignore | Chip Power Down. |

*1 Tie 0Ω to GND

*2 Tie 180kΩ to GND

*3 Leave Open

*4 Tie 0Ω to VCC

Detect Function

THCX222R05 has Input Signal Detect (SignalDetect) and Receiver Detect (RxDetect) functionality for USB3.x transmission.

Detect functionality must be disabled when it is not USB3.x application.

Linear Equalizer Settings

Table 2. Equalization and -1dB Compression Point Linear Swing Settings

| EQACnU ⁿ¹ | EQACnL ⁿ¹ | Equalizer Settings (dB) @2.5GHz | Output Linear Swing Settings (mVppd) | |
|----------------------|----------------------|------------------------------------|--------------------------------------|---------|
| | | | @100MHz | @2.5GHz |
| 0 | 0 | 1.5 | 830 | 760 |
| 0 | R | 2.7 | | |
| 0 | F | 3.7 | | |
| 0 | 1 | 4.8 | | |
| R | 0 | 5.6 | | |
| R | R | 6.7 | | |
| R | F | 8.0 | | |
| R | 1 | 8.9 | | |
| F | 0 | 4.3 | | |
| F | R | 5.5 | 1200 | 1000 |
| F | F | 6.5 | | |
| F | 1 | 7.6 | | |
| 1 | 0 | 8.4 | | |
| 1 | R | 9.5 | | |
| 1 | F | 10.8 | | |
| 1 | 1 | 11.6 | | |

*1 n=1,2

Table 3. Flat Gain Settings

| EQDCn ⁿ¹ | Flat Gain Settings (dB)@Up to 200MHz | |
|---------------------|--------------------------------------|---------------------------|
| | EQACn ⁿ¹ U=0/R | EQACn ⁿ¹ U=F/1 |
| 0 | -2.2 | -0.7 |
| R | -1.3 | 0.2 |
| F | 0.1 | 1.8 |
| 1 | 4.1 | 5.6 |

*1 n=1,2

-1dB Compression Point is showed below. It means output voltage range that has linearity.

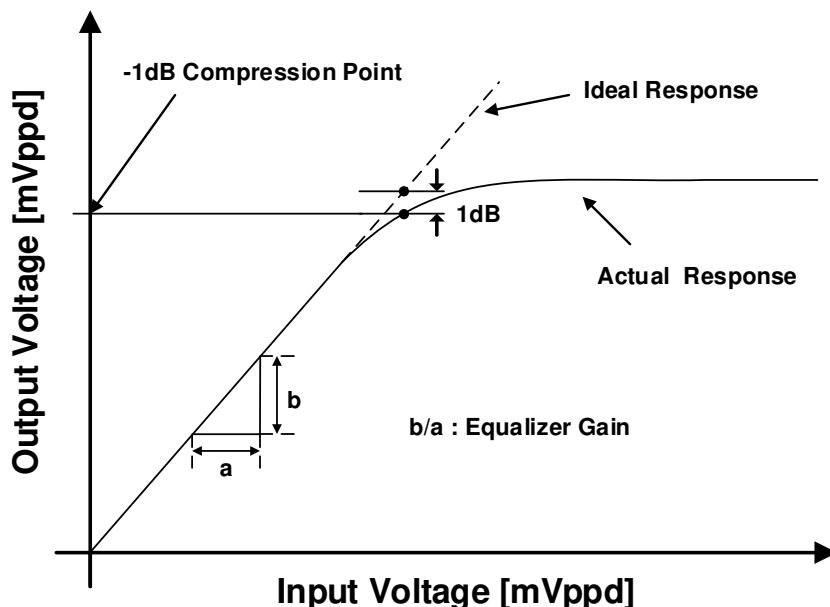


Figure 1. -1dB Compression Point

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

| Parameter | | Min | Typ | Max | Unit | |
|--------------------------------|-----|----------------|-----|---------|--------|----|
| Supply Voltage(VCC) | | -0.3 | - | 4.0 | V | |
| LVCMOS Input/Output Voltage | | -0.3 | - | VCC+0.3 | V | |
| 4-Level LVCMOS Input Voltage | | -0.3 | - | VCC+0.3 | V | |
| CML Receiver Input Voltage | | -0.3 | - | 3.0 | V | |
| CML Transmitter Output Voltage | | -0.3 | - | 3.0 | V | |
| ESD Rating | HBM | High-Speed CML | - | - | ±4 | kV |
| | | All Other Pin | - | - | ±2 | |
| | MM | | - | - | ±200 | V |
| | CDM | | - | - | ±500 | V |
| Storage Temperature | | -55 | - | 125 | °C | |
| Junction Temperature | | - | - | 125 | °C | |
| Reflow Peak Temperature/Time | | - | - | 260/10 | °C/sec | |

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|-------------------------|-----|-----|-----|------|
| Supply Voltage(VCC) | 3.0 | 3.3 | 3.6 | V |
| Supply Ramp Requirement | 0.1 | - | 50 | ms |
| Operating Temperature | -40 | - | 85 | °C |

Equivalent CML Input Schematic Diagram

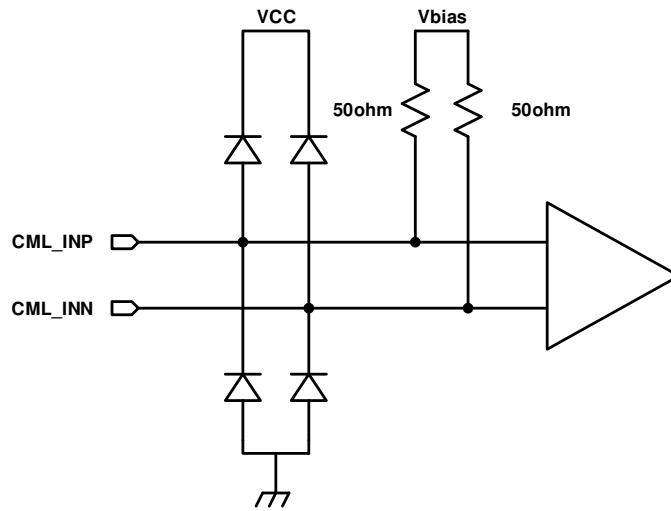


Figure 2. CML Input Schematic Diagram

Equivalent CML Output Schematic Diagram

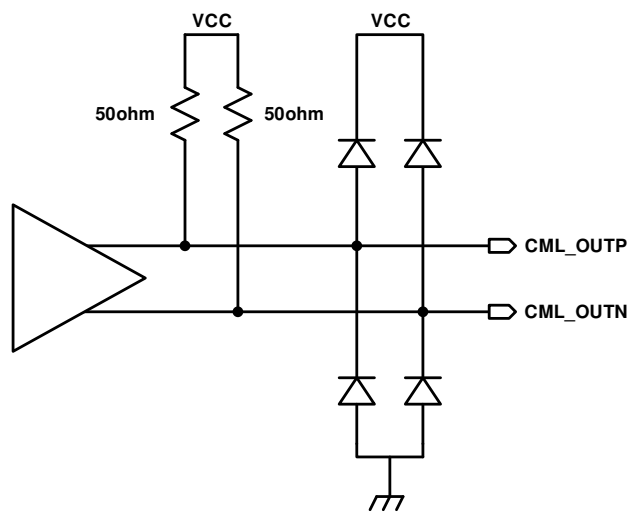


Figure 3. CML Output Schematic Diagram

Equivalent LVC MOS Input Schematic Diagram

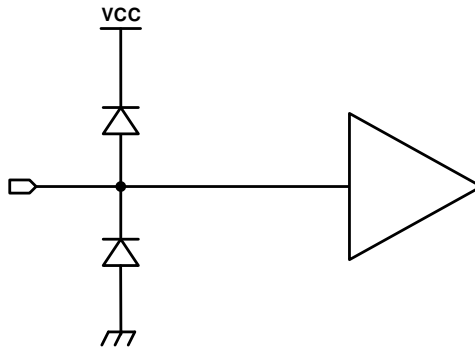


Figure 4. LVC MOS Input Schematic Diagram

Equivalent 4-Level LVC MOS Input Schematic Diagram

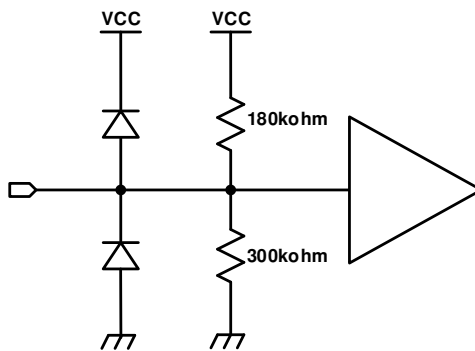


Figure 5. 4-Level LVC MOS Input Schematic Diagram



Electrical Specification

Supply Current

Table 6. Supply Current

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------------------------|--------------------------|-----|-----|-----|------|
| ICCW | Active Mode Supply Current | EQACn ¹ U=F/1 | - | 84 | 150 | mA |
| | | EQACn ¹ U=0/R | - | 69 | - | mA |
| ICCSL | Slumber Mode Supply Current | - | - | 45 | 65 | mA |
| ICCI | Unplug Mode Supply Current | - | - | 1.2 | 2.9 | mA |
| ICCS | Power Down Supply Current | - | - | 120 | 180 | uA |

*1 n=1,2

LVC MOS DC Specification

Table 7. LVC MOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|--------------------------|-----------|-----|-----|-----|------|
| VIH | High Level Input Voltage | - | 2.0 | - | VCC | V |
| VIL | Low Level Input Voltage | - | 0 | - | 0.7 | V |

4-Level LVC MOS DC Specification

Table 8. 4-Level LVC MOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------------------|-------------------------------|-----------|----------------|-----|----------------|------|
| V _{THL} | Low Level Input Voltage | 0(*1) | 0 | - | VCC*0.25 - 0.3 | V |
| V _{THR} | R-Level Input Voltage | R(*2) | VCC*0.25 + 0.3 | - | VCC*0.5 - 0.3 | V |
| V _{THF} | F-Level Input Voltage | F(*3) | VCC*0.5 + 0.3 | - | VCC*0.75 - 0.3 | V |
| V _{THH} | High Level Input Voltage | 1(*4) | VCC*0.75 + 0.3 | - | VCC | V |
| I _{IH_3L} | High level Input Leak Current | VIN=VCC | -100 | - | 100 | uA |
| I _{IL_3L} | Low Level Input Leak Current | VIN=GND | -100 | - | 100 | uA |

*Must be tied for setting each level

*1 : Tie 0Ω to GND

*2 : Tie 180kΩ±5% to GND

*3 : Leave pin open

*4 : Tie 0Ω to VCC

Receiver DC/AC Specification

Table 9. Receiver DC/AC Specification

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---------------------------------|---|-----------------|-----|-----|------|------|
| V _{IN-DIFF-PP} | AC Coupled Differential Input Peak to Peak Signal | 5Gbps PRBS9 | - | - | 1200 | mV |
| R _{RX-DC} | Receiver DC Common Mode Impedance | - | - | 30 | - | Ω |
| R _{RX-DIFF-DC} | DC Differential Impedance | - | 72 | 100 | 120 | Ω |
| R _{RX-HIGH-IMP-DC-POS} | DC Input CM Input Impedance for V>0 | - | 25 | - | - | kΩ |
| R _{LRX-DIFF} | Rx Differential Return Loss | 0.05 to 2.5 GHz | - | -7 | - | dB |
| R _{LRX-CM} | Rx Common Mode Return Loss | 0.05 to 2.5 GHz | - | -6 | - | dB |

Transmitter DC / AC Specifications

Table 10. Transmitter DC / AC specification

Over recommended operating supply and temperature range unless otherwise specified

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---------------------------------|--|------------------|-----|-------|-----|--------|
| T _{TX-DJ-DD} | Deterministic Jitter | Loss=18dB@2.5GHz | - | 0.125 | - | UIpp |
| T _{TX-RJ-DD} | Random Jitter | - | - | 0.5 | - | ps RMS |
| T _{TX-RISE-FALL} | Tx Rise/Fall Time | 20% to 80 % | - | 40 | - | ps |
| T _{RF-MISMATCH} | Tx Rise/Fall Mismatch | - | - | 0.01 | - | UI |
| RL _{TX-DIFF} | Tx Differential Return Loss ^{*1} | 0.05 to 2.5 GHz | - | -10 | - | dB |
| RL _{TX-CM} | Tx Common Mode Return Loss ^{*1} | 0.05 to 2.5 GHz | - | -6 | - | dB |
| R _{TX-DIFF-DC} | DC Differential Impedance | - | 72 | 100 | 120 | Ω |
| V _{TX-RCV-DETECT} | The Amount of Voltage Change Allowed during Receiver Detection | - | - | - | 0.6 | V |
| V _{TX-DC-CM} | Transmitter DC Common-mode Voltage | - | - | 1.9 | - | V |
| V _{TX-CM-AC-PP_ACTIVE} | Transmitter AC Common-mode Voltage Active | - | - | - | 100 | mVpp |
| V _{TX-IDLE-DIFF-AC-pp} | Electrical Idle Differential Peak-Peak Output Voltage | - | 0 | - | 10 | mV |
| V _{TX-IDLE-DIFF-DC} | DC Electrical Idle Differential Output Voltage | - | 0 | - | 10 | mV |
| C _{TX-PARASITIC} | Tx Input Capacitance | - | - | - | 1.1 | pF |
| T _{EN} | Power On to EN High Delay | - | 0 | - | - | ns |
| T _{ACTIVE} | EN High to Active Delay | - | - | - | 200 | us |
| T _{PROPAGATION} | Differential Propagation Delay | - | - | 150 | - | ps |

*1 Confirmed evaluation board.

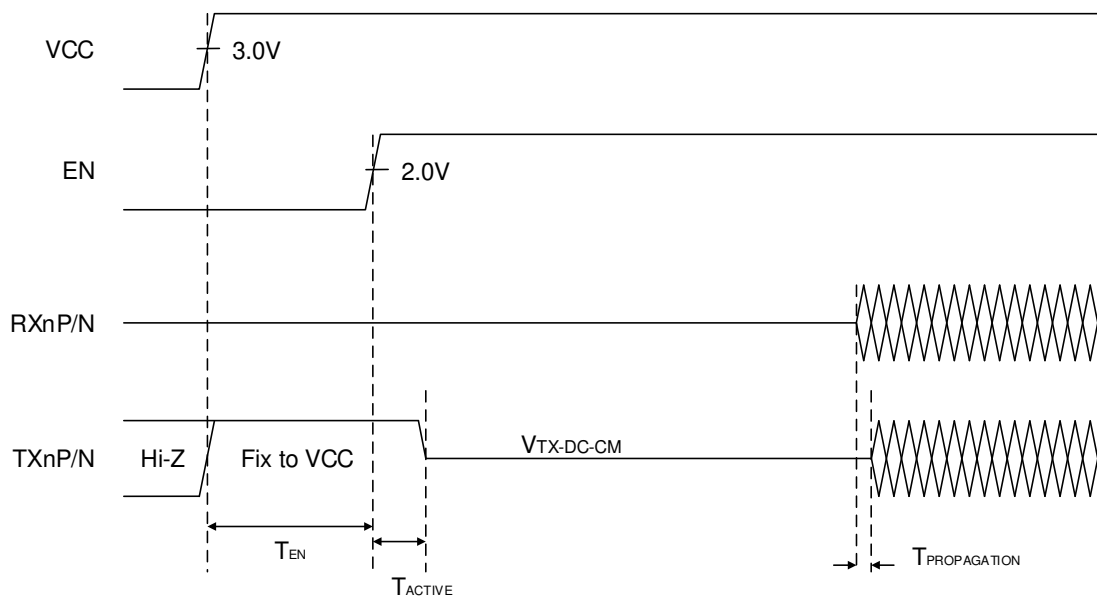
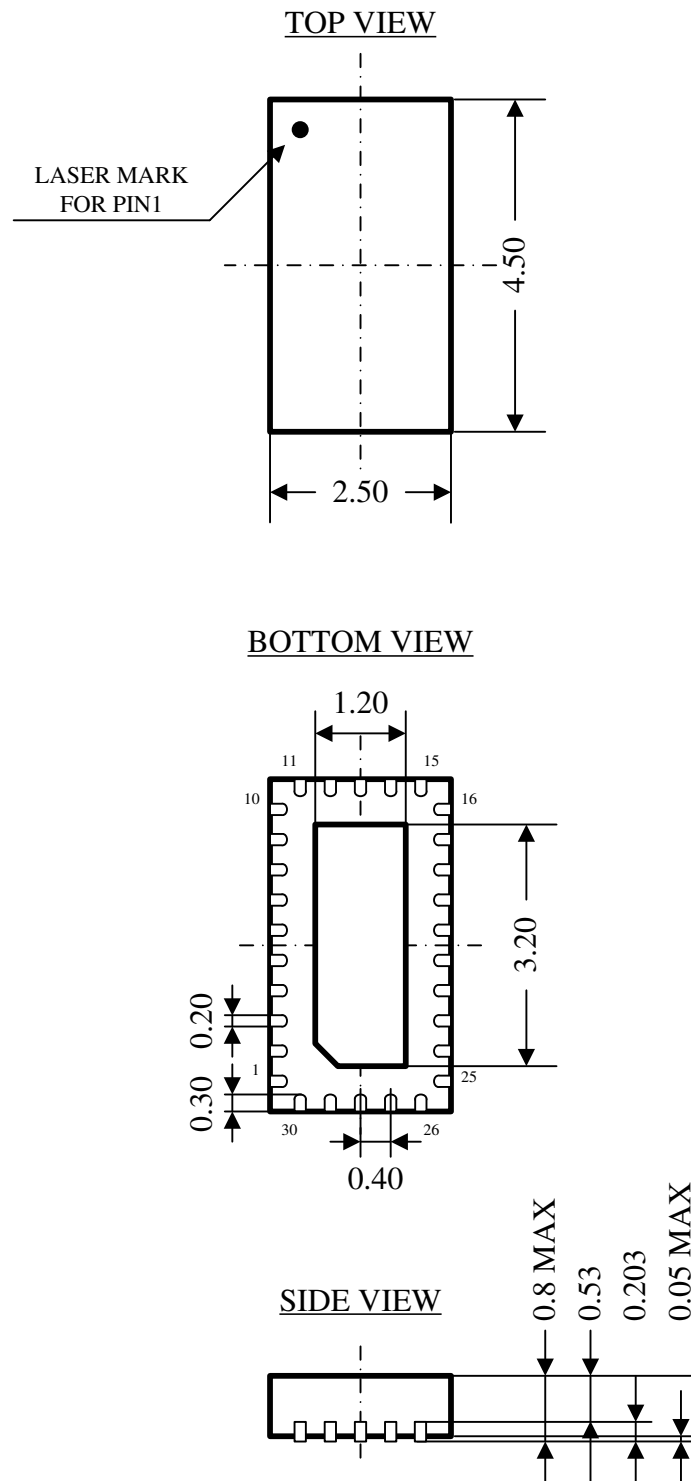


Figure 6. Power on Sequence (SignalDetect Disable/ RxDetect Disable)

n=1,2

Package



Unit: mm

Notices and Requests

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THine Electronics, Inc.

sales@thine.co.jp

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