PCK9447

3.3 V/2.5 V 1 : 9 LVCMOS clock fan-out buffer

Rev. 01 — 13 October 2005 **Product data sheet**

1. General description

The PCK9447 is a 3.3 V or 2.5 V compatible, 1 : 9 clock fan-out buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz, and output skews less than 150 ps, the device meets the needs of most demanding clock applications.

The PCK9447 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with near zero skew. The output buffers support driving of 50 Ω terminated transmission lines on the incident edge: each is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable independent LVCMOS compatible clock inputs are available, providing support of redundant clock source systems. The PCK9447 CLK_STOP control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic LOW state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5 V or 3.3 V power supply and an ambient temperature range of –40 °C to +85 °C. The PCK9447 is pin and function compatible but performance-enhanced to the PCK947.

2. Features

- 9 LVCMOS compatible clock outputs
- 2 selectable, LVCMOS compatible inputs
- Maximum clock frequency of 350 MHz
- Maximum clock skew of 150 ps
- Synchronous output stop in logic LOW state eliminates output runt pulses
- High-impedance output control
- 3.3 V or 2.5 V power supply
- Drives up to 18 series terminated clock lines
- T_{amb} = –40 °C to +85 °C
- Available in LQFP32 package
- Supports clock distribution in networking, telecommunications and computer applications
- Pin and function compatible to PCK947

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PCK9447BD	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

4. Functional diagram

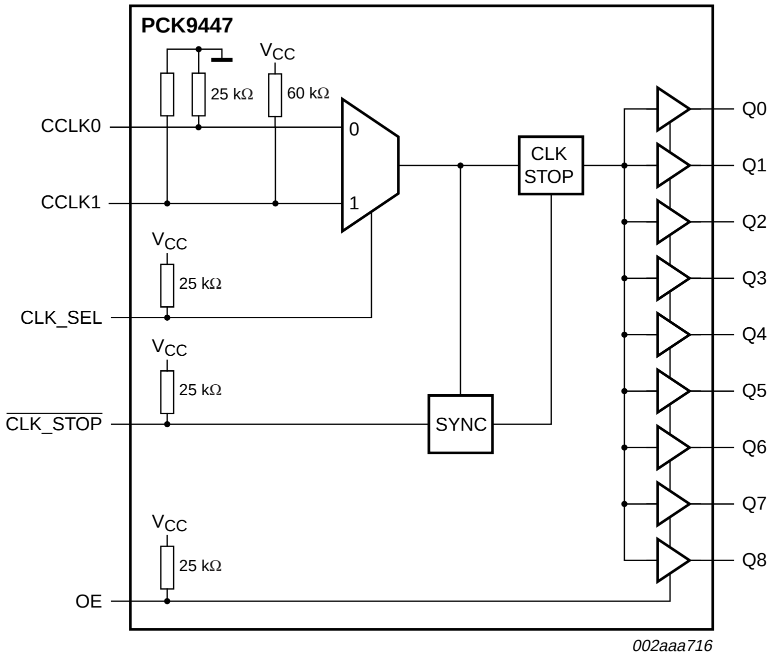


Fig 1. Functional diagram of PCK9447

5. Pinning information

5.1 Pinning

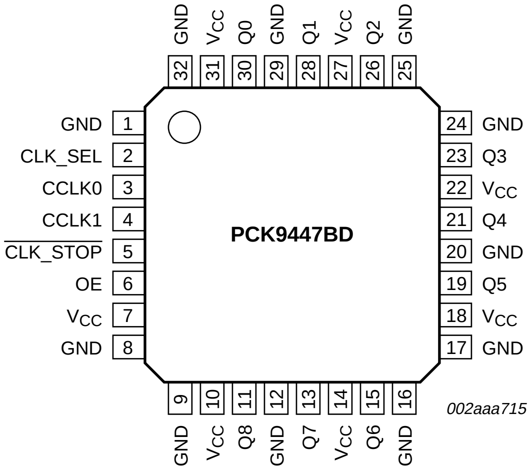


Fig 2. Pin configuration for LQFP32

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
CCLK0	3	I	clock signal input
CCLK1	4	I	alternative clock signal input
CLK_SEL	2	I	clock input select
$\overline{\text{CLK\_STOP}}$	5	I	clock output enable/disable
OE	6	I	output enable/disable (high-impedance, 3-state)
Q0 to Q8	30, 28, 26, 23, 21, 19, 15, 13, 11	O	clock outputs
GND	1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	ground	negative power supply (GND)
V_{CC}	7, 10, 14, 18, 22, 27, 31	power	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.

6. Functional description

6.1 Function table

Table 3: Function table

Control	Default	Logic 0	Logic 1
CLK_SEL	1	CCLK0 input selected	CCLK1 input selected
OE	1	outputs disabled (high-impedance state) [1]	outputs enabled
$\overline{\text{CLK\_STOP}}$	1	outputs synchronously stopped in logic LOW state	outputs active

[1] OE = 0 will high-impedance 3-state all outputs independent of $\overline{\text{CLK\_STOP}}$.

7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+3.9	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
V_O	output voltage		–0.3	V_{CC} + 0.3	V
I_I	input current		-	±20	mA
I_O	output current		-	±50	mA
T_{stg}	storage temperature		–65	+125	°C

8. Characteristics

8.1 General characteristics

Table 5: General characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{TT}	termination voltage (output)			-	$V_{CC}/2$	-	V
V_{esd}	electrostatic discharge voltage	Machine Model	[1]	200	-	-	V
		Human Body Model	[2]	2000	-	-	V
$I_{latch(prot)}$	latch-up protection current			200	-	-	mA
C_{PD}	power dissipation capacitance	per output		-	10	-	pF
C_i	input capacitance	inputs		-	4.0	-	pF

[1] 200 pF capacitor discharged via a 10 Ω resistor and a 0.75 µH inductor

[2] 100 pF capacitor discharged via a 1.5 kΩ resistor

8.2 Static characteristics

Table 6: Static characteristics (3.3 V)
T_{amb} = –40 °C to +85 °C; V_{CC} = 3.3 V ± 5 %

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-state input voltage	LVCMOS		2.0	-	V_{CC} + 0.3	V
V_{IL}	LOW-state input voltage	LVCMOS		–0.3	-	+0.8	V
V_{OH}	HIGH-state output voltage	I_{OH} = –24 mA	[1]	2.4	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 24 mA		-	-	0.55	V
		I_{OL} = 12 mA		-	-	0.30	V
Z_o	output impedance			-	17	-	Ω
I_I	input current	V_I = V_{CC} or GND	[2]	-	-	±300	µA
$I_{q(max)}$	maximum quiescent current	all V_{CC} pins	[3]	-	-	2.0	mA

[1] The PCK9447is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines (V_{CC} = 3.3 V).

[2] Inputs have pull-down or pull-up resistors affecting the input current.

[3] $I_{q(max)}$ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 7: Static characteristics (2.5 V)
T_{amb} = –40 °C to +85 °C; V_{CC} = 2.5 V ± 5 %

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-state input voltage	LVCMOS		1.7	-	V_{CC} + 0.3	V
V_{IL}	LOW-state input voltage	LVCMOS		–0.3	-	+0.7	V
V_{OH}	HIGH-state output voltage	I_{OH} = –15 mA	[1]	1.8	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 15 mA		-	-	0.6	V
Z_o	output impedance			-	19	-	Ω
I_I	input current	V_I = V_{CC} or GND	[2]	-	-	±300	µA
$I_{q(max)}$	maximum quiescent current	all V_{CC} pins	[3]	-	-	2.0	mA

[1] The PCK9447 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives one 50 Ω series terminated transmission line per output (V_{CC} = 2.5 V).

[2] Inputs have pull-down or pull-up resistors affecting the input current.

[3] $I_{q(max)}$ is the DC current consumption of the device with all outputs open and the input in its default state or open.

8.3 Dynamic characteristics

Table 8: Dynamic characteristics (3.3 V)

T_{amb} = −40 °C to +85 °C; V_{CC} = 3.3 V ± 5 % [1] [2]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			0	-	350	MHz
f_o	output frequency			0	-	350	MHz
$t_{W(i)(ref)}$	reference input pulse width			1.4	-	-	ns
t_{PLH}, t_{PHL}	propagation delay	CCLK0 or CCLK1 to any Q		1.3	-	3.3	ns
t_{PLZ}, t_{PHZ}	output disable time			-	-	11	ns
t_{PZL}, t_{PZH}	output enable time			-	-	11	ns
t_{su}	setup time	CCLK0 or CCLK1 to CLK_STOP	[3]	0.0	-	-	ns
t_h	hold time	CCLK0 or CCLK1 to CLK_STOP	[3]	1.0	-	-	ns
$t_{sk(o)}$	output skew time	output-to-output		-	-	150	ps
$t_{sk(pr)}$	process skew time	part-to-part		-	-	2.0	ns
$t_{sk(p)}$	pulse skew time (output)		[4]	-	-	300	ps
δ_o	output duty cycle	f_q < 170 MHz; δ_{ref} = 50 %		45	50	55	%
t_r, t_f	output rise/fall time	0.55 V to 2.4 V		0.1	-	1.0	ns

[1] Dynamic characteristics apply for parallel output termination of 50 Ω to V_{TT}.

[2] Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle, and maximum frequency specifications. CCLK0, CCLK1; 0.7 V to 1.7 V.

[3] Setup and hold times are referenced to the falling edge of the selected clock signal input.

[4] Pulse skew time is the absolute difference of the propagation delay times: | t_{PLH} – t_{PHL} |.

Table 9: Dynamic characteristics (2.5 V)

T_{amb} = −40 °C to +85 °C; V_{CC} = 2.5 V ± 5 % [1] [2]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			0	-	350	MHz
f_o	output frequency			0	-	350	MHz
$t_{W(i)(ref)}$	reference input pulse width			1.4	-	-	ns
t_{PLH}, t_{PHL}	propagation delay	CCLK0 or CCLK1 to any Q		1.7	-	4.4	ns
t_{PLZ}, t_{PHZ}	output disable time			-	-	11	ns
t_{PZL}, t_{PZH}	output enable time			-	-	11	ns
t_{su}	setup time	CCLK0 or CCLK1 to CLK_STOP	[3]	0.0	-	-	ns
t_h	hold time	CCLK0 or CCLK1 to CLK_STOP	[3]	1.0	-	-	ns
$t_{sk(o)}$	output skew time	output-to-output		-	-	150	ps
$t_{sk(pr)}$	process skew time	part-to-part		-	-	2.7	ns
$t_{sk(p)}$	pulse skew time (output)		[4]	-	-	200	ps
δ_o	output duty cycle	f_q < 170 MHz; δ_{ref} = 50 %		45	50	55	%
t_r, t_f	output rise/fall time	0.6 V to 1.8 V		0.1	-	1.0	ns

[1] Dynamic characteristics apply for parallel output termination of 50 Ω to V_{TT}.

[2] Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle, and maximum frequency specifications. CCLK0, CCLK1; 0.7 V to 1.7 V.

[3] Setup and hold times are referenced to the falling edge of the selected clock signal input.

[4] Pulse skew time is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

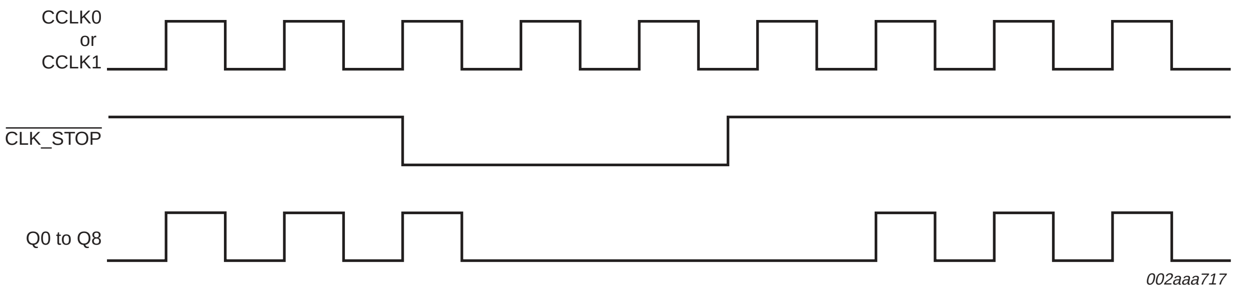
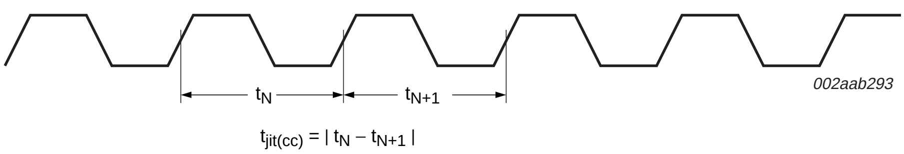


Fig 3. Output clock stop (CLK_STOP) timing diagram



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

Fig 4. Cycle-to-cycle jitter time

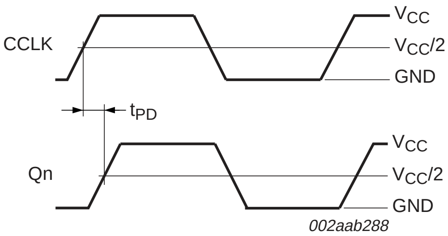


Fig 5. Propagation delay (t_{PD}) test reference

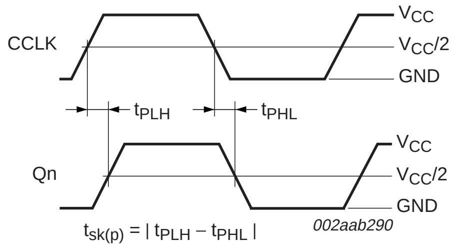
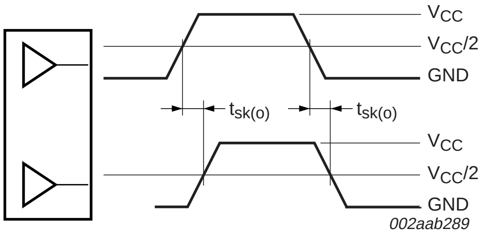
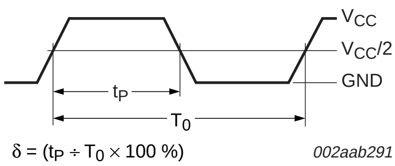


Fig 6. Pulse skew time ($t_{sk(p)}$) test reference



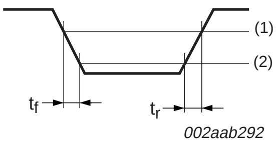
The pin-to-pin skew is defined as the worst-case difference in propagation delay between any similar delay path within a single device.

Fig 7. Output skew time ($t_{sk(o)}$)



The time from the output controlled edge to the non-controlled edge, divided by the time between output controlled edges, expressed as a percentage.

Fig 8. Output Duty Cycle (δ_o)



(1) 2.4 V (V_{CC} = 3.3 V)
1.8 V (V_{CC} = 2.5 V)

(2) 0.55 V (V_{CC} = 3.3 V)
0.6 V (V_{CC} = 2.5 V)

Fig 9. Output transition time test reference

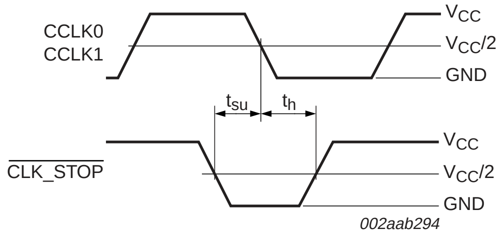


Fig 10. Setup and hold time (t_{su}, t_h)

9. Application information

9.1 Driving transmission lines

The PCK9447 clock driver was designed to drive high-speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 17 Ω (V_{CC} = 3.3 V) or 19 Ω (V_{CC} = 2.5 V), the outputs can drive either parallel or series terminated transmission lines.

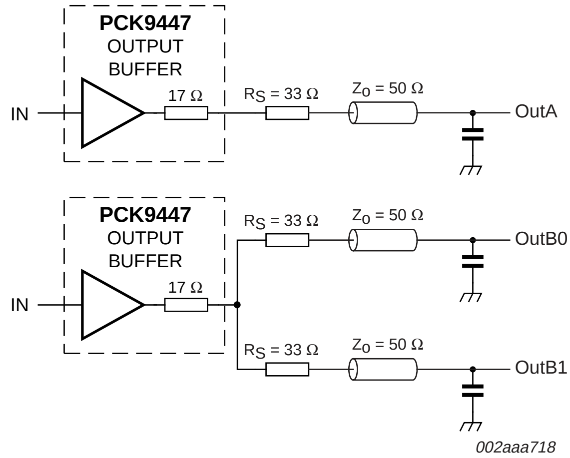


Fig 11. Single versus dual transmission lines

In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current, and thus only a single terminated line can be driven by each output of the PCK9447 clock driver. For the series terminated case, however, there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 11, illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fan-out of the PCK9447 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 12 show simulation results of an output driving a single line versus two lines. In both cases the drive capability of the PCK9447 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurement in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the PCK9447. The output waveform in Figure 12 shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 33 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S\left(\frac{Z_O}{R_S + R_O + Z_0}\right)$$

$$Z_O = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 33\ \Omega \parallel 33\ \Omega$$
$$R_O = 17\ \Omega$$

$$V_L = 3.0\left(\frac{25}{16.5 + 17 + 25}\right) = 1.28\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

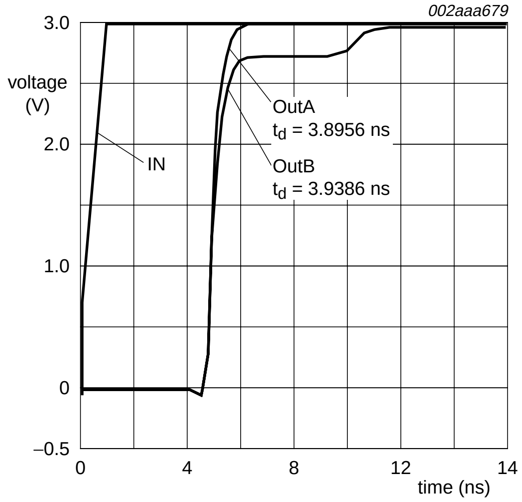
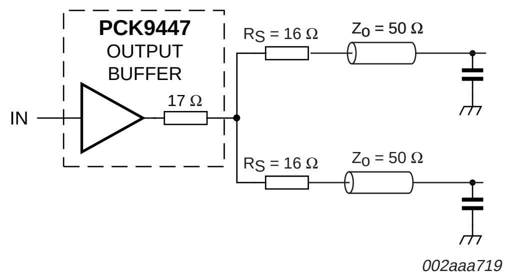


Fig 12. Single versus dual line termination waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 13 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$17\ \Omega + 16\ \Omega \parallel 16\ \Omega = 50\Omega \parallel 50\ \Omega$$

$$25\ \Omega = 25\ \Omega$$

Fig 13. Optimized dual line termination

10. Test information

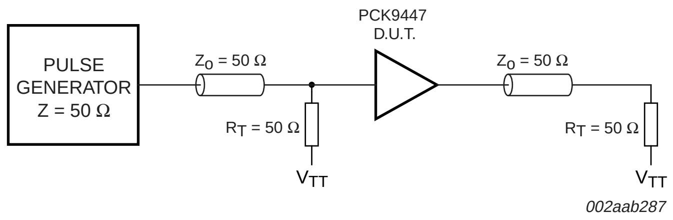
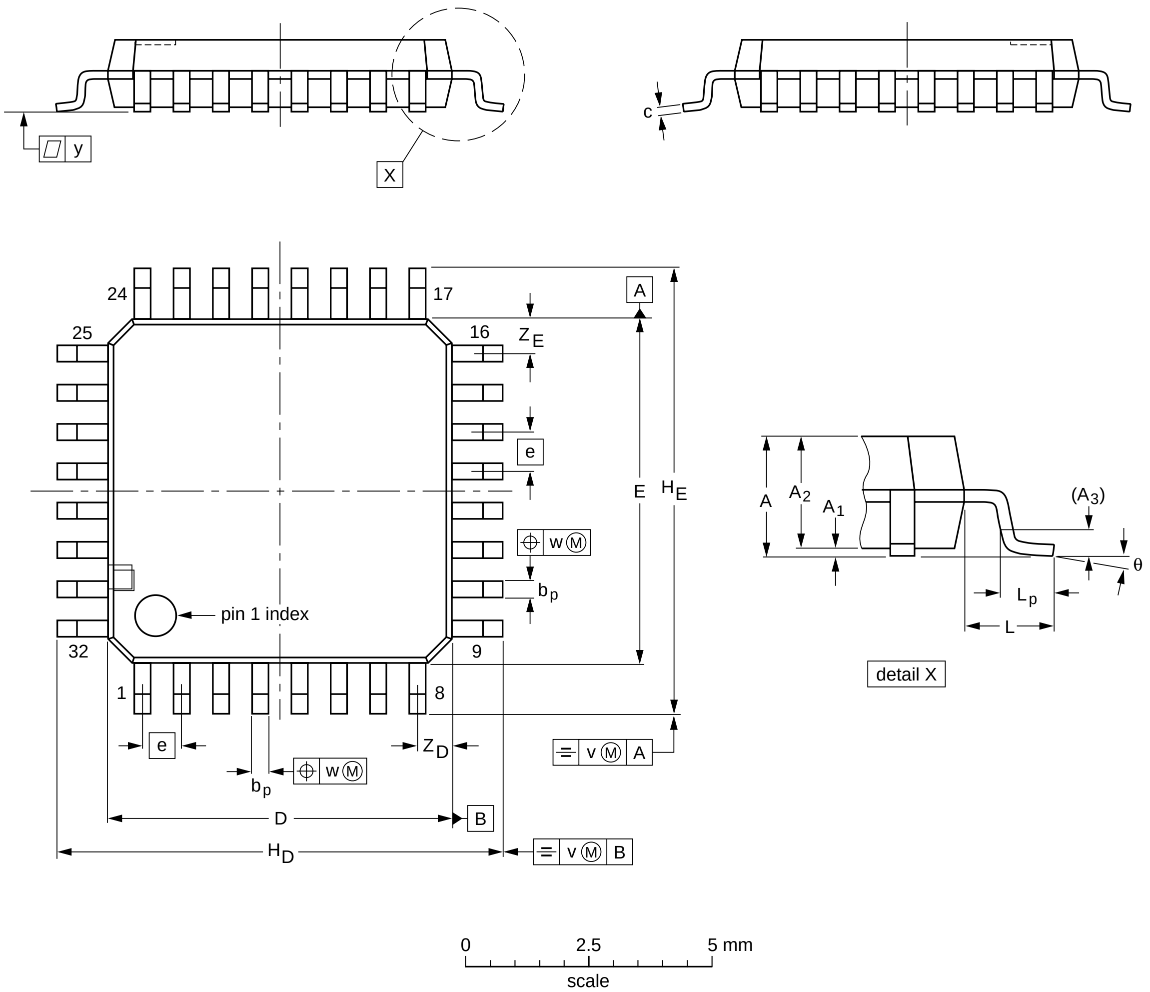


Fig 14. CCLK AC test reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

11. Package outline

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~00-01-19~~ 03-02-25

Fig 15. Package outline SOT358-1 (LQFP32)

12. Soldering

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

  – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

12.5 Package related soldering information

Table 10: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

13. Abbreviations

Table 11: Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
LVCMOS	Low Voltage Complementary Metal Oxide Silicon

14. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCK9447_1	20051013	Product data sheet	-	9397 750 12522	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

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20. Contents

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