Single-Channel, 14-Bit Voltage and Current Output DAC with HART Connectivity

Data Sheet **AD5413**

FEATURES

- 14-bit resolution and monotonicity
- Voltage and current output available on a single terminal
- Current output range: 0 mA to 24 mA, ±0.3% FSR TUE maximum
- Output voltage range, trimmed: ±10.5 V, ±0.3% FSR TUE
- Output voltage range with untrimmed overrange: ±12.6 V (equivalent to 26% overrange at +10 V)
- User-programmable offset and gain
- On-chip reference
- On-chip diagnostics
- −40°C to +105°C temperature range
- 32-lead, 5 mm × 5 mm, LFCSP

APPLICATIONS

- Process control
- Actuator control
- Channel isolated analog outputs
- Programmable logic controller (PLC) and distributed control systems (DCS) applications
- HART network connectivity

GENERAL DESCRIPTION

The AD5413 is a single-channel, 14-bit voltage and current output, digital-to-analog converter (DAC) that operates within a power supply range from a −33 V minimum on the AV_{SS} pin to a +33 V maximum on the AV_{DD1} pin. The C_{HART} pin enables a highway addressable remote transducer (HART®) signal to be ac-coupled on the current output.

The AD5413 uses a versatile, 4-wire serial peripheral interface (SPI) that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, digital signal processor (DSP), and microcontroller interface standards. The SPI interface has an optional SPI cyclic redundancy check (CRC). The AD5413 implements improved diagnostic features from earlier versions of similar DACs.

PRODUCT HIGHLIGHTS

1. 14-bit performance.
2. ±0.3% FSR TUE with internal reference.
3. Voltage or current output on the same pin.
4. Range of diagnostic features.

COMPANION PRODUCTS

Product Family: AD5758, AD5753, AD5423, AD5422
HART Modem: AD5700, AD5700-1
External References: ADR431, ADR3425, ADR4525
Digital Isolators: ADuM141D, ADuM142D
Power: ADP1031, ADP2360, ADM6339

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REVISION HISTORY

6/2020—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

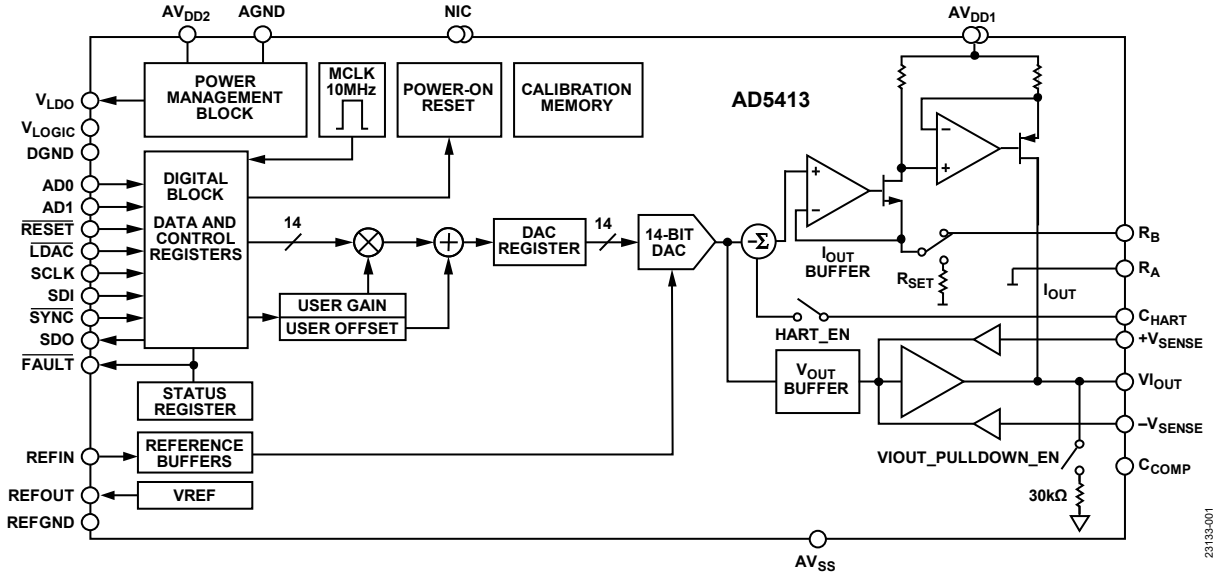


Figure 1.

SPECIFICATIONS

AV_{DD1} = +15 V, AV_{DD2} = +5 V, AV_{SS} = −15 V, V_{LOGIC} = +1.71 V to +5.5 V, AGND = DGND = REFGND = 0 V, REFIN = +2.5 V external, load resistor (R_{LOAD}) = 1 kΩ and load capacitor (C_{LOAD}) = 220 pF for voltage output, and R_{LOAD} = 300 Ω for current output. All specifications at T_A = −40°C to +105°C, junction temperature (T_J) < 125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					Statement of available ranges instead of absolute minimum and maximum values
Output Voltage (V_{OUT}) Range	−10.5		+10.5	V	Trimmed V_{OUT} range
	−12.6		+12.6	V	Untrimmed overrange, equivalent to 26% overrange at 10 V
Resolution	14			Bits	
VOLTAGE OUTPUT ACCURACY					Loaded and unloaded, accuracy specifications refer to all V_{OUT} ranges
Total Unadjusted Error (TUE)	−0.1		+0.1	% full-scale range (FSR)	
	−0.03		+0.03	% FSR	T_A = 25°C
	−0.3		+0.3	% FSR	REFIN = REFOUT (internal reference)
TUE Long-Term Stability[1]		15		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		0.35	1.5	ppm FSR/°C	
Integral Nonlinearity (INL)	−0.012		+0.012	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.05		+0.05	% FSR	
Zero-Scale Error Temperature Coefficient (TC)[2]		±0.3		ppm FSR/°C	
Bipolar Zero Error	−0.05		+0.05	% FSR	
Bipolar Zero Error TC[2]		±0.4		ppm FSR/°C	
Offset Error	−0.05		+0.05	% FSR	
Offset Error TC[2]		±0.3		ppm FSR/°C	
Gain Error	−0.05		+0.05	% FSR	
Gain Error TC[2]		±0.6		ppm FSR/°C	
Full-Scale Error	−0.05		+0.05	% FSR	
Full-Scale Error TC[2]		±0.5		ppm FSR/°C	
VOLTAGE OUTPUT CHARACTERISTICS					
Headroom	2			V	Minimum voltage required between VI_{OUT} supply and AV_{DD1} supply
Footroom	2			V	Minimum voltage required between VI_{OUT} supply and AV_{SS} supply
Short-Circuit Current		16		mA	
Load	1			kΩ	For specified performance
Capacitive Load Stability[2]			10	nF	
			2	µF	External compensation capacitor of 220 pF connected
DC Output Impedance		7		mΩ	
DC Power Supply Rejection Ratio (PSRR)		10		µV/V	
V_{OUT} and $-V_{SENSE}$ Common-Mode Rejection Ratio (CMRR)		10		µV/V	Error in V_{OUT} because of changes in $-V_{SENSE}$
CURRENT OUTPUT (I_{OUT})					
Current Output Ranges	0		24	mA	
Resolution	14			Bits	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT ACCURACY (EXTERNAL CURRENT SETTING RESISTOR (R_{SET}))[3]					Assumes ideal 13.7 kΩ resistor
TUE	−0.1		+0.1	% FSR	
	−0.03		+0.03	% FSR	T_A = 25°C
	−0.3		+0.3	% FSR	REFIN = REFOUT (internal reference)
TUE Long-Term Stability[1]		125		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		2	5	ppm FSR/°C	
INL	−0.012		+0.012	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.05		+0.05	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Offset Error	−0.05		+0.05	% FSR	
Offset Error TC[2]		±0.7		ppm FSR/°C	
Gain Error	−0.05		+0.05	% FSR	
Gain Error TC[2]		±0.3		ppm FSR/°C	
Full-Scale Error	−0.05		+0.05	% FSR	
Full-Scale Error TC[2]		±0.3		ppm FSR/°C	
CURRENT OUTPUT ACCURACY (INTERNAL R_{SET})[3]					
TUE	−0.2		+0.2	% FSR	
	−0.37		+0.37	% FSR	REFIN = REFOUT (internal reference)
TUE Long-Term Stability[1]		380		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		3	6	ppm FSR/°C	Output drift
INL	−0.012		+0.012	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.05		+0.05	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Offset Error	−0.05		+0.05	% FSR	
Offset Error TC[2]		±1		ppm FSR/°C	
Gain Error	−0.2		+0.2	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.2		+0.2	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	
CURRENT OUTPUT CHARACTERISTICS					
Headroom	2.3			V	Minimum voltage required between VI_{OUT} supply and AV_{DD1} supply
Footroom	0			V	Minimum voltage required between VI_{OUT} supply and AV_{SS} supply
Resistive Load[2]			1000	Ω	The current output is characterized with a maximum load of 1 kΩ, do not exceed the headroom compliance
Output Impedance		100		MΩ	Midscale output
DC PSRR		0.1		µA/V	
REFERENCE INPUT/OUTPUT					
Reference Input					
Reference Input Voltage[4]		2.5		V	For specified performance
DC Input Impedance	55	120		MΩ	
Reference Output					
Output Voltage	2.495	2.5	2.505	V	T_A = 25°C (including drift after 1000 hours at T_J = 150°C)
Reference TC[2]	−12		+12	ppm/°C	
Output Noise[2]		7		µV p-p	At 0.1 Hz to 10 Hz
Noise Spectral Density[2]		80		nV/√Hz	At 10 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Capacitive Load[2]			1000	nF	
Load Current		3		mA	
Short-Circuit Current		5		mA	
Line Regulation		1		ppm/V	
Load Regulation		80		ppm/mA	
Thermal Hysteresis[2]		150		ppm	
V_{LDO} PIN OUTPUT					
Output Voltage		3.3		V	
Output Voltage TC[2]		25		ppm/°C	
Output Voltage Accuracy	−2		+2	%	
Externally Available Current			30	mA	
Short-Circuit Current		55		mA	
Load Regulation		0.8		mV/mA	
Capacitive Load		0.1		µF	Recommended operation
DIGITAL INPUTS					
Input Voltage					
$3\ V \le V_{LOGIC} \le 5.5\ V$					
High (V_{IH})	$0.7 \times V_{LOGIC}$			V	
Low (V_{IL})			$0.3 \times V_{LOGIC}$	V	
$1.71\ V \le V_{LOGIC} < 3\ V$					
V_{IH}	$0.8 \times V_{LOGIC}$			V	
V_{IL}			$0.2 \times V_{LOGIC}$	V	
Input Current	−1.5		+1.5	µA	Per pin, internal pull-down on SCLK, SDI, $\overline{\text{RESET}}$, and $\overline{\text{LDAC}}$, internal pull-up on $\overline{\text{SYNC}}$
Pin Capacitance[2]		2.4		pF	Per pin
DIGITAL OUTPUTS					
SDO					
Output Voltage					
Low (V_{OL})			0.4	V	Sinking = 200 µA
High (V_{OH})	$V_{LOGIC} - 0.2$			V	Sourcing = 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance[2]		2.2		pF	
$\overline{\text{FAULT}}$					
Output Voltage					
V_{OL}			0.4	V	10 kΩ pull-up resistor to V_{LOGIC}
		0.6		V	At 2.5 mA
V_{OH}	$V_{LOGIC} - 0.05$			V	10 kΩ pull-up resistor to V_{LOGIC}
POWER REQUIREMENTS					
Supply Voltages					
AV_{DD1}	7		33	V	Maximum operating range of $\lvert AV_{DD1}$ to $AV_{SS}\rvert$ = 50 V
AV_{DD2}	4.5		33	V	Maximum operating range of $\lvert AV_{DD2}$ to $AV_{SS}\rvert$ = 50 V
AV_{SS}	−33		0	V	Maximum operating range of $\lvert AV_{DD1}$ to $AV_{SS}\rvert$ = 50 V
V_{LOGIC}	1.71		5.5	V	
Supply Quiescent Currents[5]					Quiescent current, assuming no load current
AI_{DD1}[6]		1.0		mA	Voltage output mode
		0.8		mA	Current output mode (unipolar)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AI_{DD2}[6]		3.3		mA	Voltage output mode
		2.9		mA	Current output mode
AI_{SS}[6]		−1.1		mA	Voltage output mode
		−0.23		mA	Current output mode (unipolar)
Current Drawn from V_{LOGIC} Supply (I_{LOGIC})			0.01	mA	V_{IH} is the voltage on the V_{LOGIC} pin, V_{IL} = DGND
Power Dissipation					Power dissipation assuming an ideal power supply and excluding the external load power dissipation
		108		mW	AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, R_{LOAD} = 1 kΩ, I_{OUT} = 20 mA
		505		mW	AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, R_{LOAD} = 0 Ω, I_{OUT} = 20 mA
		155		mW	AV_{DD1} = AV_{DD2} = 24 V, AV_{SS} = −15 V, R_{LOAD} = 1 kΩ, I_{OUT} = 20 mA
		550		mW	AV_{DD1} = AV_{DD2} = 24 V, AV_{SS} = −15 V, R_{LOAD} = 0 Ω, I_{OUT} = 20 mA

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[2] Guaranteed by design and characterization. Not production tested.
[3] See the Current Output section for more information on the internal and external R_{SET} resistors.
[4] The AD5413 is factory calibrated with an external 2.5 V reference connected to REFIN.
[5] Production tested to AV_{DD1} = 30 V and AV_{SS} = −20 V.
[6] AI_{DD1}, AI_{DD2}, and AI_{SS} are the currents of the AV_{DD1}, AV_{DD2}, and AV_{SS} supplies, respectively.

AC PERFORMANCE CHARACTERISTICS

AV_{DD1} = +15 V, AV_{DD2} = +5 V, AV_{SS} = −15 V, V_{LOGIC} = +1.71 V to +5.5 V, AGND = DGND = REFGND = 0 V, REFIN = +2.5 V external, R_{LOAD} = 1 kΩ and C_{LOAD} = 220 pF for voltage output, and R_{LOAD} = 300 Ω for current output. All specifications at T_A = −40°C to +105°C, T_J < 125°C, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Voltage Output					
Output Voltage Settling Time		12	20	µs	10 V step to ±0.03% FSR
			15	µs	100 mV step to 1 LSB (14-bit LSB)
Slew Rate		3		V/µs	Digital slew rate control disabled
Power-On Glitch Energy		25		nV-sec	
Digital-to-Analog Glitch Energy		7		nV-sec	
Glitch Impulse Peak Amplitude		25		mV	
Digital Feedthrough		2		nV-sec	
Output Noise		0.2		LSB p-p	14-bit LSB, 0.1 Hz to 10 Hz bandwidth
Output Noise Spectral Density		185		nV/√Hz	Measured at 10 kHz, midscale output
AC PSRR		70		dB	200 mV, 50 Hz, and 60 Hz sine waves superimposed on the power supply voltage
Current Output					
Output Current Settling Time		15		µs	To 0.1% FSR
Output Noise		0.2		LSB p-p	14-bit LSB, 0.1 Hz to 10 Hz bandwidth
Output Noise Spectral Density		0.8		nA/√Hz	Measured at 10 kHz, midscale output
AC PSRR		80		dB	200 mV, 50 Hz, and 60 Hz sine waves superimposed on the power supply voltage

[1] Guaranteed by design and characterization. Not production tested.

TIMING CHARACTERISTICS

AV_{DD1} = +15 V, AV_{DD2} = +5 V, AV_{SS} = −15 V, V_{LOGIC} = +1.71 V to +5.5 V, AGND = DGND = REFGND = 0 V, REFIN = +2.5 V external, R_{LOAD} = 1 kΩ and C_{LOAD} = 220 pF for voltage output, and R_{LOAD} = 300 Ω for current output. All specifications at T_A = −40°C to +105°C, T_J < 125°C, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	1.71 V ≤ V_{LOGIC} < 3 V	3 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	33	20	ns minimum	SCLK cycle time, write operation
	120	66	ns minimum	SCLK cycle time, read operation
t_2	16	10	ns minimum	SCLK high time, write operation
	60	33	ns minimum	SCLK high time, read operation
t_3	16	10	ns minimum	SCLK low time, write operation
	60	33	ns minimum	SCLK low time, read operation
t_4	10	10	ns minimum	$\overline{SYNC}$ falling edge to SCLK falling edge setup time, write operation
	33	33	ns minimum	$\overline{SYNC}$ falling edge to SCLK falling edge setup time, read operation
t_5	10	10	ns minimum	24th or 32nd SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	500	500	ns minimum	$\overline{SYNC}$ high time (applies to all register writes outside of those listed in this table)
	1.5	1.5	µs minimum	$\overline{SYNC}$ high time (DAC_INPUT register write)
	500	500	µs minimum	$\overline{SYNC}$ high time (DAC_CONFIG register write, where the RANGE bits (Bits[3:0]) change, see the Calibration Memory CRC section for more timing information)
t_7	5	5	ns minimum	Data setup time
t_8	6	6	ns minimum	Data hold time
t_9	750	750	ns minimum	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{10}	1.5	1.5	µs minimum	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	250	250	ns minimum	$\overline{LDAC}$ pulse width low
t_{12}	600	600	ns maximum	$\overline{LDAC}$ falling edge to DAC output response time, digital slew rate control disabled
	2	2	µs maximum	$\overline{LDAC}$ falling edge to DAC output response time, digital slew rate control enabled
t_{13}	See the AC Performance Characteristics section	See the AC Performance Characteristics section	µs maximum	DAC output settling time
t_{14}	1.5	1.5	µs maximum	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0)
t_{15}	5	5	µs minimum	$\overline{RESET}$ pulse width low
t_{16}	40	28	ns maximum	SCLK rising edge to SDO valid
t_{17}	100	100	µs minimum	$\overline{RESET}$ rising edge to first SCLK falling edge after $\overline{SYNC}$ falling edge

[1] Guaranteed by design and characterization. Not production tested.
[2] All input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of V_{LOGIC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2 to Figure 5.

Timing Diagrams

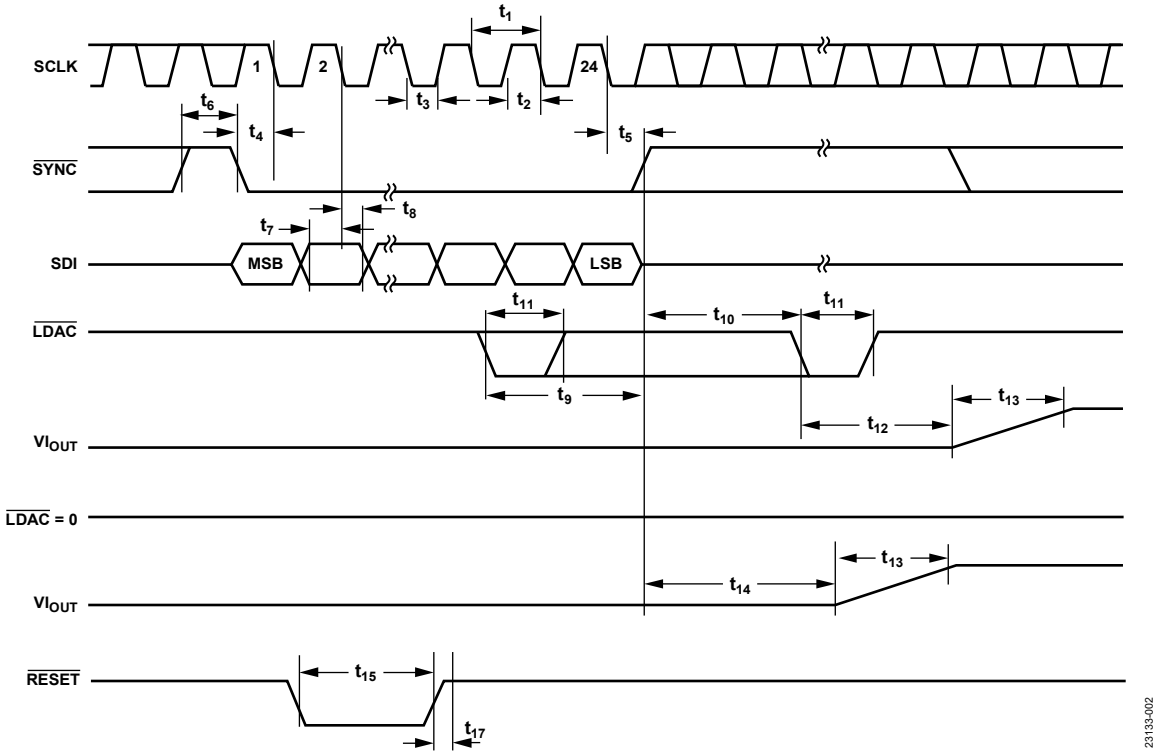


Figure 2. SPI Timing Diagram

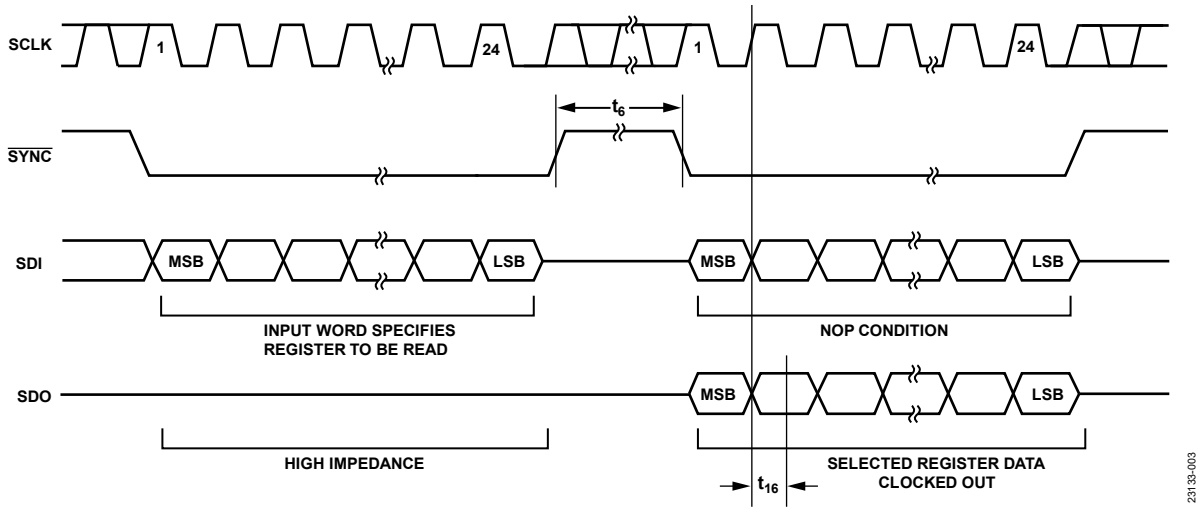
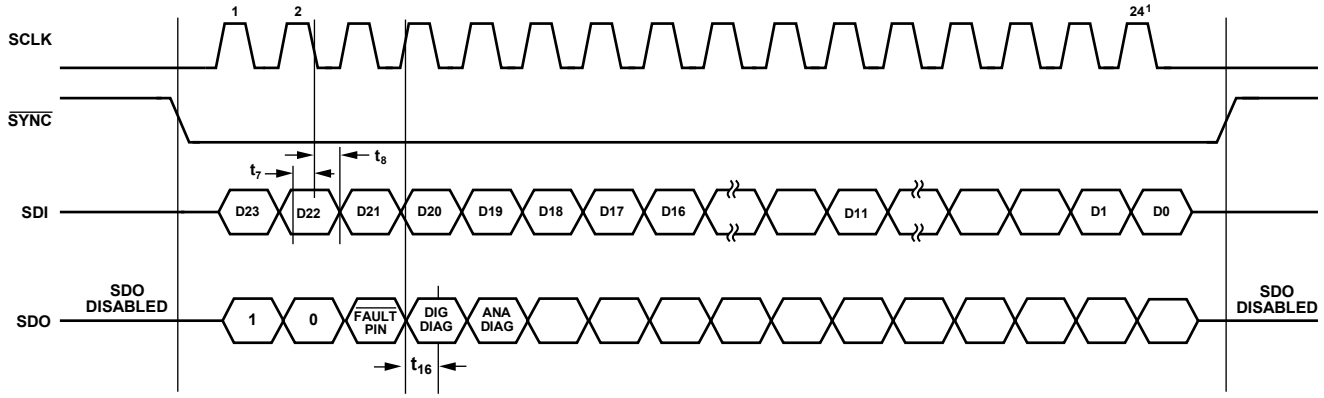


Figure 3. Readback Timing Diagram



[1]IF ANY EXTRA FALLING EDGES ARE RECEIVED AFTER THE 24TH (OR 32ND, IF CRC IS ENABLED) SCLK, BEFORE $\overline{SYNC}$ RETURNS HIGH, SDO CLOCKS OUT 0.

Figure 4. Autostatus Readback Timing Diagram

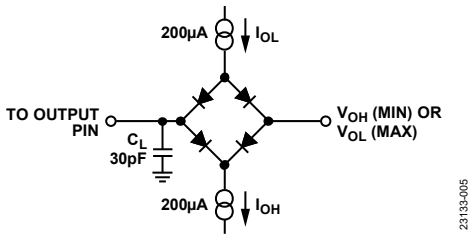


Figure 5. Load Circuit for the SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to ±150 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 4.

Parameter	Rating
AV_{DD1} to AGND, DGND	−0.3 V to +45 V
AV_{SS} to AGND, DGND	−45 V to +0.3 V
AV_{DD1} to AV_{SS}	−0.3 V to +55 V
AV_{DD2} to AGND, DGND	−0.3 V to +45 V
AV_{DD2} to AV_{SS}	−0.3 V to +55 V
V_{LOGIC} to DGND	−0.3 V to +6 V
Digital Inputs[1] to DGND	−0.3 V to V_{LOGIC} + 0.3 V or +6 V (whichever voltage is less)
Digital Outputs[2] to DGND	−0.3 V to V_{LOGIC} + 0.3 V or +6 V (whichever voltage is less)
REFIN, REFOUT, V_{LDO}, C_{HART} to AGND	−0.3 V to AV_{DD2} + 0.3 V or +6 V (whichever voltage is less)
R_A to AGND	−0.3 V to +4.5 V
R_B to AGND	−0.3 V to +4.5 V
VI_{OUT} to AGND	AV_{SS} − 0.3 V or −45 V (whichever voltage is greater) to AV_{DD1} + 0.3 V or +45 V (whichever voltage is less)
$+V_{SENSE}$ to AGND	±40 V
$-V_{SENSE}$ to AGND	±40 V
C_{COMP} to AGND	AV_{SS} − 0.3 V to AV_{DD1} + 0.3 V
AGND, DGND to REFGND	−0.3 V to +0.3 V
Industrial T_A[3]	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
T_J Maximum	125°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] The digital inputs are SCLK, SDI, $\overline{SYNC}$, AD0, AD1, $\overline{RESET}$, and $\overline{LDAC}$.
[2] The digital outputs are $\overline{FAULT}$ and SDO.
[3] Power dissipated on the chip must be derated to keep the junction temperature below 125°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required. θ_{JA} is the junction to ambient thermal resistance, and Ψ_{JT} is the junction to top of package thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JT}	Unit
CP-32-12[1]	41.43	0.29	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings for AD5413

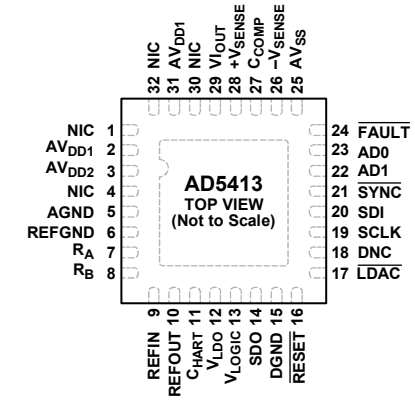
Table 6. AD5413, 32-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±3000	2
FICDM	±750	2B
MM	±200	B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. DNC = DO NOT CONNECT.
3. EXPOSED PAD. EITHER CONNECT THE EXPOSED PAD TO THE POTENTIAL OF THE AV_{SS} PIN, OR LEAVE THE EXPOSED PAD ELECTRICALLY UNCONNECTED. FOR ENHANCED THERMAL PERFORMANCE, THERMALLY CONNECT THE EXPOSED PAD TO A COPPER PLANE.

23133-006

Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 30, 32	NIC	No Internal Connection.
2, 31	AV_{DD1}	Positive Analog Supply. The voltage range on these pins is from 7 V to 33 V.
3	AV_{DD2}	Positive Low Voltage Analog Supply. The voltage range on this pin is from 4.5 V to 33 V.
5	AGND	Ground Reference Point for the Analog Circuitry. Connect this pin to 0 V.
6	REFGND	Ground Reference Point for the Internal Reference. Connect this pin to 0 V.
7	R_A	External Current Setting Resistor. To improve the I_{OUT} temperature drift performance, connect an external precision, low drift, 13.7 kΩ current setting resistor between R_A and R_B.
8	R_B	External Current Setting Resistor. To improve the I_{OUT} temperature drift performance, connect an external precision, low drift, 13.7 kΩ current setting resistor between R_A and R_B.
9	REFIN	External Reference Voltage Input.
10	REFOUT	Internal 2.5 V Reference Voltage Output. Connect REFOUT to REFIN to use the internal reference. A capacitor between REFOUT and REFGND is not recommended.
11	C_{HART}	HART Input Connection. AC-couple the HART signal to C_{HART}. If the HART protocol is not used, leave this pin unconnected. This pin is disconnected from the HART summing node by default and can be connected via the HART_EN bit in the GP_CONFIG1 register.
12	V_{LDO}	3.3 V Low Dropout (LDO) Output Voltage. Decouple V_{LDO} to AGND with a 0.1 µF capacitor.
13	V_{LOGIC}	Digital Supply. The voltage range on V_{LOGIC} is 1.71 V to 5.5 V. Decouple V_{LOGIC} to DGND with a 0.1 µF capacitor.
14	SDO	Serial Data Output. SDO clocks data from the serial register in readback mode. The maximum SCLK speed for readback mode is 15 MHz and depends on V_{LOGIC}.
15	DGND	Digital Ground.
16	$\overline{\text{RESET}}$	Hardware Reset. Active low input.
17	$\overline{\text{LDAC}}$	Load DAC, Active Low Input. $\overline{\text{LDAC}}$ updates the DAC_OUTPUT register and the DAC output. Do not assert $\overline{\text{LDAC}}$ within the 500 ns window before the rising edge of $\overline{\text{SYNC}}$ or 1.5 µs after the rising edge of $\overline{\text{SYNC}}$.
18	DNC	Do Not Connect.
19	SCLK	Serial Clock Input. Data is clocked to the input shift register on the falling edge of SCLK. In write mode, this pin operates at clock speeds of up to 50 MHz that depend on the V_{LOGIC} voltage. In read mode, the maximum SCLK speed is 20 MHz and depends on the V_{LOGIC} voltage.
20	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
21	$\overline{\text{SYNC}}$	Frame Synchronization Signal for the Serial Interface. Active low input. While $\overline{\text{SYNC}}$ is low, data is transferred to the device on the falling edge of SCLK.
22	AD1	Address Decode 1 for the On-Board AD5413.
23	AD0	Address Decode 0 for the On-Board AD5413.

Pin No.	Mnemonic	Description
24	$\overline{\text{FAULT}}$	Fault Pin, Active Low, Pseudo Open-Drain Output. $\overline{\text{FAULT}}$ is high impedance when no faults are detected and is asserted low when certain faults are detected, including an open circuit in current mode, a short circuit in voltage mode, a CRC error, or an overtemperature error. Connect $\overline{\text{FAULT}}$ to V_{LOGIC} with a 10 kΩ pull-up resistor.
25	AV_{SS}	Negative Analog Supply. The voltage range on this pin is from 0 V to −33 V. If 0 V is applied, only current output mode is supported.
26	$-V_{SENSE}$	Sense Connection for Negative Voltage Output Load Connection in V_{OUT} Mode. $-V_{SENSE}$ must stay within ±10 V of AGND for specified operation. Connect a series 1 kΩ resistor to $-V_{SENSE}$. If remote sensing is not used, short $-V_{SENSE}$ to AGND via a series 1 kΩ resistor.
27	C_{COMP}	Optional Compensation Capacitor Connection for the V_{OUT} Buffer. Connect a 220 pF capacitor between C_{COMP} and VI_{OUT} to allow the voltage output to drive up to 2 µF. The addition of this capacitor reduces the bandwidth of the output amplifier and increases the settling time.
28	$+V_{SENSE}$	Sense Connection for the Positive Voltage Output Load Connection in V_{OUT} Mode. If remote sensing is not used, short $+V_{SENSE}$ to VI_{OUT} via a series 1 kΩ resistor.
29	VI_{OUT}	Voltage or Current Output Pin. VI_{OUT} is a shared pin that provides either a buffered output voltage or output current.
	EPAD	Exposed Pad. Either connect the exposed pad to the potential of the AV_{SS} pin, or leave the exposed pad electrically unconnected. For enhanced thermal performance, thermally connect the exposed pad to a copper plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUT

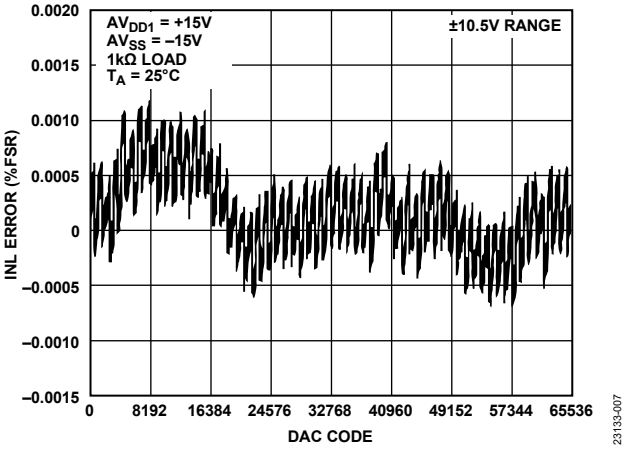


Figure 7. INL Error vs. DAC Code

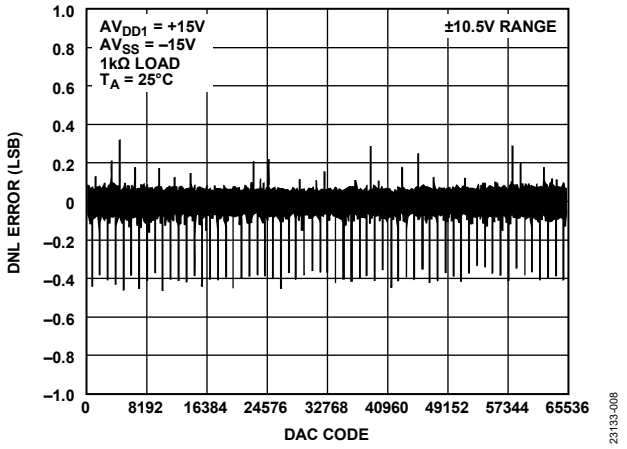


Figure 8. DNL Error vs. DAC Code

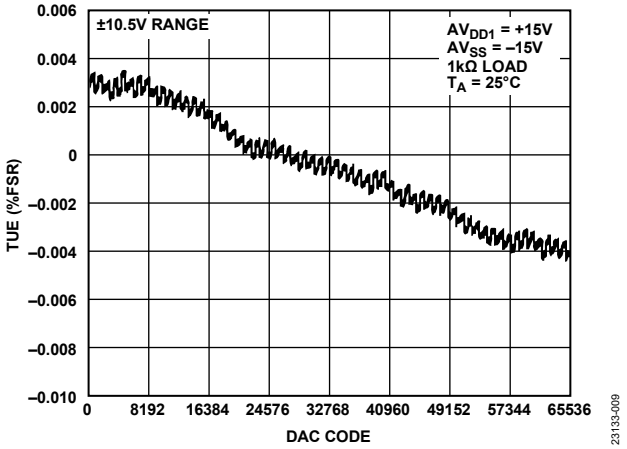


Figure 9. TUE vs. DAC Code

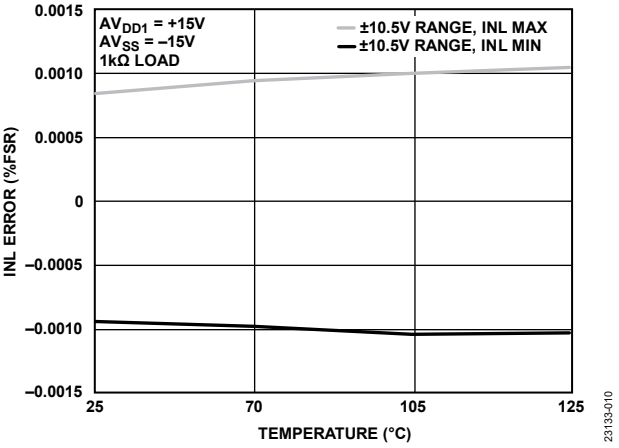


Figure 10. INL Error vs. Temperature

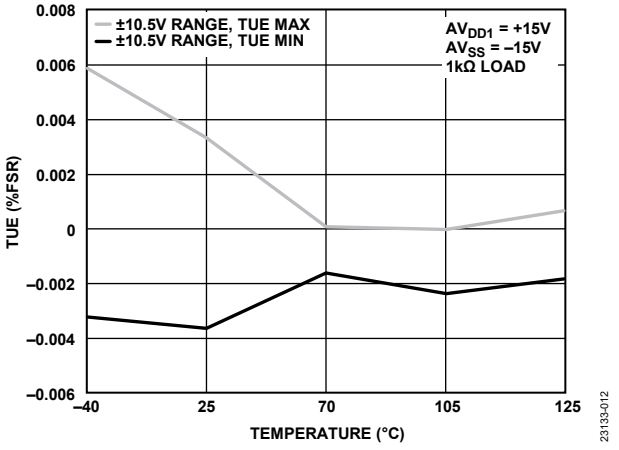


Figure 11. TUE vs. Temperature

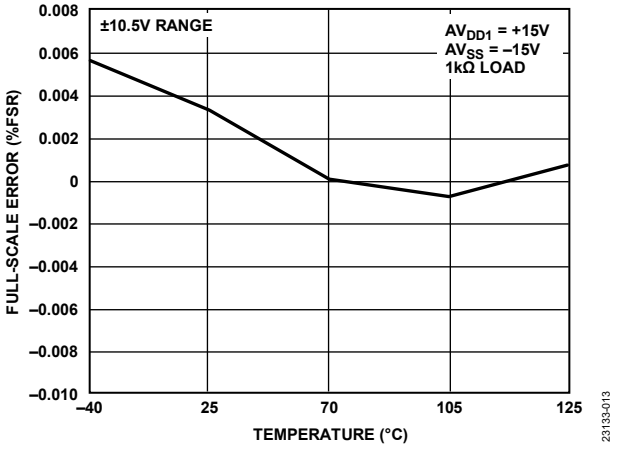


Figure 12. Full-Scale Error vs. Temperature

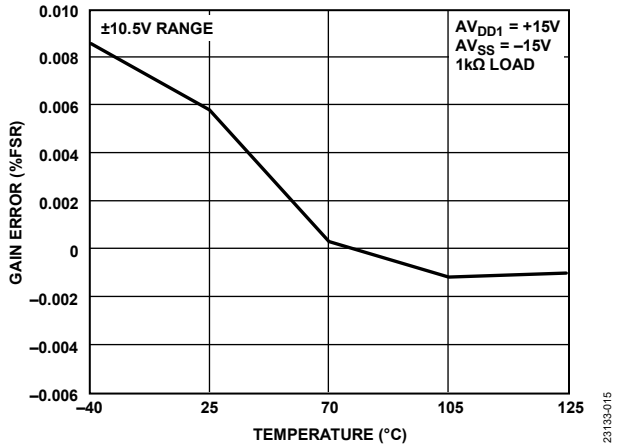


Figure 13. Gain Error vs. Temperature

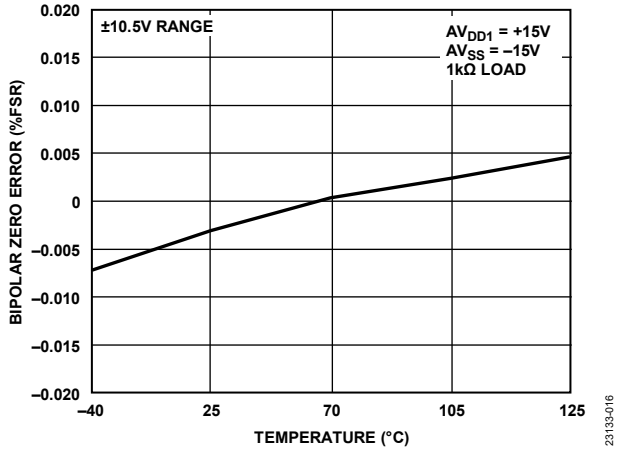


Figure 14. Bipolar Zero Error vs. Temperature

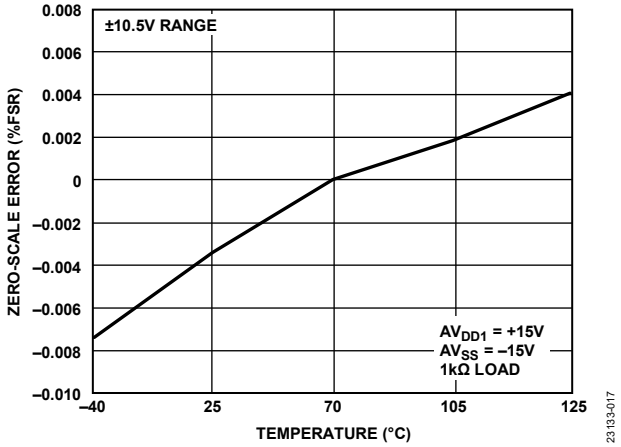


Figure 15. Zero-Scale Error vs. Temperature

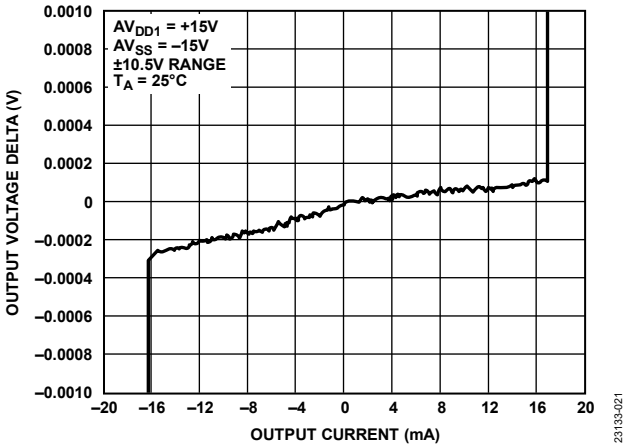


Figure 16. Sink and Source Capability of the Output Amplifier

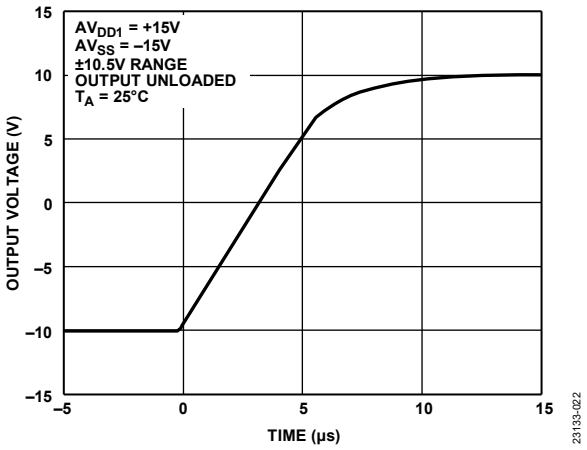


Figure 17. Full-Scale Positive Step

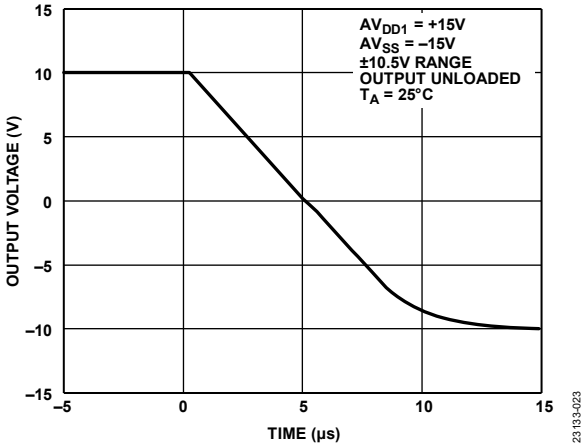


Figure 18. Full-Scale Negative Step

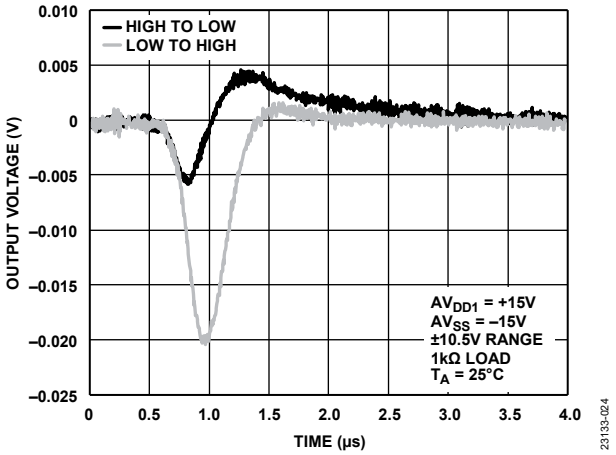


Figure 19. Digital-to-Analog Glitch Major Code Transition

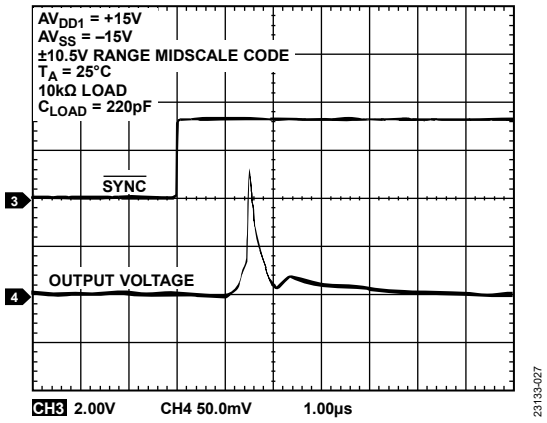


Figure 22. $\overline{SYNC}$ and Output Voltage vs. Time on Output Enable

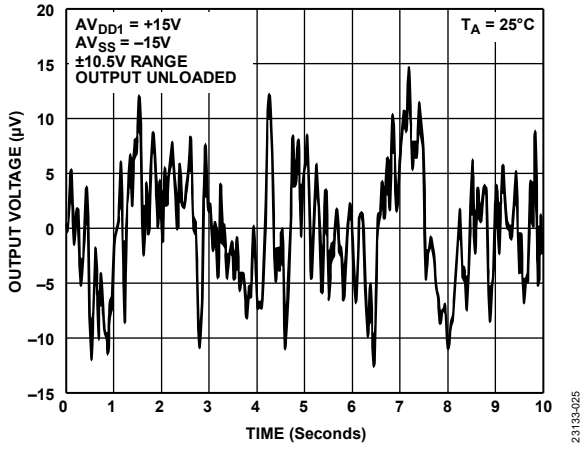


Figure 20. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

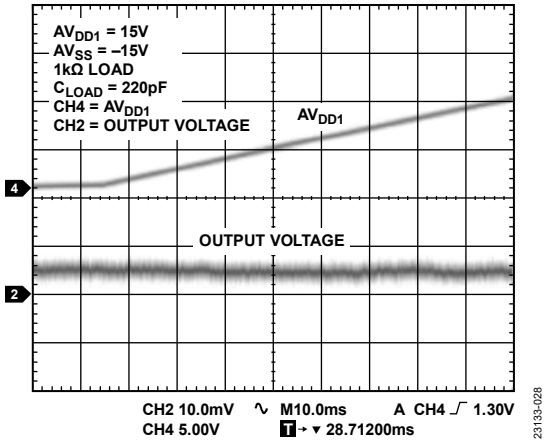


Figure 23. Output Voltage vs. Time on Power-Up

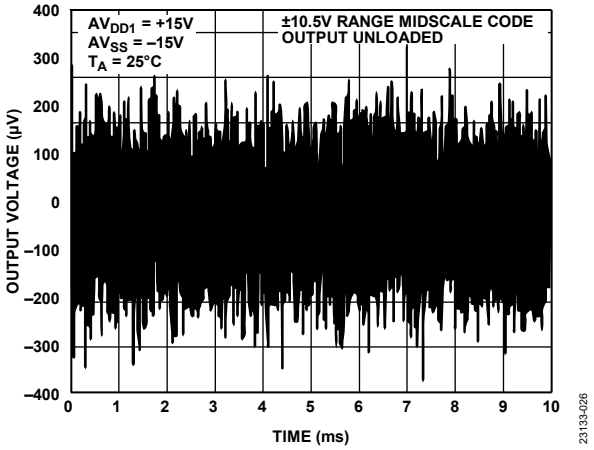


Figure 21. Peak-to-Peak Noise (100 kHz Bandwidth)

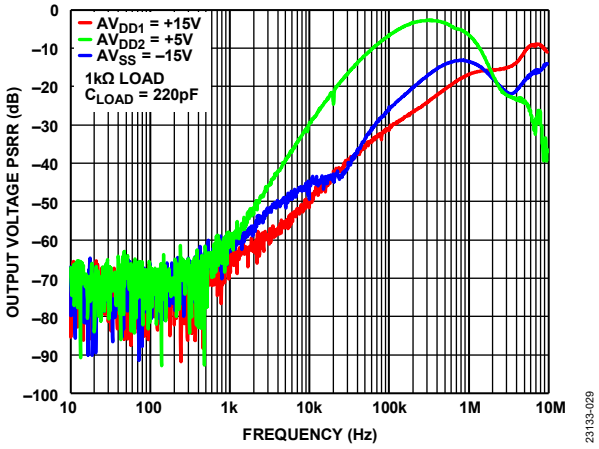


Figure 24. Output Voltage PSRR vs. Frequency

CURRENT OUTPUT

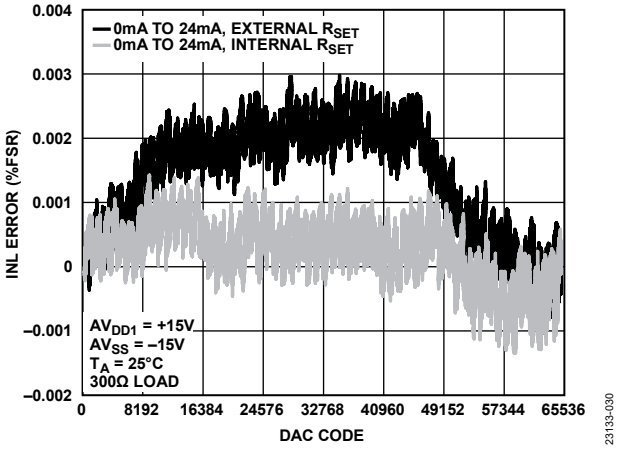


Figure 25. INL Error vs. DAC Code

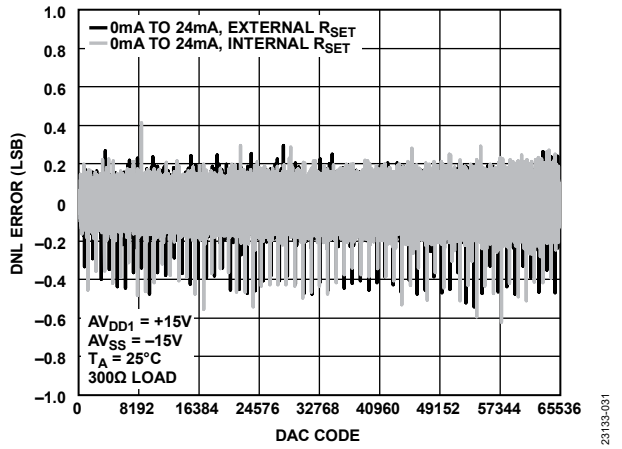


Figure 26. DNL Error vs. DAC Code

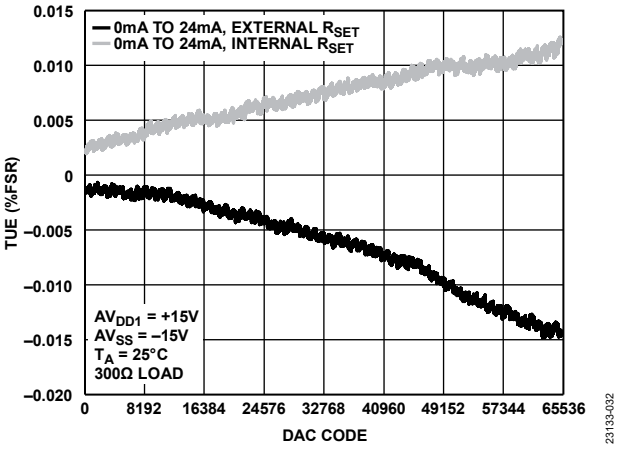


Figure 27. TUE vs. DAC Code

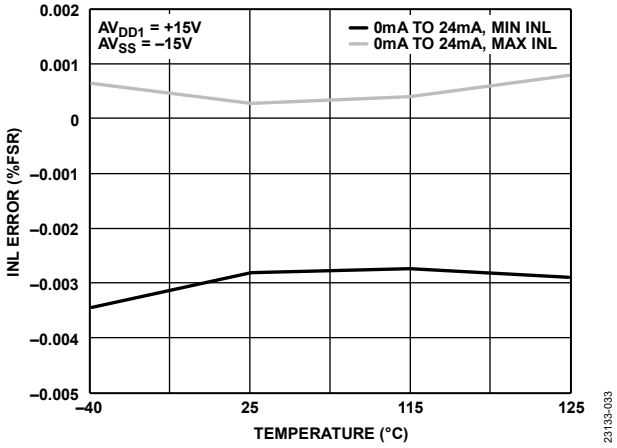


Figure 28. INL Error vs. Temperature, Internal R_{SET}

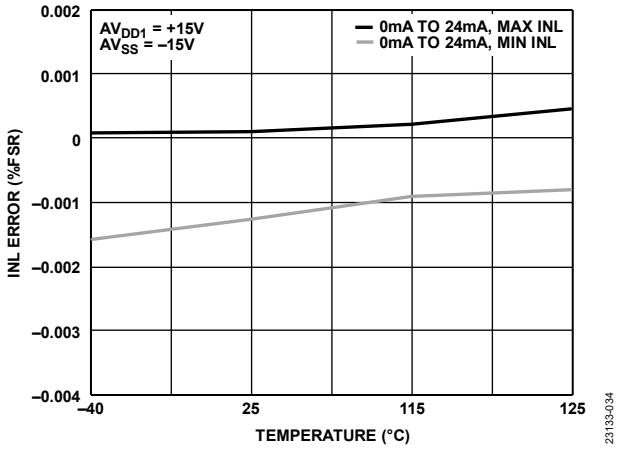


Figure 29. INL Error vs. Temperature, External R_{SET}

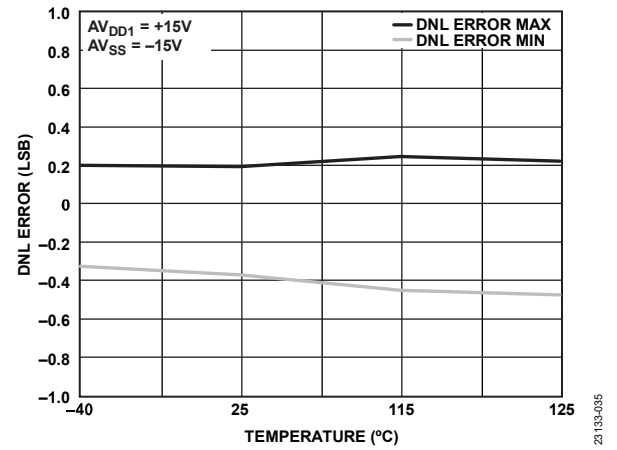


Figure 30. DNL Error vs. Temperature

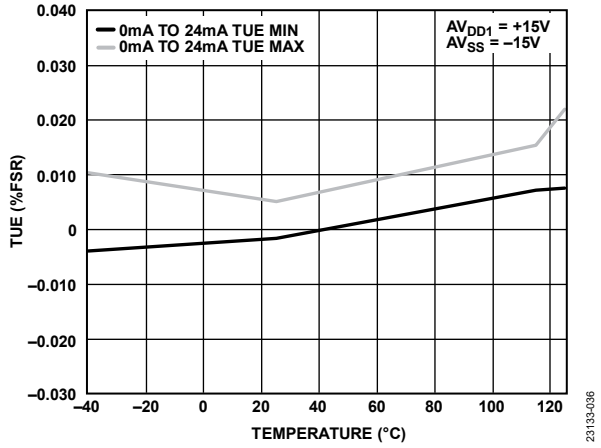


Figure 31. TUE vs. Temperature, Internal R_{SET}

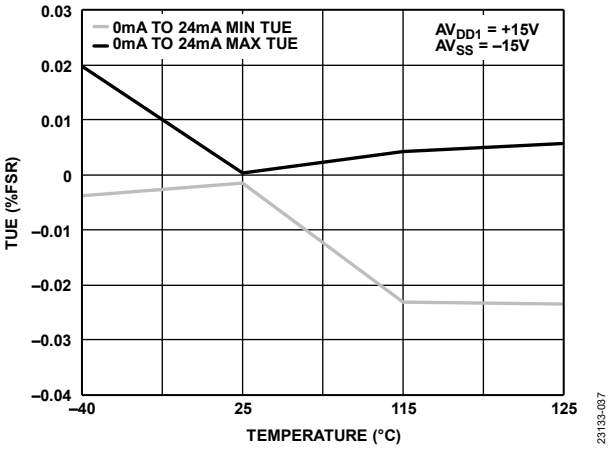


Figure 32. TUE vs. Temperature, External R_{SET}

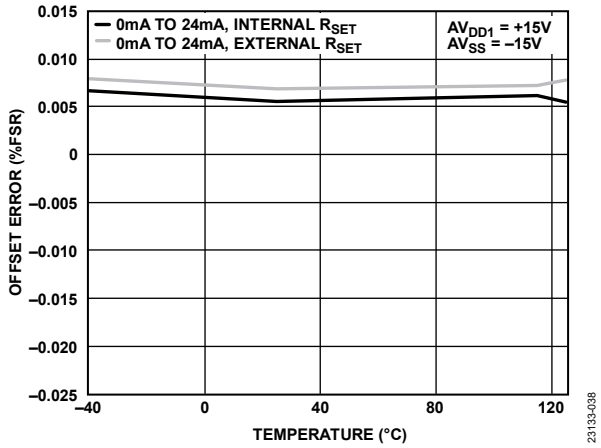


Figure 33. Offset Error vs. Temperature

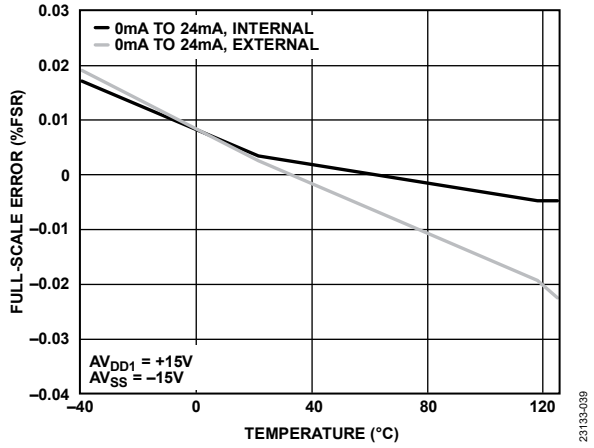


Figure 34. Full-Scale Error vs. Temperature

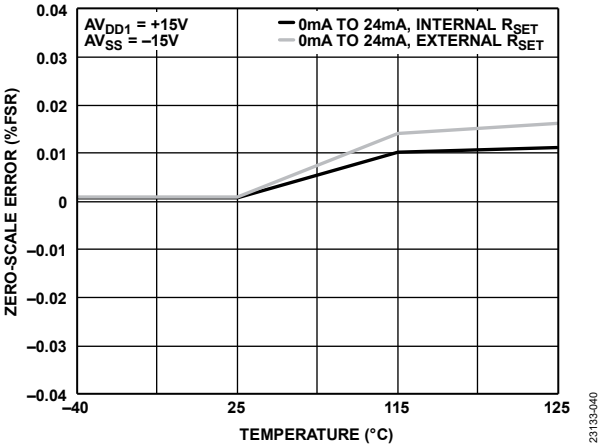


Figure 35. Zero-Scale Error vs. Temperature

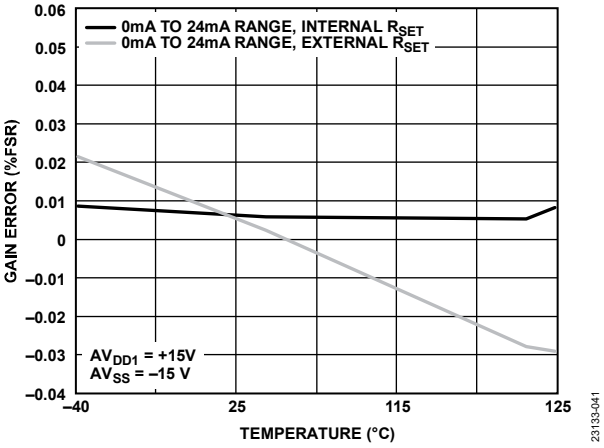


Figure 36. Gain Error vs. Temperature

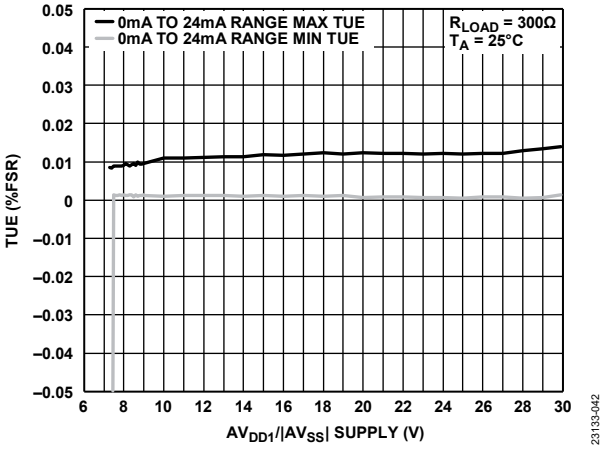


Figure 37. TUE vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

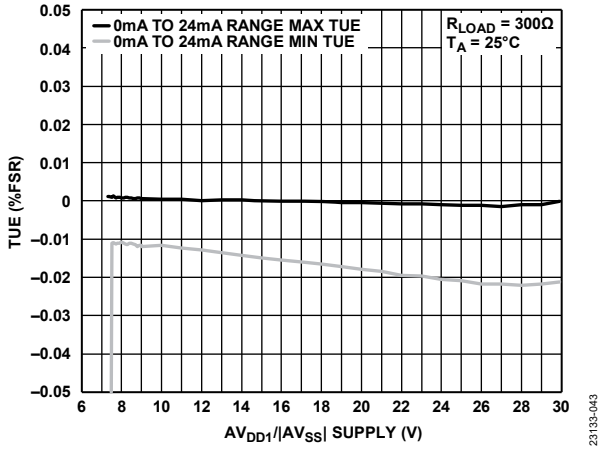


Figure 38. TUE vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

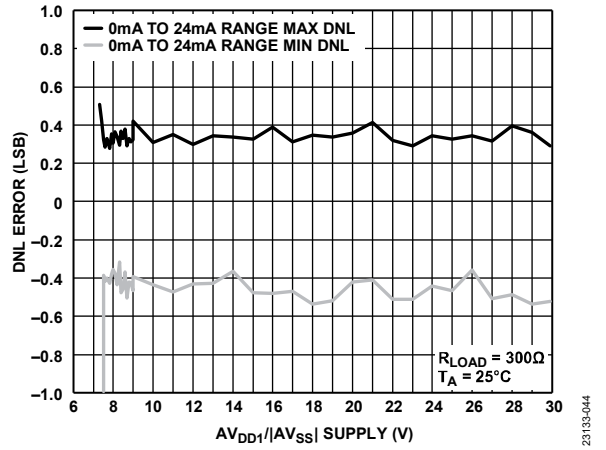


Figure 39. DNL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

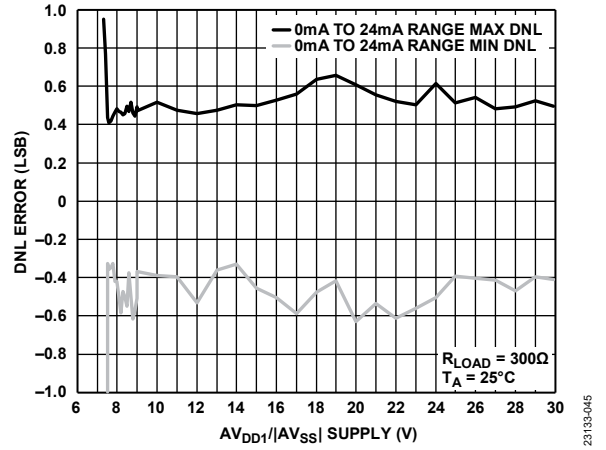


Figure 40. DNL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

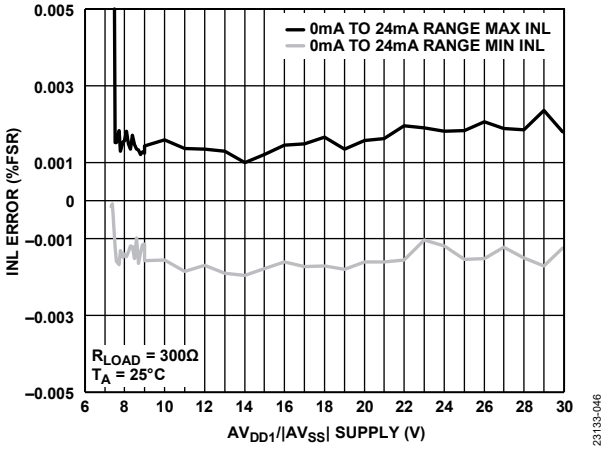


Figure 41. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

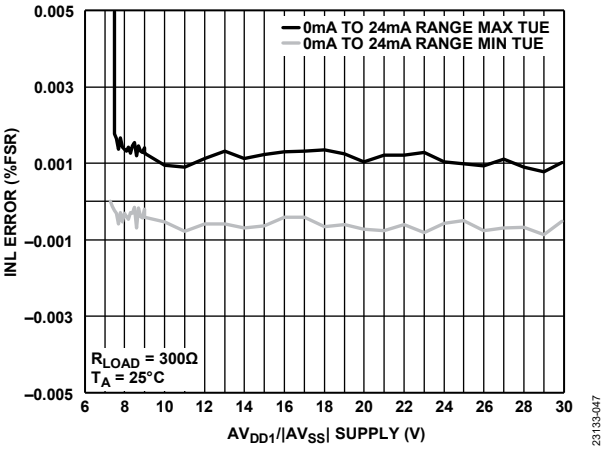


Figure 42. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

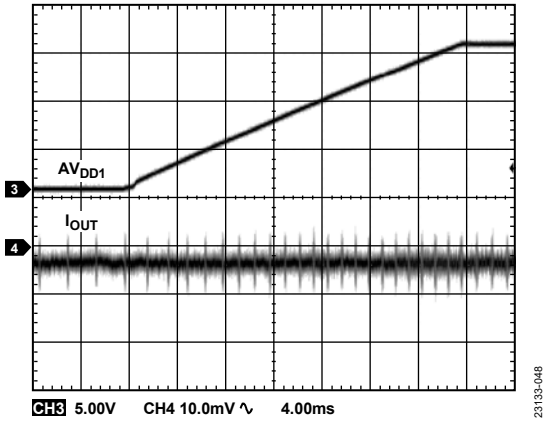


Figure 43. Output Current vs. Time on Power-Up

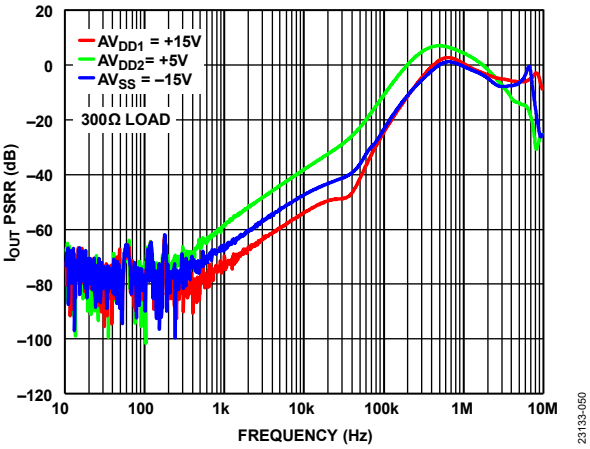


Figure 45. I_{OUT} PSRR vs. Frequency

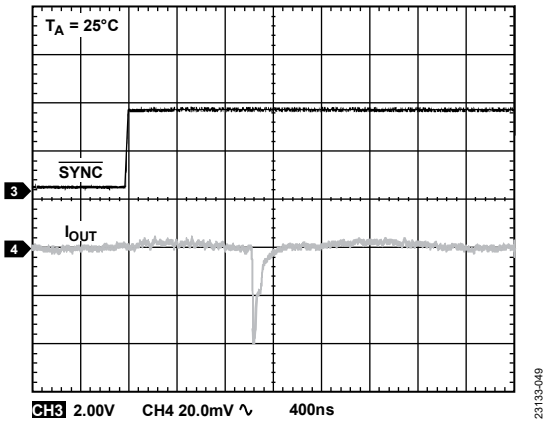


Figure 44. Output Current vs. Time on Output Enable

REFERENCE

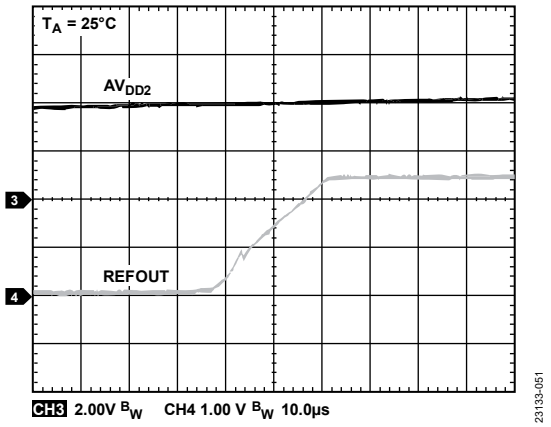


Figure 46. REFOUT Turn On Transient

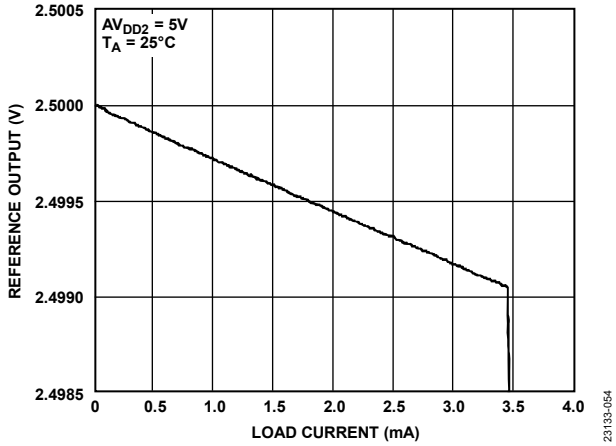


Figure 49. Reference Output vs. Load Current

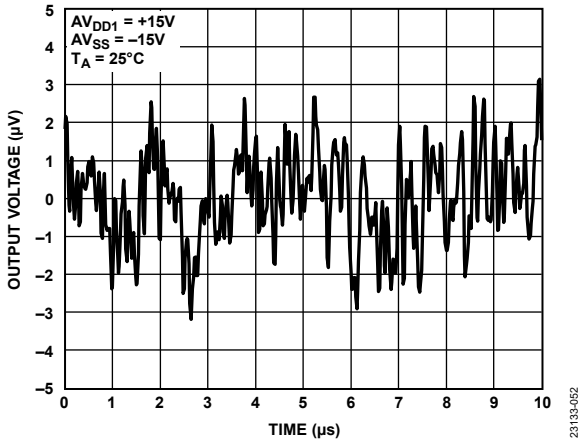


Figure 47. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

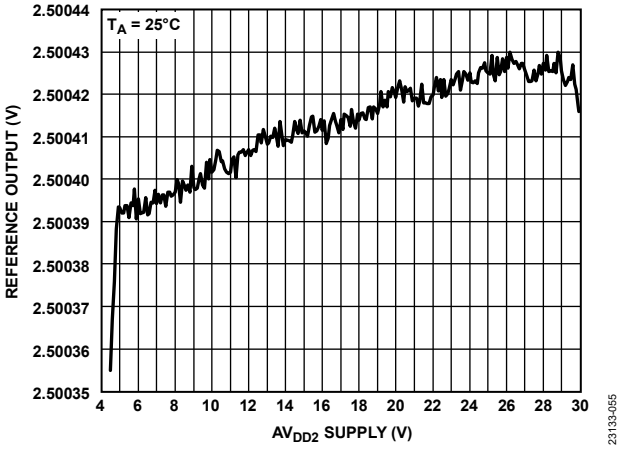


Figure 50. Reference Output vs. AV_{DD2} Supply

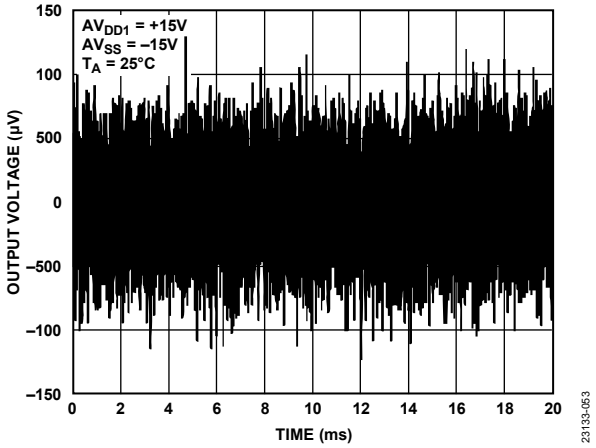


Figure 48. Peak-to-Peak Noise (100 kHz Bandwidth)

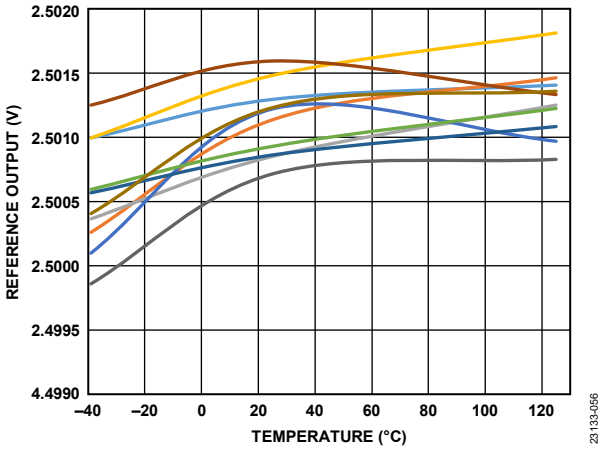


Figure 51. Reference Output vs. Temperature for Multiple Devices

GENERAL

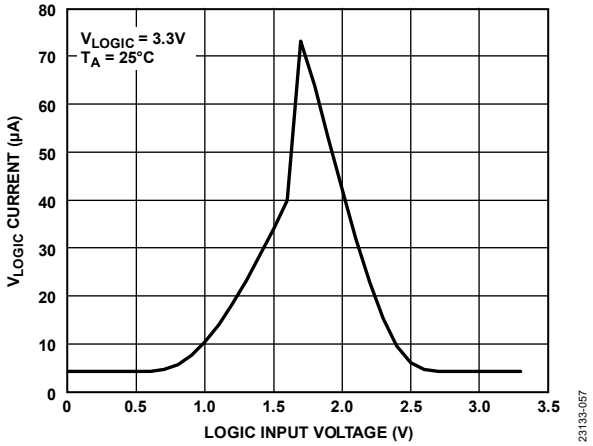


Figure 52. V_{LOGIC} Current vs. Logic Input Voltage

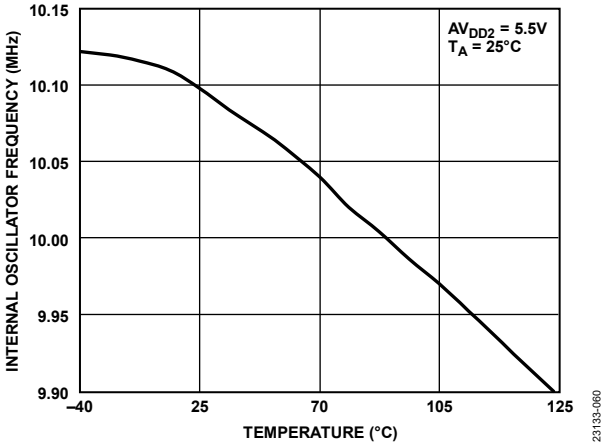


Figure 55. Internal Oscillator Frequency vs. Temperature

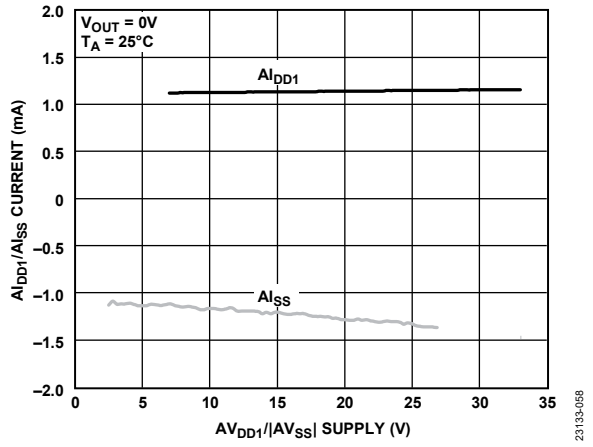


Figure 53. AI_{DD1}/AI_{SS} Current vs. $AV_{DD1}/|AV_{SS}|$ Supply

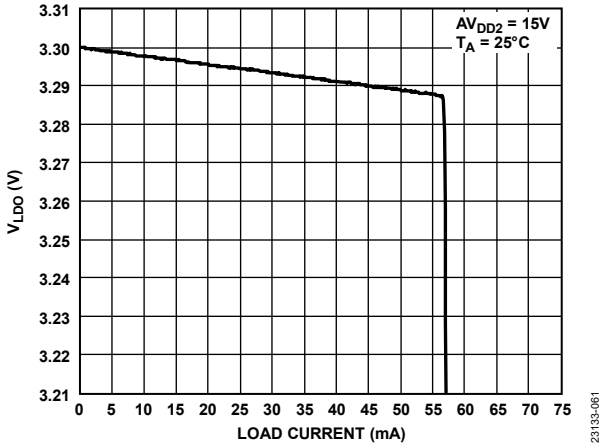


Figure 56. V_{LDO} vs. Load Current

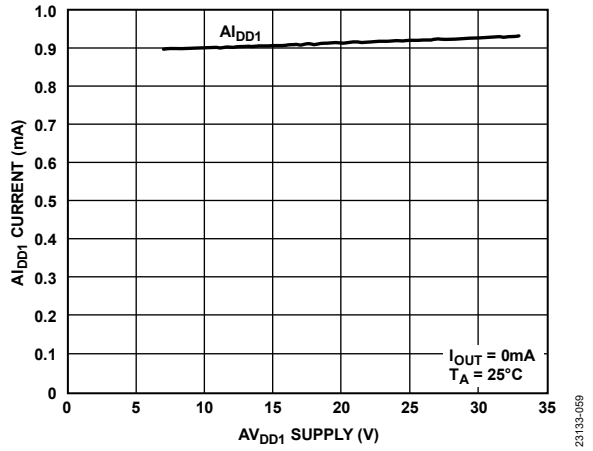


Figure 54. AI_{DD1} Current vs. AV_{DD1} Supply

TERMINOLOGY

Total Unadjusted Error (TUE)
TUE is a measure of the output error that takes into account various errors including INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or INL, is a measure of the maximum deviation from the best fit line passing through the DAC transfer function. INL is expressed either in LSBs or % FSR.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of a ±1 LSB maximum ensures monotonicity.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5413 is monotonic over the full operating temperature range.

Zero-Scale or Negative Full-Scale Error
Zero-scale, or negative full-scale error, is the error in the DAC output voltage when 0x0000 (straight binary coding) is loaded to the DAC output register.

Zero-Scale Temperature Coefficient
Zero-scale temperature coefficient is a measure of the change in the zero-scale error with a change in temperature. Zero-scale error temperature coefficient is expressed in ppm FSR/°C.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC output register is loaded with 0x8000 (straight binary coding).

Bipolar Zero Temperature Coefficient
Bipolar zero temperature coefficient is a measure of the change in the bipolar zero error with a change in temperature. Bipolar zero temperature coefficient is expressed in ppm FSR/°C.

Offset Error
Offset error is the deviation of the analog output from the ideal and is measured using ¼ scale and ¾ scale digital code measurements. Offset error is expressed in % FSR.

Offset Error Temperature Coefficient
Offset error temperature coefficient is a measure of the change in the offset error with a change in temperature. Offset error temperature coefficient is expressed in ppm FSR/°C.

Gain Error
Gain error is a measure of the span error of the DAC and is the DAC transfer characteristic slope deviation from the ideal value. Gain error is expressed in % FSR.

Gain Error Temperature Coefficient
Gain error temperature coefficient is a measure of the change in gain error with changes in temperature. Gain error temperature coefficient is expressed in ppm FSR/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC output register. Ideally, the output is full-scale − 1 LSB. Full-scale error is expressed in % FSR.

V_{OUT} or−V_{SENSE} Common-Mode Rejection Ratio (CMRR)
V_{OUT} or $-V_{SENSE}$ CMRR is the error in V_{OUT} that occurs because of changes in $-V_{SENSE}$.

Reference Thermal Hysteresis
Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C, then to +105°C, and then back to +25°C.

Reference Temperature Coefficient
Voltage reference temperature coefficient is a measure of the change in the reference output voltage with a change in temperature. To calculate the voltage reference temperature coefficient, use the box method. This method defines the temperature coefficient as the maximum change in the reference output over a given temperature range expressed in ppm/°C, and is calculated as follows:

$$TC = \left(\frac{V_{REF_MAX} - V_{REF_MIN}}{V_{REF_NOM} \times Temperature\ Range} \right) \times 10^6$$

where:
V_{REF_MAX} is the maximum reference output measured over the total temperature range.
V_{REF_MIN} is the minimum reference output measured over the total temperature range.
V_{REF_NOM} is the nominal reference output voltage, which in this case is 2.5 V.
Temperature Range is the specified temperature range, −40°C to +105°C.

Line Regulation
Line regulation is the change in reference output voltage that occurs because of a specified change in power supply voltage. Line regulation is expressed in ppm/V.

Load Regulation
Load regulation is the change in reference output voltage that occurs because of a specified change in reference load current. Load regulation is expressed in ppm/mA.

Output Voltage Settling Time
Output voltage settling time is the amount of time the output takes to settle to a specified level for a full-scale input change.

Slew Rate
The device slew rate is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage output DAC is typically limited by the slew rate of the amplifier used at the output. Slew rate is measured from 10% to 90% of the output signal and is expressed in V/µs.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5413 is powered on. Power-on glitch energy is specified as the area of the glitch in nV-sec.

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the energy of the impulse injected into the analog output when the input code in the DAC output register changes state. Digital-to-analog glitch energy is normally specified as the area of the glitch in nV-sec. The worst case of the glitch typically occurs when the digital input code is changed by 1 LSB at the major carry transition.

Glitch Impulse Peak Amplitude

Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC output register changes state. Glitch impulse peak amplitude is specified as the amplitude of the glitch in mV and the worst case of the glitch typically occurs when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the DAC analog output from the DAC digital inputs. However, the digital feedthrough is measured when the DAC output is not updated, which occurs when the $\overline{\text{LDAC}}$ pin is held high. The digital feedthrough is specified in nV-sec and is measured with a full-scale code change on the data bus.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the DAC output is affected by changes in the power supply voltage.

THEORY OF OPERATION

The AD5413 is a single-channel, 14-bit voltage and current output DAC that meets the requirements of industrial factory automation and process control applications. The device provides a high precision, fully integrated, single-chip solution to generate a unipolar current, bipolar current, or voltage output.

DAC ARCHITECTURE

The DAC core architecture of the AD5413 consists of a voltage mode R-2R DAC ladder network. The DAC core voltage output is converted to either a current output or a voltage output at the VI_{OUT} pin. Only one mode can be enabled at a time. The voltage and current output stages are both supplied by the AV_{DD1} power rail and the AV_{SS} power rail.

Current Output Mode

When current output mode is enabled, the DAC voltage output is converted to a current that is mirrored to the supply rail so that the application only sees a current source output (see Figure 57).

An internal or external 13.7 kΩ R_{SET} resistor can be used for the voltage to current conversion.

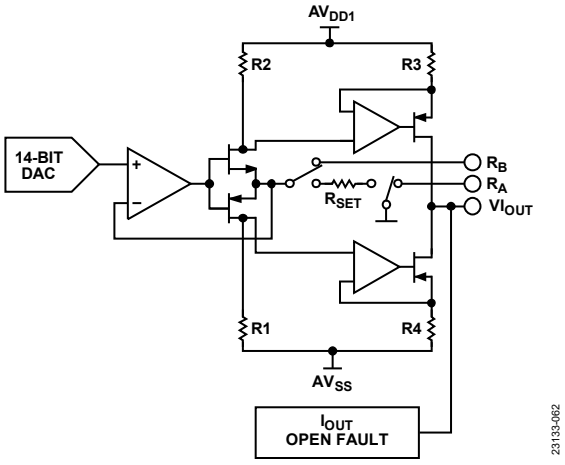


Figure 57. Voltage to Current Conversion Circuitry

Voltage Output Mode

When voltage output mode is enabled, the DAC voltage output is buffered and scaled to output a software selectable, unipolar or bipolar voltage range (see Figure 58).

The available voltage output range is ±10.5 V. A 20% overrange feature is also available via the DAC_CONFIG register.

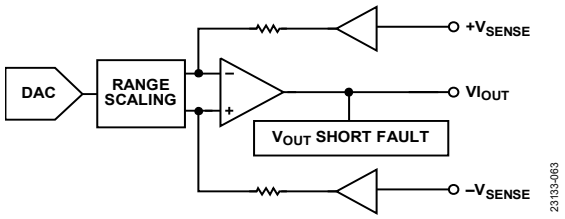


Figure 58. Voltage Output Architecture

Reference

The AD5413 can operate with either an external or internal reference. The reference input requires a 2.5 V reference for specified performance. This input voltage is internally buffered before being applied to the DAC.

The AD5413 has an integrated, buffered, 2.5 V voltage reference that is externally available for use elsewhere within the system. To use the internal reference to drive the DAC, connect the REFOUT pin to the REFIN pin.

SPI

The AD5413 is controlled over a versatile, 4-wire SPI that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP standards. Data coding is always straight binary.

Input Shift Register

With the SPI CRC enabled (default state), the input shift register is 32 bits wide. Data is loaded to the device MSB first as a 32-bit word under the control of SCLK. Data is clocked in on the falling edge of SCLK. If the CRC is disabled, the serial interface reduces to 24 bits. In this case, a 32-bit frame is still accepted, but the last 8 bits are ignored. See the AD5413 Register section for full details on the registers that can be addressed via the SPI interface.

Table 8. Writing to a Register (CRC Enabled)

MSB				LSB
D31	**[D30:D29]**	**[D28:D24]**	**[D23:D8]**	**[D7:D0]**
Slip bit	AD5413 address	Register address	Data	CRC

Transfer Function

Table 9 shows the ideal output voltage to AD5413 input code relationship for straight binary data coding of the ±10.5 V output range. The lower 2 bits are unused and must not be written to.

Table 9. Ideal Output Voltage to Input Code Relationship[1]

Digital Input, Straight Binary Data Coding				Analog Output
MSB		LSB[2]		V_{OUT} (V)
1111	1111	1111	11XX	10.5 × (8192/8192)
1111	1111	1111	10XX	10.5 × (8191/8192)
1000	0000	0000	00XX	0
0000	0000	0000	01XX	−10.5 × (8191/8192)
0000	0000	0000	00XX	−10.5

[1] Assuming a 2.5 V voltage reference.
[2] X means do not write.

POWER-ON STATE

On initial power-on or a device reset of the AD5413, the voltage and current output channels are disabled. The switch connecting VI_{OUT} to AGND via a 30 kΩ pull-down resistor opens. To enable this switch, see the General-Purpose Configuration 1 Register section.

A calibration memory refresh command is required after a device power-on or a device reset (see the Programming Sequence to Enable the Output section). When this command is written, wait a minimum of 500 µs before writing further instructions to the device to allow time for internal calibrations to take place (see Figure 70).

Power-On Reset

The AD5413 incorporates a power-on reset circuit to ensure that the AD5413 is held in reset if the power supplies are insufficient to allow reliable operation. The power-on reset circuit (see Figure 59) monitors the V_{LDO} generated from the AV_{DD2} external supply, the INT_AVCC internal node voltages, the $\overline{\text{RESET}}$ pin, and the SPI reset signals. The power-on reset circuit holds the AD5413 in reset until the voltages on the V_{LDO} and the INT_AVCC nodes are sufficient for reliable operation. If the power-on reset circuit receives a signal from the $\overline{\text{RESET}}$ pin, or if a software reset is written to the AD5413 via the SPI interface, the AD5413 resets. Do not write SPI commands to the device within 100 µs of a reset event.

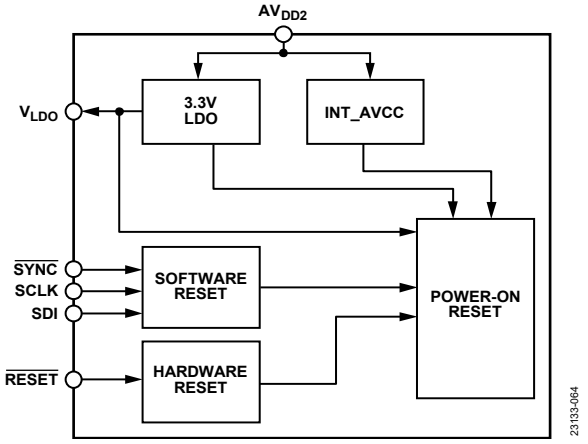


Figure 59. Power-On Reset Block Diagram

POWER SUPPLY CONSIDERATIONS

The AD5413 has four supply rails: AV_{DD1}, AV_{DD2}, AV_{SS}, and V_{LOGIC}. See Table 1 for the voltage range of the four supply rails and the associated conditions.

AV_{DD1} Considerations

AV_{DD1} is the DAC supply rail and has a voltage range from 7 V to 33 V. Although the maximum value of AV_{DD1} is 33 V and the minimum value of AV_{SS} is −33 V, the maximum operating range of $|AV_{DD1}$ to $AV_{SS}|$ is 50 V. The minimum AV_{DD1} can be calculated as $(I_{OUT_MAX} \times R_{LOAD}) + I_{OUT_HEADROOM}$.

where:
I_{OUT_MAX} is the maximum current output for the current range selected by the user.
$I_{OUT_HEADROOM}$ is the headroom voltage needed for the current output mode.

AV_{SS} Considerations

AV_{SS} is the negative analog supply rail and has a voltage range of 0 V to −33 V. AV_{SS} must also operate within the maximum operating range of $|AV_{DD1}$ to $AV_{SS}| = 50$ V.

AV_{DD2} Considerations

AV_{DD2} is the positive low voltage analog supply rail and has a voltage range of 4.5 V to 33 V. If only one positive power rail is available, AV_{DD2} can be tied to AV_{DD1}. To optimize reduced power dissipation, supply AV_{DD2} with a separate, lower voltage supply.

V_{LOGIC} Considerations

V_{LOGIC} is the digital supply and has a voltage range from 1.71 V to 5.5 V. The 3.3 V V_{LDO} output voltage can be used to drive V_{LOGIC}.

APPLICATIONS INFORMATION

VOLTAGE OUTPUT

Voltage Output Amplifier and +V_{SENSE} Functionality

The voltage output amplifier can generate both unipolar and bipolar output voltages. The amplifier can use an external compensation capacitor connected to the AGND signal to drive a 1 kΩ load in parallel with 2 μF.

Figure 60 shows the voltage output driving a load, R_{LOAD}, on top of a common-mode voltage (V_{CM}) of ±10 V. An integrated 2 MΩ resistor ensures that the amplifier loop is kept closed and prevents potentially large and damaging voltages on VIOUT because of the broken amplifier loop in applications where a cable can disconnect from +V_{SENSE}. If remote sensing of the load is not required, connect +V_{SENSE} directly to V_{IOUT} via the 1 kΩ series resistor and connect −V_{SENSE} directly to AGND via the external 1 kΩ series resistor.

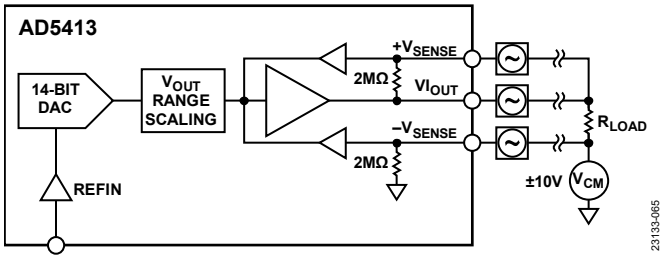


Figure 60. Voltage Output Load Connection

Driving Large Capacitive Loads

An additional external, 220 pF, nonpolarized compensation capacitor allows the voltage output amplifier to drive capacitive loads of up to 2 μF. This capacitor allows the AD5413 to drive higher capacitive loads and reduce overshoot, but this capacitor also increases the device settling time and negatively affects the bandwidth of the system. Without the compensation capacitor, capacitive loads of up to 10 nF can be driven.

Voltage Output Short-Circuit Protection

Under normal operation, the voltage output sinks and sources up to 12 mA and maintains specified operation. The short-circuit current is typically 15 mA. If a short circuit is detected, the $\overline{\text{FAULT}}$ pin goes low and the VOUT_SC_ERR bit in the ANALOG_DIAG_RESULTS register is set.

CURRENT OUTPUT

External Current Setting Resistor

As shown in Figure 57, R_{SET} is an internal sense resistor that forms part of the voltage to current conversion circuitry. The stability of the output current value overtemperature depends on the stability of the R_{SET} value. To improve the output current overtemperature stability, connect an external, 13.7 kΩ, low drift resistor between the AD5413 R_A pin and R_B pin instead of the internal resistor.

Table 1 shows the AD5413 performance specifications with both the internal R_{SET} resistor and an external 13.7 kΩ R_{SET} resistor. The external R_{SET} resistor specification assumes an ideal resistor. The actual device performance depends on the absolute value and temperature coefficient of the resistor used. Therefore, the resistor specifications directly affect the gain error of the output and the TUE.

To arrive at the absolute worst case overall TUE of the output with a particular external R_{SET} resistor, add the percentage of the R_{SET} resistor absolute error (the absolute value of the error) to the TUE of the AD5413 that is using the R_{SET} external resistor shown in Table 1 (expressed in % FSR). Consider the temperature coefficient as well as the specifications of the external reference if this option is used in the system.

The magnitude of the error (derived from summing the absolute error and the temperature coefficient error of the external R_{SET} resistor and the external reference with the AD5413 TUE specification) is unlikely to occur because the temperature coefficient values of the individual components are unlikely to exhibit the same drift polarity and an element of cancellation occurs. For this reason, add the temperature coefficient values with a root of squares method. To gain further TUE specification improvement, perform a two-point calibration at zero-scale and full-scale, which reduces the absolute errors of the voltage reference and the R_{SET} resistor.

Current Output Open-Circuit Detection

When in current output mode, if the available headroom falls below the compliance range because of an open-loop circuit or an insufficient power supply voltage, the IOUT_OC_ERR bit flag in the ANALOG_DIAG_RESULTS register is asserted and the $\overline{\text{FAULT}}$ pin goes low.

HART CONNECTIVITY

A HART signal can be ac-coupled onto the AD5413 C_{HART} pin. The HART signal appears on the current output if the HART_EN bit in the GP_CONFIG1 register as well as the VI_{OUT} output are enabled. Figure 61 shows the recommended circuit for attenuating and coupling the HART signal into the AD5413. To achieve 1 mA p-p at the V_{IOUT} pin, a signal of approximately 125 mV p-p is required at the C_{HART} pin. The HART signal on the V_{IOUT} pin is inverted relative to the signal input at the C_{HART} pin.

In addition to being used to attenuate the incoming HART modem signal, a minimum capacitance of the C1 and C2 capacitors is required to ensure that the bandwidth presented to the modem output signal allows the 1.2 kHz and 2.2 kHz frequencies through the capacitors. Assuming a HART signal of 500 mV p-p, the recommended capacitance values are C1 = 47 nF and C2 = 150 nF. Digitally controlling the output slew rate is required to meet the analog rate of change requirements for the HART protocol.

If the HART feature is not required, disable the HART_EN bit and leave the C_{HART} pin as an open circuit. If the DAC output signal must be slowed with a capacitor, enable the HART_EN bit and connect the required C2 capacitor to the C_{HART} pin.

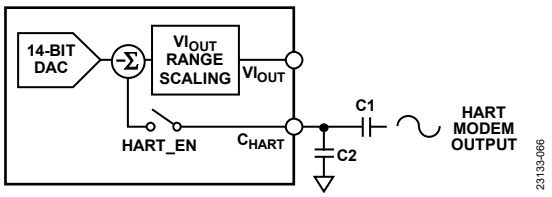


Figure 61. Coupling the HART Signal

DEVICE FEATURES AND DIAGNOSTICS

DIGITAL SLEW RATE CONTROL

The AD5413 slew rate control feature allows the user to control the rate at which the output value changes. This feature is available in both current mode and voltage mode. Disabling the slew rate control feature changes the output value at a rate limited by the output drive circuitry and the attached load. To reduce the slew rate, enable the slew rate control feature to cause the output to digitally step from one output value to the next at a rate defined by two parameters that are accessible via the DAC_CONFIG register. These two parameters are SR_CLOCK and SR_STEP. The SR_CLOCK parameter defines the rate at which the digital slew is updated. For example, if the selected update rate is 8 kHz, the output updates every 125 µs. In conjunction with the SR_CLOCK parameter, the SR_STEP parameter defines how much the output value changes at each update. Together, both parameters define the rate of change of the output value. The following equation describes the slew rate as a function of the step size, the slew rate frequency, and the LSB size:

$$Slew\ Time = \frac{Output\ Change}{Step\ Size \times Slew\ Rate\ Frequency \times LSB\ Size}$$

where:
Slew Time is expressed in seconds.
Output Change is expressed in amps for current output mode or volts for voltage output mode.
Step Size is the step size in amps for current output mode, or volts for voltage output mode.
Slew Rate Frequency is the SR_CLOCK parameter value.
LSB Size is the SR_STEP parameter value.

When the slew rate control feature is enabled, all output changes occur at the programmed slew rate.

AD5413 ADDRESS PINS

The AD5413 address pins (AD0 and AD1) are used in conjunction with the AD5413 address bits within the SPI frame (see Table 10) to determine which AD5413 device is being addressed by the system controller. Up to four devices can be independently addressed on one board using the two address pins.

SPI INTERFACE AND DIAGNOSTICS

The AD5413 is controlled over a 4-wire SPI with an 8-bit cyclic redundancy check (CRC-8) that is enabled by default. The input shift register is 32 bits wide and data is loaded into the device MSB first under the control of the SCLK signal. Data is clocked in on the falling edge of SCLK. If CRC is disabled, the SPI is reduced to 24 bits. A 32-bit frame is still accepted, but the last 8 bits are ignored.

Table 10. Writing to a Register (CRC Enabled)

MSB				LSB
D31	**[D30:D29]**	**[D28:D24]**	**[D23:D8]**	**[D7:D0]**
Slip bit	AD5413 address	Register address	Data	CRC

As shown in Table 10, every SPI frame contains two AD5413 address bits. These bits must match the AD0 pin and AD1 pin for a particular device to accept the SPI frame on the bus.

SPI Cyclic Redundancy Check

To verify that data is correctly received in noisy environments, the AD5413 offers a CRC based on a CRC-8. The device controlling the AD5413, either a micro gate array or a field-programmable gate array (FPGA), generates an 8-bit frame check sequence using the following polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

This 8-bit frame check sequence is added to the end of the data-word and 32 bits are sent to the AD5413 before pulling $\overline{\text{SYNC}}$ high (see Figure 62).

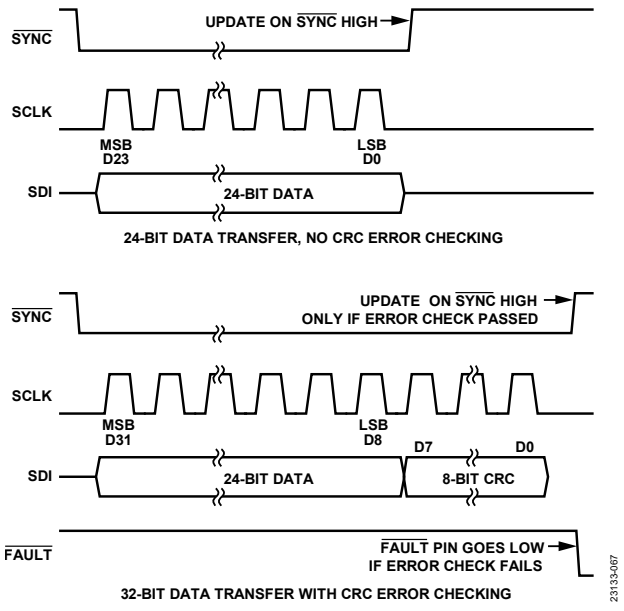


Figure 62. CRC Timing (Assume $\overline{LDAC}$ = 0)

If the SPI_CRC_EN bit in the DIGITAL_DIAG_CONFIG register is set high (default state), supply a frame that is exactly 32 bits wide and contains the 24 data bits and the 8-bit CRC. If the CRC check is valid, the data is written to the selected register. If the CRC check fails, the data is ignored, the $\overline{\text{FAULT}}$ pin goes low, and the $\overline{\text{FAULT}}$ pin status bit and the digital diagnostic status bit (DIG_DIAG_STATUS) in the status register are asserted. A subsequent readback of the DIGITAL_DIAG_RESULTS register shows that the SPI_CRC_ERR bit is also set. This register is per individual bits. A write one per bit clears the register (see the

Sticky Diagnostic Results Bits section for more details). Therefore, to clear the SPI_CRC_ERR bit, write a 1 to Bit 0 of the DIGITAL_DIAG_RESULTS register. Writing a 1 clears the SPI_CRC_ERR bit and causes the FAULT pin to return high, assuming that there are no other active faults. When configuring the FAULT_PIN_CONFIG register, the user decides whether the SPI CRC error affects the FAULT pin. See the FAULT Pin Configuration Register section for more details. The SPI CRC feature is used for both transmitting and receiving data packets.

SPI Interface Slip Bit

An additional slip bit enhances the interface robustness. The MSB of the SPI frame must equal the inverse of MSB – 1 for the frame to be considered valid. If an incorrect slip bit is detected, the data is ignored and the SLIPBIT_ERR bit in the DIGITAL_DIAG_ RESULTS register is asserted.

SPI Interface SCLK Count Feature

An SCLK count feature is also built into the SPI diagnostics. If the CRC is enabled, only SPI frames with exactly 32 SCLK falling edges are accepted by the interface as a valid write. If the CRC is disabled, SPI fames with either 24 or 32 SCLK falling edges are accepted by the interface as a valid write. SPI frame lengths other than these are ignored and the SCLK_COUNT_ERR flag asserts in the DIGITAL_DIAG_RESULTS register.

Readback Modes

The AD5413 offers the following four readback modes:

- Two-stage readback mode
- Autostatus readback mode
- Shared SYNC autostatus readback mode
- Echo mode

The two-stage readback consists of a write to a dedicated register, TWO_STAGE_READBACK_SELECT, to select the register location to be read back. This write is followed by a no operation (NOP) command, during which the contents of the selected register are available on the SDO pin.

Table 11. SDO Contents for Read Operation

MSB				LSB
[D31:D30]	D29	[D28:24]	[D23:D8]	[D7:D0]
0b10	FAULT pin status	Register address	Data	CRC

Bits[D31:D30] = 0b10 are used for synchronization purposes during readback.

If autostatus readback mode is selected, the status register contents are available on the SDO line during each SPI transaction. This feature allows the user to continuously monitor the status register and to act quickly if a fault occurs. The AD5413 powers up with this feature disabled. When this feature is enabled, the normal two-stage readback feature is not available. Only the status register is available on the SDO when autostatus readback mode is selected. To read back other registers, disable the automatic readback feature and then follow the two-stage readback sequence. The automatic status readback can be re-enabled after the register is read back.

The shared AD5413 SYNC autostatus readback is a unique version of the autostatus readback mode used to avoid SDO bus contention when multiple devices share the same SYNC line. See the Shared Autostatus Readback Mode section for more details. Echo mode behaves similarly to autostatus readback mode, except that every second readback consists of an echo of the previous command written to the AD5413 (see Figure 63). See the Reading from Registers section for further details on the readback modes.

Figure 63. SDO Contents in Echo Mode

USER DIGITAL OFFSET AND GAIN CONTROL

The AD5413 has a USER_GAIN register and a USER_OFFSET register that trim the gain and offset errors from the entire signal chain. The USER_GAIN register allows the user to adjust the DAC channel gain in steps of 1 LSB. The USER_GAIN register coding is straight binary, as shown in Table 12. The default code in the USER_GAIN register is 0xFFFC, which results in a no gain factor applied to the programmed output. In theory, the gain can be tuned across the full range of the output. In practice, the maximum recommended gain trim is approximately 50% of the programmed range to maintain accuracy. The lower two bits, D1 and D0, are unused and must not be written to.

Table 12. Gain Register Adjustment

Gain Adjustment Factor	D13	[D12:D3]	D2	[D1:D0]
1	1	1	1	X
16383/16384	1	1	0	X
…	…	…	…	X
2/16384	0	0	1	X
1/16384	0	0	0	X

The USER_OFFSET register allows the user to adjust the DAC channel offset from −8192 LSBs to +8192 LSBs in steps of 1 LSB. The USER_OFFSET register coding is straight binary, as shown in Table 13. The default code in the USER_OFFSET register is 0x8000, which results in zero offset programmed to the output. The lower two bits, D1 and D0, are unused and must not be written to.

Table 13. Offset Register Adjustment

Gain Adjustment Factor	D13	[D12:D3]	D2	[D1:D0]
+8192 LSBs	1	1	1	X
+8191LSBs	1	1	0	X
…	…	…	…	X
No Adjustment (Default)	1	0	0	X
…	…	…	…	X
−8191 LSBs	0	0	1	X
−8192 LSBs	0	0	0	X

To calculate the decimal value that is written to the internal DAC register (DAC_{CODE}), use the following equation:

$$DAC_{CODE} = D \times \frac{(M+1)}{2^{14}} + C - 2^{13}$$

where:
D is the code loaded to the DAC_INPUT register.
M is the code in the USER_GAIN register (default code = $2^{14} - 1$).
C is the code in the USER_OFFSET register (default code = 2^{13}).

Data from the DAC_INPUT register is processed by a digital multiplier and adder, which are controlled by the contents of the USER_GAIN register and USER_OFFSET register, respectively. The calibrated DAC data is loaded to the DAC. The DAC data loading depends on the state of the $\overline{\text{LDAC}}$ pin.

Each time data is written to the USER_GAIN register or USER_OFFSET register, the DAC output is not automatically updated. Instead, the next write to the DAC_INPUT register uses these user gain and user offset values to perform a new calibration and automatically update the output channel. The read only DAC_OUTPUT register represents the value currently loaded into the DAC before any user gain or user offset calibrations are applied.

The USER_GAIN register and the USER_OFFSET register both have 14 bits of resolution. Always calibrate the gain first and then calibrate the offset.

DAC OUTPUT UPDATE AND DATA INTEGRITY DIAGNOSTICS

Figure 64 shows a simplified version of the DAC input loading circuitry. If the gain and offset are used, update the USER_GAIN register and USER_OFFSET register before writing to the DAC_INPUT register.

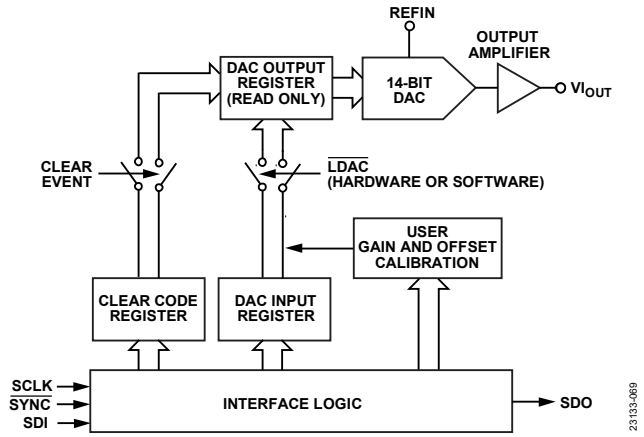


Figure 64. Simplified Serial Interface of Input Loading Circuitry

The DAC_OUTPUT register and the DAC output update in any of the following cases:

- If a write is performed on the DAC_INPUT register with the hardware $\overline{\text{LDAC}}$ pin tied low, the DAC_OUTPUT register updates on the rising edge of $\overline{\text{SYNC}}$ and is subject to the timing specifications in Table 3.
- If a write is performed on the DAC_INPUT register with the hardware $\overline{\text{LDAC}}$ pin tied high, the DAC_OUTPUT register does not update until a software $\overline{\text{LDAC}}$ instruction is issued or the hardware $\overline{\text{LDAC}}$ pin is pulsed low.
- If the slew rate control feature is enabled, the DAC_OUTPUT register contains the dynamic value of the DAC as the register slews between values.

The GP_CONFIG2 register contains a bit to enable a global software LDAC active low mode that ignores the AD5413 address bits of the SW_LDAC command, which enables multiple AD5413 devices to be simultaneously updated with a single SW_LDAC command. This feature is useful if the hardware $\overline{\text{LDAC}}$ pin is not being used in a system containing multiple AD5413 devices.

DAC Data Integrity Diagnostics

To protect against transient changes to the internal digital circuitry, the digital block stores both the digital DAC value and an inverted copy of the digital DAC value. A check is completed to ensure that the two values correspond to each other before the DAC is strobed to update to the DAC code. This matching feature is enabled by default via the INVERSE_DAC_CHECK_EN bit in the DIGITAL_DIAG_CONFIG register.

Outside of the digital block, the DAC code is stored in latches, as shown in Figure 65. These latches are potentially vulnerable to the same transient events that affect the digital block. To protect the DAC latches against such transients, enable the DAC latch monitor feature via the DAC_LATCH_MON_EN bit within the DIGITAL_DIAG_CONFIG register. This latch monitor feature monitors the actual digital code driving the DAC and compares the code with the digital code generated within the digital block. Any difference between the two codes sets the DAC_LATCH_MON_ERR bit flag in the DIGITAL_DIAG_RESULTS register.

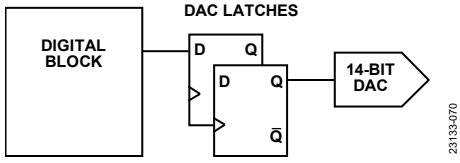


Figure 65. DAC Data Integrity

USE OF KEY CODES

Key codes are used via the key register to initiate calibration memory refresh and initiate a software reset (see the Key Register section for more details).

Using specific keys to initiate actions such as a calibration memory refresh or a software reset provides extra system robustness because the keys reduce the probability of either task being initiated in error.

SOFTWARE RESET

A software reset requires two consecutive writes of 0x15FA and 0xAF51, respectively, to the key register. A device reset can be initiated via the hardware $\overline{\text{RESET}}$ pin or the software reset keys. The RESET_OCCURRED bit in the DIGITAL_DIAG_RESULTS register is set when the device is reset. This bit defaults to 1 on power-up. Both diagnostic results registers implement a write of 1 to clear the function. That is, write a 1 to this bit to clear the bit (see the Sticky Diagnostic Results Bits section).

CALIBRATION MEMORY CRC

For each calibration memory refresh cycle, which is either initiated via a key code write to the key register or automatically initiated when the RANGE bits (Bits[3:0]) of the DAC_CONFIG register are changed, an automatic CRC is calculated on the contents of the calibration memory shadow registers. The result of this CRC is compared with the factory stored reference CRC value. If the CRC values match, the read of the entire calibration memory is considered valid. If the values do not match, the CAL_MEM_CRC_ERR bit in the DIGITAL_DIAG_RESULTS register is set to 1. This calibration memory CRC feature is enabled by default. Disable this feature via the CAL_MEM_CRC_EN bit in the DIGITAL_DIAG_CONFIG register.

Two-stage readback commands are permitted while this calibration memory refresh cycle is active. However, a write to any register other than the TWO_STAGE_READBACK_SELECT register or the NOP register sets the INVALID_SPI_ACCESS_ERR bit in the DIGITAL_DIAG_RESULTS register. As described in the Programming Sequence to Enable the Output section, a wait period of 500 µs is recommended after a calibration memory refresh cycle is initiated.

INTERNAL OSCILLATOR DIAGNOSTICS

An internal frequency monitor uses the internal oscillator (MCLK) to increment a 16-bit counter at a rate of 1 kHz (MCLK/10000). The counter value can be read in the FREQ_MONITOR register. The user can poll this register periodically and use the result as a diagnostic tool for MCLK (to monitor that the oscillator is running) and to measure the oscillator frequency. This counter feature is enabled by default via the FREQ_MON_EN bit in the DIGITAL_DIAG_CONFIG register.

If the MCLK oscillator stops, the AD5413 sends a specific code of 0x07DEAD to the SDO line for each SPI frame. This oscillator dead code feature is enabled by default. To disable this feature, clear the OSC_STOP_DETECT_EN bit in the GP_CONFIG1 register. This feature is limited to the maximum readback timing specifications described in Table 3.

STICKY DIAGNOSTIC RESULTS BITS

The AD5413 contains a digital diagnostic results register (DIGITAL_DIAG_RESULTS) and an analog diagnostic results register (ANALOG_DIAG_RESULTS) (see Table 36 and Table 37, respectively, for the diagnostic error bits). The diagnostic results bits contained within these registers are sticky and a 1 must be written to each bit to clear the error bit (R/W-1-C). If the fault is still present after writing a 1 to the bit in question, the error bit does not clear to 0. When Logic 1 is written to the bit, the bit updates to the latest value, which is Logic 1 if the fault is still present, and Logic 0 if the fault is no longer present.

There are two exceptions to this R/W-1-C access within the DIGITAL_DIAG_RESULTS register, the CAL_MEM_UNREFRESHED bit and the SLEW_BUSY bit, which automatically clear when the calibration memory refreshes and when the output slew completes, respectively.

The STATUS register contains a DIG_DIAG_STATUS bit and an ANA_DIAG_STATUS bit. Both bits are the result of a logical OR of the diagnostic results bits contained in each diagnostic results register. All analog diagnostic flag bits are included in the logical OR of the ANA_DIAG_STATUS bit, and all digital diagnostic flag bits, except for the SLEW_BUSY bit, are included in the logical OR of the DIG_DIAG_STATUS bit. The OR'ed bits within the status register are read only and are not sticky (R/W-1-C).

BACKGROUND SUPPLY AND TEMPERATURE MONITORING

Excessive die temperature and overvoltage are related to common cause failures.

The die has a built in temperature sensor with a ±5°C accuracy. The die temperature is monitored by a comparator and the background temperature comparators are permanently enabled. Programmable trip points corresponding to 142°C, 127°C, 112°C, and 97°C can be configured in the GP_CONFIG1 register. If the temperature of the die exceeds the programmed limit, the relevant status bit in the ANALOG_DIAG_RESULTS register is set, and the $\overline{\text{FAULT}}$ pin asserts low.

The low voltage supplies on the AD5413 are monitored via low power static comparators. This monitoring function is disabled by default and is enabled via the COMPARATOR_CONFIG bits in the GP_CONFIG2 register. The INT_EN bit in the DAC_CONFIG register must be set for the REFIN buffer to be powered up and for this node to be available to the REFIN comparator. The monitored nodes are REFIN, REFOUT, V_{LDO}, and an internally generated AV_{CC} voltage. A status bit in the ANALOG_DIAG_RESULTS register corresponds to each monitored node. If any monitored node supplies exceed the upper or lower threshold values (see Table 14 for the threshold values), the corresponding status bit is set. Note that if a REFOUT fault occurs, the REFOUT_ERR status bit is set. The INT_AVCC, VLDO, and temperature comparator status bits (DIE_TEMP_ERR) can then also be set because REFOUT is used as the comparison voltage for these nodes.

Similar to all other status bits in the ANALOG_DIAG_RESULTS register, assuming that the error condition is subsided, these bits are sticky, and a 1 must be written to the bits to clear the bits. If the error condition is still present, the flag remains high even after a 1 is written to clear the flag.

Table 14. Comparator Supply Activation Thresholds

Supply	Lower Threshold (V)	Nominal Value/Range (V)	Upper Threshold (V)
INT_AVCC	3.8	4 to 5	5.2
VLDO	2.8	3 to 3.6	3.8
REFIN	2.24	2.5	2.83
REFOUT	2.24	2.5	2.83

OUTPUT FAULT

The AD5413 has a $\overline{\text{FAULT}}$ pin that is an active low, pseudo open-drain output that connects several AD5413 devices together to one pull-up resistor for global fault detection. This pin is high impedance when no faults are detected and is asserted low when certain faults, such as an open circuit in current mode, a short circuit in voltage mode, a CRC error, or an overtemperature error, are detected. Table 15 shows the fault conditions that automatically force the $\overline{\text{FAULT}}$ pin active and shows the user maskable fault bits available via the FAULT_PIN_CONFIG register (see Table 34). All registers contain a corresponding $\overline{\text{FAULT}}$ pin status bit, FAULT_PIN_STATUS, that mirrors the inverted current state of the $\overline{\text{FAULT}}$ pin.

The DIG_DIAG_STATUS bit and ANA_DIAG_STATUS bit of the status register are used in conjunction with the $\overline{\text{FAULT}}$ pin and the FAULT_PIN_STATUS bit to inform the user which fault condition is causing either the $\overline{\text{FAULT}}$ pin or a FAULT_PIN_STATUS bit to activate.

Table 15. $\overline{\text{FAULT}}$ Pin Trigger Sources.

Fault Type	Mapped to $\overline{\text{FAULT}}$ Pin	Mask Ability
Digital Diagnostic Faults		
Oscillator Stop Detect	Yes	Yes
Calibration Memory Not Refreshed	No	N/A[1]
Reset Detected	No	N/A[1]
DAC Latch Monitor Error	Yes	Yes
Inverse DAC Check Error	Yes	Yes
Calibration Memory CRC Error	Yes	No
Invalid SPI Access	Yes	Yes
SCLK Count Error[2]	Yes	No
Slip Bit Error	Yes	Yes
SPI CRC Error	Yes	Yes
Analog Diagnostic Faults		
Current Output Open-Circuit Error	Yes	Yes
Voltage Output Short-Circuit Error	Yes	Yes
Die Temperature Error	Yes	Yes
REFOUT Comparator Error	Yes	No
REFIN Comparator Error	Yes	No
INT_AVCC Comparator Error	Yes	No
V_{LDO} Comparator Error	Yes	No

[1] Not applicable.
[2] The SCLK count error cannot be masked in the $\overline{\text{FAULT}}$_PIN_CONFIG register. However, the error can be excluded from the $\overline{\text{FAULT}}$ pin by enabling the SPI_DIAG_QUIET_EN bit (Bit 3) in the GP_CONFIG1 register.

AD5413 REGISTERS

The AD5413 is controlled and configured via the 20 on-chip registers described in the Register Map section. Possible access permissions include the following:

- R/W is read or write.
- R is read only.
- R/W-1-C is read or write 1 to clear.
- R0/W is read zero or write.

Reading from or writing to reserved registers is flagged as an invalid SPI access (see Table 36). When accessing registers with reserved bit fields, the default value of those bit fields must be written. These values are listed in the reset column of Table 22 to Table 41.

WRITING TO REGISTERS

Use the format data frame in Table 16 when writing to any register. By default, the SPI CRC is enabled, and the input register is 32 bits wide with the last 8 bits corresponding to the CRC code. Only frames that are exactly 32 bits wide are accepted as valid. If the CRC is disabled, the input register is 24 bits wide, and 32-bit frames are also accepted with the final 8 bits ignored. Table 17 describes the bit names and functions of Bits[D23:D16]. Bits[D15:D0] depend on the register that is being addressed.

READING FROM REGISTERS

The AD5413 options for readback modes that can be configured in the TWO_STAGE_READBACK_SELECT register (see Table 35) include the following:

- Two-stage readback
- Autostatus readback
- Shared $\overline{\text{SYNC}}$ autostatus readback
- Echo mode

Two-Stage Readback Mode

Two-stage readback mode consists of a write to the TWO_STAGE_READBACK_SELECT register to select the register location to be read back, followed by an NOP command. To perform an NOP command, write all 0s to Bits[D15:D0] of the NOP register. During the NOP command, the contents of the selected register are available on the SDO pin in the data frame format shown in Table 18. The user can also write a new two-stage readback command during the second frame, such that the corresponding new data is available on the SDO pin in the subsequent frame (see Figure 66). Bits[D31:D30] (or Bits[D23:D22] if SPI CRC is not enabled) = 0b10 and are used as part of the synchronization during readback. The contents of the first write instruction to the TWO_STAGE_READBACK_SELECT register are shown in Table 19.

Autostatus Readback Mode

When autostatus readback mode is selected, the contents of the status register are available on the SDO line during each SPI transaction. When reading back the status register, the SDO contents differ from the data frame format shown in Table 18. The contents of the status register are shown in Table 20. Refer to the example shown in Figure 67.

Configure the autostatus readback mode via the READBACK_MODE bits in the TWO_STAGE_READBACK_SELECT register (see the Two-Stage Readback Select Register section).

Shared $\overline{\text{SYNC}}$ Autostatus Readback Mode

The shared $\overline{\text{SYNC}}$ autostatus readback mode is a unique version of the autostatus readback mode used to avoid SDO bus contention when multiple AD5413 devices share the same $\overline{\text{SYNC}}$ line. If this issue occurs, the AD5413 devices are distinguished from each other using the hardware address pins, AD0 and AD1. An internal flag is set after each valid write to a device and the flag is cleared on the subsequent falling edge of $\overline{\text{SYNC}}$. The shared $\overline{\text{SYNC}}$ autostatus readback mode behaves in a similar manner to the normal autostatus readback mode, except the device does not output the status register contents on SDO when $\overline{\text{SYNC}}$ goes low unless the internal flag is set, which occurs when the previous SPI write is valid. Refer to the example shown in Figure 68.

Echo Mode

Echo mode behaves in a similar manner to the autostatus readback mode, except that every second readback consists of an echo of the previous command written to the AD5413. Echo mode is useful for checking which SPI instruction is received in the previous SPI frame. Refer to the example shown in Figure 69.

Table 16. Writing to a Register

MSB								LSB
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**[D15:D0]**
$\overline{\text{AD1}}$	AD1	AD0	REG_ADR4	REG_ADR3	REG_ADR2	REG_ADR1	REG_ADR0	Data

Table 17. Input Register Decode

Bit	Description
$\overline{\text{AD1}}$	Slip Bit. This bit must equal the inverse of Bit D22 (the AD1 pin).
AD1, AD0	These bits are used in association with the external pins, AD1 and AD0, to determine which AD5413 device is being addressed by the system controller. Up to four unique devices can be addressed corresponding to the AD1 and AD0 addresses of 0b00, 0b01, 0b10, and 0b11.
REG_ADR4, REG_ADR3, REG_ADR2, REG_ADR1, REG_ADR0	These bits select which register is written to. See Table 21 for a summary of the available registers.

Table 18. SDO Contents for Read Operation

MSB			LSB
[D23:D22]	**D21**	**[D20:16]**	**[D15:D0]**
0b10	$\overline{\text{FAULT}}$ pin status	Register address	Data

Table 19. Reading from a Register Using Two-Stage Readback Mode

MSB													LSB
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**[D15:D5]**	**D4**	**D3**	**D2**	**D1**	**D0**
$\overline{\text{AD1}}$	AD1	AD0	0x13					Reserved	READBACK_SELECT[4:0]				

Table 20. SDO Contents for a Read Operation on the Status Register

MSB					LSB
D23	**D22**	**D21**	**D20**	**D19**	**[D18:D0]**
1	0	FAULT_PIN_STATUS	DIG_DIAG_STATUS	ANA_DIAG_STATUS	Reserved

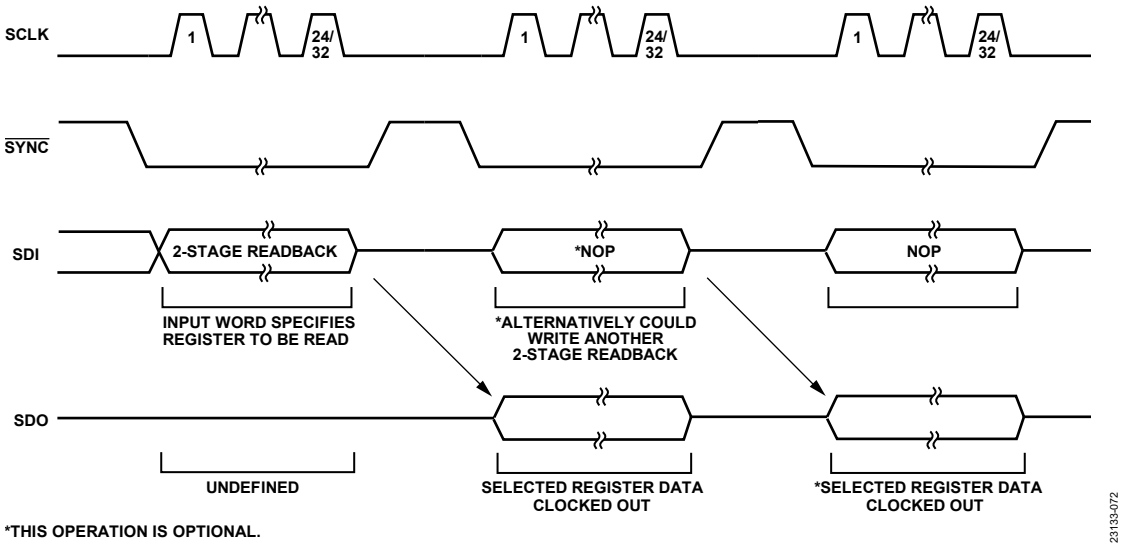


Figure 66. Two-Stage Readback Example

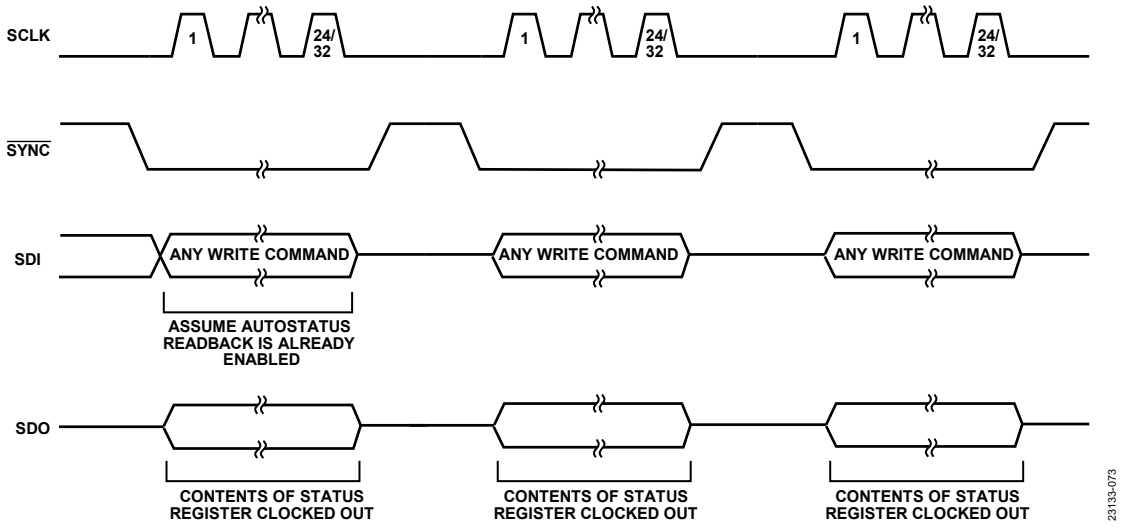


Figure 67. Autostatus Readback Example

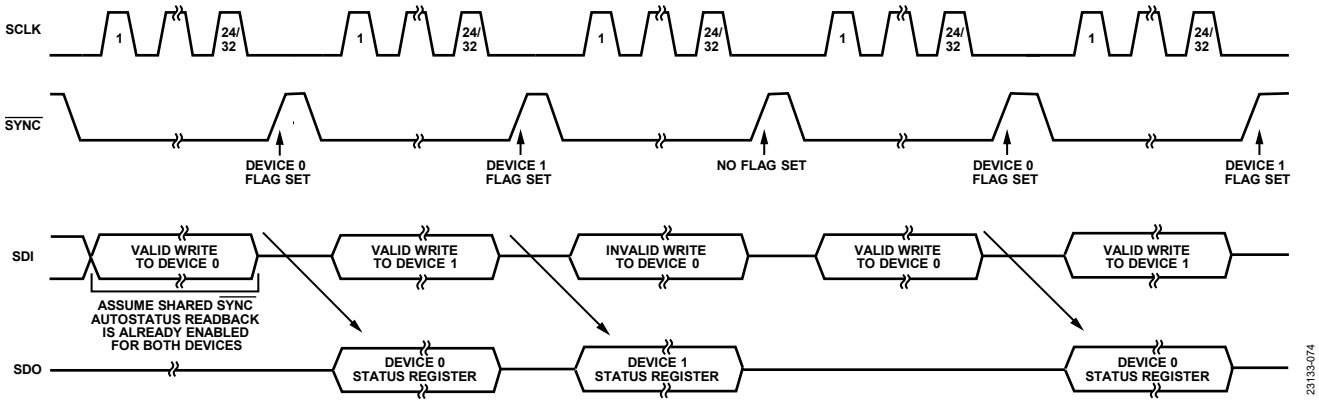


Figure 68. Shared $\overline{SYNC}$ Autostatus Readback Example

Figure 69. SDO Contents in Echo Mode

PROGRAMMING SEQUENCE TO ENABLE THE OUTPUT

To write to and set up the AD5413 device from a power-on or reset condition, take the following steps:

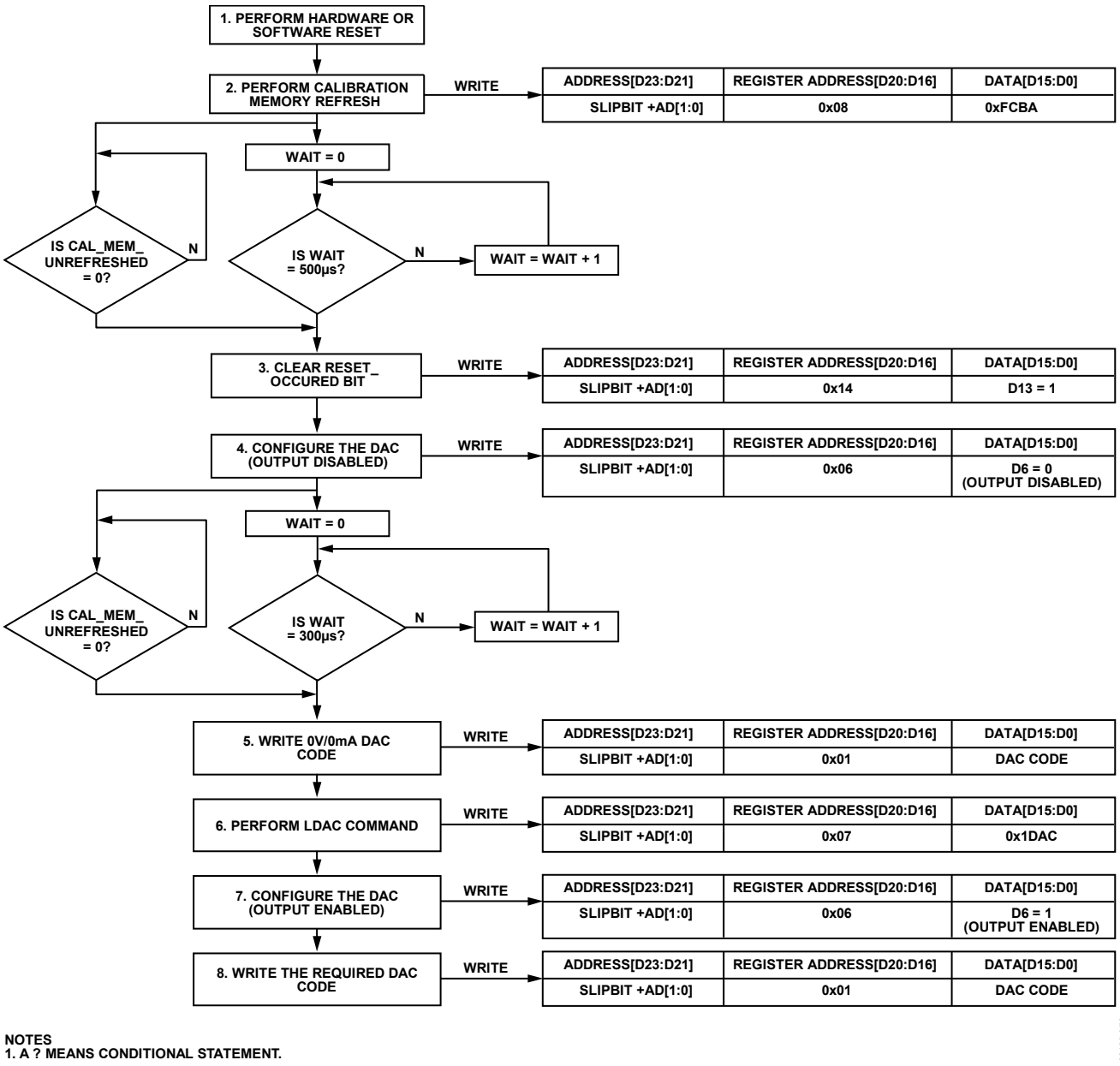
1. Perform either a hardware or software reset and wait 100 µs.
2. Write 0xFCBA to the key register to perform a calibration memory refresh. Wait a minimum of 500 µs before proceeding to Step 3 to allow time for the internal calibrations to complete or poll the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register until the bit reads 0.
3. Write 1 to Bit 13 in the DIGITAL_DIAG_RESULTS register to clear the RESET_OCCURRED flag.
4. Write to the DAC_CONFIG register to set the INT_EN bit, which powers up the DAC and internal amplifiers without enabling the channel output, and configure the output range, internal or external R_{SET}, and slew rate. Keep the OUT_EN bit disabled at this point. Wait a minimum of 500 µs before proceeding to Step 6 to allow the internal calibrations to complete or poll the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register until the bit reads 0.
5. Write a zero-scale DAC code to the DAC_INPUT register. If the voltage mode is to be selected in Step 7, write a DAC code that represents a 0 V output to the DAC_INPUT register. Ensure that this step is completed even if the contents of the DAC_INPUT register are not changing.
6. If the LDAC command functionality is used, perform either a software or hardware LDAC command.
7. Rewrite the same word used in Step 4 to the DAC_CONFIG register but keep the OUT_EN bit enabled.
8. Write the required DAC code to the DAC_INPUT register.

An example configuration for this setup is shown in Figure 70.

Changing and Reprogramming the Range

When the output is enabled, take the following steps to change the output range:

1. Write to the DAC_INPUT register. Set the output to 0 mA or 0 V.
2. Write to the DAC_CONFIG register. Disable the output (OUT_EN = 0) and set the new output range. Keep the INT_EN bit set. Wait a minimum or 500 µs before proceeding to Step 3 to allow time for internal calibrations to complete.
3. Write Code 0x000, or Code 0x8000 in the case of voltage output mode, to the DAC_INPUT register. Ensure that this step is completed even if the contents of the DAC_INPUT register do not change.
4. Reload the DAC_CONFIG register word from Step 2 and set the OUT_EN bit to 1 to enable the output.
5. Write the required DAC code to the DAC_INPUT register.



NOTES
1. A ? MEANS CONDITIONAL STATEMENT.

Figure 70. Example Configuration to Correctly Enable the Output (CRC Disabled for Simplicity)

REGISTER MAP

Table 21. Register Summary

Address	Name	Description	Reset	Access
0x00	NOP	NOP register	0x000000	R0/W
0x01	DAC_INPUT	DAC input register	0x010000	R/W
0x02	DAC_OUTPUT	DAC output register	0x020000	R
0x03	CLEAR_CODE	Clear code register	0x030000	R/W
0x04	USER_GAIN	User gain register	0x04FFFC	R/W
0x05	USER_OFFSET	User offset register	0x058000	R/W
0x06	DAC_CONFIG	DAC configuration register	0x060C00	R/W
0x07	SW_LDAC	Software LDAC register	0x070000	R0/W
0x08	KEY	Key register	0x080000	R0/W
0x09	GP_CONFIG1	General-Purpose Configuration 1 register	0x090204	R/W
0x0A	GP_CONFIG2	General-Purpose Configuration 2 register	0x0A0200	R/W
0x0B	RESERVED	Reserved	0x0B0000	R/W
0x0C	RESERVED	Reserved	0x0C0100	R/W
0x0D	RESERVED	Reserved	0x0D0000	R/W
0x0E	RESERVED	Reserved	0x0E0000	R/W
0x0F	RESERVED	Reserved	0x0F0009	R/W
0x10	DIGITAL_DIAG_CONFIG	Digital diagnostic configuration register	0x10005D	R/W
0x11	RESERVED	Reserved	0x110000	R/W
0x12	FAULT_PIN_CONFIG	$\overline{\text{FAULT}}$ pin configuration register	0x120000	R/W
0x13	TWO_STAGE_READBACK_SELECT	Two-stage readback select register	0x130000	R/W
0x14	DIGITAL_DIAG_RESULTS	Digital diagnostic results register	0x14A000	R/W-1-C
0x15	ANALOG_DIAG_RESULTS	Analog diagnostic results register	0x150000	R/W-1-C
0x16	STATUS	Status register	0x160000	R
0x17	CHIP_ID	Chip ID register	0x170101	R
0x18	FREQ_MONITOR	Frequency monitor register	0x180000	R
0x19	RESERVED	Reserved	0x190000	R
0x1A	RESERVED	Reserved	0x1A0000	R
0x1B	RESERVED	Reserved	0x1B0000	R
0x1C	DEVICE_ID_3	Generic ID register	0x1C0000	R

REGISTER DETAILS

NOP Register

Address: 0x00, Reset: 0x000000, Name: NOP

Write 0x0000 to Bits[15: 0] at this address to perform an NOP command. Bits[15:0] of the NOP register always read back as 0x0000.

Table 22. Bit Descriptions for NOP

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:0]	NOP command	Write 0x0000 to these bits to perform an NOP command.	0x0	R0/W

DAC Input Register

Address: 0x01, Reset: 0x010000, Name: DAC_INPUT

Bits[15:2] consist of the 14-bit data to be written to the DAC. If the $\overline{\text{LDAC}}$ pin is tied low (active), the DAC_INPUT register contents are written directly to the DAC_OUTPUT register without any $\overline{\text{LDAC}}$ functionality dependence. If the $\overline{\text{LDAC}}$ pin is tied high, the contents of the DAC_INPUT register are written to the DAC_OUTPUT register when the $\overline{\text{LDAC}}$ pin is brought low or when the software $\overline{\text{LDAC}}$ command is written.

Table 23. Bit Descriptions for DAC_INPUT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:2]	DAC_INPUT_DATA	DAC Input Data.	0x0	R/W
[1:0]	RESERVED	Do not write to these bits.	0x0	R/W

DAC Output Register

Address: 0x02, Reset: 0x020000, Name: DAC_OUTPUT

The DAC_OUTPUT register is a read only register and contains the latest calibrated 14-bit DAC output value.

Table 24. Bit Descriptions for DAC_OUTPUT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:2]	DAC_OUTPUT_DATA	DAC Output Data. For example, the last calibrated 14-bit DAC output value.	0x0	R
[1:0]	RESERVED	Do not write to these bits.	0x0	R/W

Clear Code Register

Address: 0x03, Reset: 0x030000, Name: CLEAR_CODE

When writing to the CLEAR_CODE register, Bits[15:2] consist of the clear code that clears the DAC when a clear event occurs. When a clear event is complete, write to the DAC_INPUT register with the 14-bit data to be written to the DAC, even if the data is the same data as previously written before the clear event. Performing an LDAC write to the hardware or software does not update the DAC_OUTPUT register to a new code until the DAC_INPUT register is written to first.

Table 25. Bit Descriptions for CLEAR_CODE

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:2]	CLEAR_CODE	Clear Code. The DAC clears to this code upon a clear event.	0x0	R/W
[1:0]	RESERVED	Do not write to these bits.	0x0	R/W

User Gain Register

Address: 0x04, Reset: 0x04FFFC, Name: USER_GAIN

The 14 USER_GAIN bits allow the user to adjust the gain of the DAC channel in steps of 1 LSB. The USER_GAIN register coding is straight binary. The default code is 0xFFFC. Theoretically, the gain can be tuned across the full range of the output. However, the maximum recommended gain trim is approximately 50% of the programmed range to maintain accuracy.

Table 26. Bit Descriptions for USER_GAIN

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:2]	USER_GAIN	User Gain Correction Code.	0x3FFF	R/W
[1:0]	RESERVED	Do not write to these bits.	0x0	R/W

User Offset Register

Address: 0x05, Reset: 0x058000, Name: USER_OFFSET

The USER_OFFSET register allows the user to adjust the DAC channel offset by −8192 LSBs to +8192 LSBs in steps of 1 LSB. The USER_OFFSET register coding is straight binary. The default code is 0x8000, which results in zero offset programmed to the output.

Table 27. Bit Descriptions for USER_OFFSET

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:2]	USER_OFFSET	User Offset Correction Code.	0x2000	R/W
[1:0]	RESERVED	Do not write to these bits.	0x0	R/W

DAC Configuration Register

Address: 0x06, Reset: 0x060C00, Name: DAC_CONFIG

The DAC_CONFIG register configures the DAC (range, internal or external R_{SET}, and output enable), enables the output stage circuitry, and configures the slew rate control function.

Table 28. Bit Descriptions for DAC_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:13]	SR_STEP	Slew Rate Step. In conjunction with the slew rate clock, the slew rate step defines how much the output value changes at each update. Together, both parameters define the rate of change of the output value. 000: 4 LSB (default). 001: 12 LSB. 010: 64 LSB. 011: 120 LSB. 100: 256 LSB. 101: 500 LSB. 110: 1820 LSB. 111: 2048 LSB.	0x0	R/W
[12:9]	SR_CLOCK	Slew Rate Clock. The slew rate clock defines the rate at which the digital slew is updated. 0000: 240 kHz. 0001: 200 kHz. 0010: 150 kHz. 0011: 128 kHz. 0100: 64 kHz. 0101: 32 kHz. 0110: 16 kHz (default).	0x6	R/W

Bits	Bit Name	Description	Reset	Access
		0111: 8 kHz. 1000: 4 kHz. 1001: 2 kHz. 1010: 1 kHz. 1011: 512 Hz. 1100: 256 Hz. 1101: 128 Hz. 1110: 64 Hz. 1111: 16 Hz.		
8	SR_EN	Slew Rate Control Enable. 0: disable (default). 1: enable.	0x0	R/W
7	RSET_EXT_EN	External Current Setting Resistor Enable. 0: select internal R_{SET} resistor (default). 1: select external R_{SET} resistor.	0x0	R/W
6	OUT_EN	VI_{OUT} Enable. 0: disable VI_{OUT} output (default). 1: enable VI_{OUT} output.	0x0	R/W
5	INT_EN	Internal Buffers Enable. Set this bit to power up the DAC and internal amplifiers. Setting this bit does not enable the output. Set this bit and allow a >200 µs delay before enabling the output. This delay results in a reduced output enable glitch. 0: disable (default). 1: enable.	0x0	R/W
4	OVRNG_EN	20% of 10.5 V Voltage Overrange Enable. 0: disable (default). 1: enable.	0x0	R/W
[3:0]	RANGE	Select Output Range. Changing the contents of these bits initiates an internal calibration memory refresh and, therefore, a subsequent SPI write must not be performed until the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register returns to 0. Writes to reserved Bits[3:0] codes are ignored. 0000: reserved. Do not write to these bits. 0001: reserved. Do not write to these bits. 0010: reserved. Do not write to these bits. 0011: ±10.5 V voltage range. 1000: reserved. Do not write to these bits. 1001: 0 mA to 24 mA current range. 1010: reserved. Do not write to these bits. 1011: reserved. Do not write to these bits. 1100: reserved. Do not write to these bits. 1101: reserved. Do not write to these bits.	0x0	R/W

Software LDAC Register

Address: 0x07, Reset: 0x070000, Name: SW_LDAC

Write 0x1DAC to the SW_LDAC register to perform a software LDAC mode update on the device that matches the address bits within the SPI frame. If the GLOBAL_SW_LDAC bit in the GP_CONFIG2 register is set, Bit 21 and Bit 22 are ignored and all devices sharing the same SPI bus are updated via the SW_LDAC command. Bits[15:0] of this register always read back as 0x0000.

Table 29. Bit Descriptions for SW_LDAC

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:0]	LDAC_COMMAND	Software LDAC Command. Write 0x1DAC to this register to perform a software LDAC instruction.	0x0	R0/W

Key Register

Address: 0x08, Reset: 0x080000, Name: KEY

The KEY register accepts specific key codes to perform tasks such as calibration memory refresh and software reset. Bits[15:0] of this register always read back as 0x0000. All unlisted key codes are reserved.

Table 30. Bit Descriptions for KEY

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:0]	KEY_CODE	Key Code. 0x15FA: first of two keys to initiate a software reset. 0xAF51: second of two keys to initiate a software reset. 0xFCBA: key to initiate a calibration memory refresh to the shadow registers. This key is only valid the first time it is run and has no effect if subsequent writes occur within a given system reset cycle.	0x0	R0/W

General-Purpose Configuration 1 Register

Address: 0x09, Reset: 0x090204, Name: GP_CONFIG1

The GP_CONFIG1 register configures functions such as the temperature comparator threshold and enables other miscellaneous features.

Table 31. Bit Descriptions for GP_CONFIG1

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:14]	RESERVED	Reserved.	0x0	R
[13:12]	SET_TEMP_THRESHOLD	Temperature Comparator Threshold Value Setting. 00: 142°C (default). 01: 127°C. 10: 112°C. 11: 97°C.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R/W
[9:7]	RESERVED	Reserved.	0x4	R/W
6	HART_EN	Path to C_{HART} Pin Enable. 0: DAC output drives the output stage directly (default). 1: C_{HART} path is coupled to the DAC output to allow a HART modem connection or a slew capacitor connection of a slew capacitor.	0x0	R/W
5	RESERVED	Reserved.	0x0	R/W
4	CLEAR_NOW_EN	Enables the clear code to update the DAC immediately, even if the output slew feature is currently enabled. 0: disable (default). 1: enable.	0x0	R/W
3	SPI_DIAG_QUIET_EN	SPI Diagnostic Quiet Mode Enable. When this bit is enabled, the SPI_CRC_ERR, SLIPBIT_ERR, and SCLK_COUNT_ERR bits are not included in the logical OR calculation, which creates the DIG_DIAG_STATUS bit in the status register. These bits are also masked from affecting the $\overline{\text{FAULT}}$ pin if this bit is set. 0: disable (default). 1: enable.	0x0	R/W
2	OSC_STOP_DETECT_EN	Enables automatic 0x07DEAD code on SDO if the MCLK stops. 0: disable. 1: enable (default).	0x1	R/W
1	RESERVED	Reserved.	0x0	R/W
0	VIOUT_PULLDOWN_EN	VI_{OUT} 30 kΩ Pull-Down Resistor to AGND Enable. 0: disable (default). 1: enable.	0x0	R/W

General-Purpose Configuration 2 Register

Address: 0x0A, Reset: 0x0A0200, Name: GP_CONFIG2

The GP_CONFIG2 register configures and enables functions such as the voltage comparators and the global software LDAC command.

Table 32. Bit Descriptions for GP_CONFIG2

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
15	RESERVED	Reserved.	0x0	R0
[14:13]	COMPARATOR_CONFIG	These pins enable or disable the voltage comparator inputs for test purposes. The temperature comparator is permanently enabled (see the Background Supply and Temperature Monitoring section). 00: disables voltage comparators (default). 01: reserved. 10: reserved. 11: enables voltage comparators. Set the INT_EN bit in the DAC_CONFIG register to power up the REFIN buffer and make the REFIN buffer available to the REFIN comparator.	0x0	R/W
12	RESERVED	Reserved.	0x0	R/W
11	RESERVED	Reserved.	0x0	R/W
10	GLOBAL_SW_LDAC	When enabled, the AD5413 address bits are ignored when performing a software LDAC command, which allows multiple devices to be simultaneously updated using one SW_LDAC command. 0: disable (default). 1: enable.	0x0	R/W
9	FAULT_TIMEOUT	Reduced Fault Detect Timeout Enable. This bit configures the delay from when the analog block indicates that a V_{IOUT} fault has been detected to the associated change of the relevant bit in the ANALOG_DIAG_RESULTS register. This feature provides flexibility to accommodate different output load values. 0: fault detect timeout 25 ms. 1: fault detect timeout 6.5 ms (default).	0x1	R/W
[8:0]	RESERVED	Reserved.	0x0	R/W

Digital Diagnostic Configuration Register

Address: 0x10, Reset: 0x10005D, Name: DIGITAL_DIAG_CONFIG

The DIGITAL_DIAG_CONFIG register configures various digital diagnostic features of interest for a particular application.

Table 33. Bit Descriptions for DIGITAL_DIAG_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:7]	RESERVED	Reserved.	0x0	R0
6	DAC_LATCH_MON_EN	Diagnostic Monitor on DAC Latches Enable. This feature monitors the actual digital code driving the DAC and compares the code with the digital code generated within the digital block. Any difference between the two codes causes the DAC_LATCH_MON_ERR flag bit to be set in the DIGITAL_DIAG_RESULTS register. 0: disable. 1: enable (default).	0x1	R/W
5	RESERVED	Reserved.	0x0	R/W
4	INVERSE_DAC_CHECK_EN	Check for DAC Code vs. Inverse DAC Code Error Enable. 0: disable. 1: enable (default).	0x1	R/W
3	CAL_MEM_CRC_EN	CRC of Calibration Memory on Calibration Memory Refresh Enable. 0: disable. 1: enable (default).	0x1	R/W

Bits	Bit Name	Description	Reset	Access
2	FREQ_MON_EN	Internal Frequency Monitor on MCLK Enable. 0: disable. 1: enable (default).	0x1	R/W
1	RESERVED	Reserved.	0x0	R/W
0	SPI_CRC_EN	SPI CRC Function Enable. 0: disable. 1: enable (default).	0x1	R/W

$\overline{\text{FAULT}}$ Pin Configuration Register

Address: 0x12, Reset: 0x120000, Name: FAULT_PIN_CONFIG

The FAULT_PIN_CONFIG register is used to mask particular fault bits from the $\overline{\text{FAULT}}$ pin, if so desired.

Table 34. Bit Descriptions for FAULT_PIN_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
15	INVALID_SPI_ACCESS_ERR	If this bit is set, do not map the invalid SPI access fault flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
14	RESERVED	Reserved.	0x0	R/W
13	RESERVED	Reserved.	0x0	R/W
12	INVERSE_DAC_CHECK_ERR	If this bit is set, do not map the inverse DAC check error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
11	RESERVED	Reserved.	0x0	R/W
10	OSCILLATOR_STOP_DETECT	If this bit is set, do not map the oscillator stop detect fault to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
9	DAC_LATCH_MON_ERR	If this bit is set, do not map the DAC latch monitor error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
8	RESERVED	Reserved.	0x0	R/W
7	SLIPBIT_ERR	If this bit is set, do not map the slip bit error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
6	SPI_CRC_ERR	If this bit is set, do not map the SPI CRC error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R/W
3	IOUT_OC_ERR	If this bit is set, do not map the current output open-circuit error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
2	VOUT_SC_ERR	If this bit is set, do not map the voltage output short-circuit error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
1	RESERVED	Reserved.	0x0	R/W
0	DIE_TEMP_ERR	If this bit is set, do not map the die temperature error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W

Two-Stage Readback Select Register

Address: 0x13, Reset: 0x130000, Name: TWO_STAGE_READBACK_SELECT

The TWO_STAGE_READBACK_SELECT register selects the address of the register required for a two-stage readback operation. The address of the register selected for readback is stored in Bits[4:0].

Table 35. Bit Descriptions for TWO_STAGE_READBACK_SELECT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:7]	RESERVED	Reserved.	0x0	R
[6:5]	READBACK_MODE	SPI Readback Mode Control Bits. 0: two-stage SPI readback mode (default). 01: autostatus readback mode. The status register contents are shifted out on SDO for each SPI frame. 10: shared $\overline{\text{SYNC}}$ autostatus readback mode. This mode allows the use of a shared $\overline{\text{SYNC}}$ line on multiple devices (distinguished using the hardware address pins). After each valid write to a device, a flag is set. This mode behaves similarly to the normal autostatus readback mode, except the device does not output the status register contents on SDO as $\overline{\text{SYNC}}$ goes low, unless the internal flag is set (that is, the previous SPI write is valid).	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		11: the status register contents and the previous SPI frame instruction are alternately available on SDO.		
[4:0]	READBACK_SELECT	Select Readback Address for a Two-Stage Readback. 0x00: NOP register (default). 0x01: DAC_INPUT register. 0x02: DAC_OUTPUT register. 0x03: CLEAR_CODE register. 0x04: USER_GAIN register. 0x05: USER_OFFSET register. 0x06: DAC_CONFIG register. 0x07: SW_LDAC register. 0x08: KEY register. 0x09: GP_CONFIG1 register. 0x0A: GP_CONFIG2 register. 0x0B: reserved (do not select this option). 0x0C: reserved (do not select this option). 0x0D: reserved (do not select this option). 0x0E: reserved (do not select this option). 0x0F: reserved (do not select this option). 0x10: DIGITAL_DIAG_CONFIG register. 0x11: reserved (do not select this option). 0x12: FAULT_PIN_CONFIG register. 0x13: TWO_STAGE_READBACK_SELECT register. 0x14: DIGITAL_DIAG_RESULTS register. 0x15: ANALOG_DIAG_RESULTS register. 0x16: STATUS register. 0x17: CHIP_ID register. 0x18: FREQ_MONITOR register. 0x19: reserved (do not select this option). 0x1A: reserved (do not select this option). 0x1B: reserved (do not select this option). 0x1C: DEVICE_ID_3 register.	0x0	R/W

Digital Diagnostic Results Register

Address: 0x14, Reset: 0x14A000, Name: DIGITAL_DIAG_RESULTS

The DIGITAL_DIAG_RESULTS register contains an error flag for the on-chip digital diagnostic features, most of which are configurable using the digital diagnostic configuration register. This register also contains a flag to indicate that a reset occurred, as well as a flag to indicate that the calibration memory has not refreshed or that an invalid SPI access was attempted. With the exception of the CAL_MEM_UNREFRESHED and SLEW_BUSY flags, a 1 must be written to all flags to update to the current value. The CAL_MEM_UNREFRESHED and SLEW_BUSY flags automatically clear when the calibration memory refresh or output slew, respectively, is complete. When the corresponding enable bits in the DIGITAL_DIAG_CONFIG register are not enabled, the respective flag bits read as zero.

Table 36. Bit Descriptions for DIGITAL_DIAG_RESULTS

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
15	CAL_MEM_UNREFRESHED	Calibration Memory Unrefreshed Flag. Modifying the RANGE bits in the DAC_CONFIG register initiates a calibration memory refresh that asserts this bit. Unlike the R/W-1-C bits in this register, this bit automatically clears when the calibration memory refresh completes. 0: calibration memory refreshes. 1: calibration memory is unrefreshed (default on power-up). This bit asserts if the RANGE bits are modified in the DAC_CONFIG register.	0x1	R

Bits	Bit Name	Description	Reset	Access
14	SLEW_BUSY	This flag is set to 1 when the DAC is actively slewing. Unlike the R/W-1-C bits in this register, this bit automatically clears when slewing completes.	0x0	R
13	RESET_OCCURRED	This bit flags that a reset occurred (default on power-up is Logic 1).	0x1	R/W-1-C
12	RESERVED	Reserved.	0x0	R/W-1-C
11	RESERVED	Reserved.	0x0	R/W-1-C
[10:9]	RESERVED	Reserved.	0x0	R/W-1-C
8	DAC_LATCH_MON_ERR	This bit flags if the output of the DAC latch does not match the input.	0x0	R/W-1-C
7	RESERVED	Reserved.	0x0	R/W-1-C
6	INVERSE_DAC_CHECK_ERR	This bit flags if a fault is detected between the DAC code driven by the digital core and an inverted copy.	0x0	R/W-1-C
5	CAL_MEM_CRC_ERR	This bit flags a CRC error for the CRC calculation of the calibration memory upon refresh.	0x0	R/W-1-C
4	INVALID_SPI_ACCESS_ERR	This bit flags if an invalid SPI access is attempted, such as writing to or reading from an invalid or reserved address. This bit also flags if an SPI write is attempted directly after powering up but before a calibration memory refresh is performed, or if an SPI write is attempted while a calibration memory refresh is in progress. Performing a two-stage readback is permitted during a calibration memory refresh and does not cause this flag to set. Attempting to write to a read only register also causes this bit to assert.	0x0	R/W-1-C
3	RESERVED	Reserved.	0x0	R/W-1-C
2	SCLK_COUNT_ERR	This bit flags an SCLK falling edge count error. If the SPI CRC is enabled, 32 clocks are required. If the SPI CRC is not enabled, either 24 clocks or 32 clocks are required.	0x0	R/W-1-C
1	SLIPBIT_ERR	This bit flags an SPI frame slip bit error, which is when the MSB of the SPI word is not equal to the inverse of MSB − 1.	0x0	R/W-1-C
0	SPI_CRC_ERR	This bit flags an SPI CRC error.	0x0	R/W-1-C

Analog Diagnostic Results Register

Address: 0x15, Reset: 0x150000, Name: ANALOG_DIAG_RESULTS

The ANALOG_DIAG_RESULTS register contains an error flag corresponding to the four voltage nodes (VLDO, INT_AVCC, REFIN, and REFOUT) monitored in the background by comparators, as well as a flag for the die temperature, which is also monitored by comparators. The voltage output short circuit and current output open circuit are contained in this register. Similar to the DIGITAL_DIAG_RESULTS register, a 1 must be written to all flags in this register to update or clear the flags. When the corresponding diagnostic features are not enabled, the respective error flags read zero.

Table 37. Bit Descriptions for ANALOG_DIAG_RESULTS

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:8]	RESERVED	Reserved.	0x0	R0
7	IOUT_OC_ERR	This bit flags a current output open-circuit error. This error bit is set in the case of a current output open circuit and cases where there is insufficient headroom available to the internal current output driver circuitry to provide the programmed output current.	0x0	R/W-1-C
6	VOUT_SC_ERR	This bit flags a voltage output short-circuit error.	0x0	R/W-1-C
5	RESERVED	Reserved.	0x0	R0
4	DIE_TEMP_ERR	This bit flags an overtemperature error for the die.	0x0	R/W-1-C
3	REFOUT_ERR	This bit flags that the REFOUT node is outside of the comparator threshold levels or if the short-circuit current limit occurs.	0x0	R/W-1-C
2	REFIN_ERR	This bit flags that the REFIN node is outside of the comparator threshold levels.	0x0	R/W-1-C
1	INT_AVCC_ERR	This bit flags that the INT_AVCC node is outside of the comparator threshold levels.	0x0	R/W-1-C
0	VLDO_ERR	This bit flags that the VLDO node is outside of the comparator threshold levels or if the short-circuit current limit occurs.	0x0	R/W-1-C

Status Register

Address: 0x16, Reset: 0x160000, Name: STATUS

The STAUS register contains status bits, as well as the, OR'd analog and digital diagnostics and the $\overline{\text{FAULT}}$ pin status bits.

Table 38. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
20	DIG_DIAG_STATUS	This bit represents the result of a logical OR of the contents of Bits[15:0] in the DIGITAL_DIAG_RESULTS register (except for the SLEW_BUSY bit). If any of these bits are high, the DIG_DIAG_STATUS bit is high. Note that this bit is high on power-up because of the active RESET_OCCURRED flag bit. A quiet mode is also available (SPI_DIAG_QUIET_EN in the GP_CONFIG1 register), in which the logical OR function only incorporates Bits[15:3] of the DIGITAL_DIAG_RESULTS register (except for the SLEW_BUSY bit). If an SPI CRC, SPI slip bit, or SCLK count error occurs, the DIG_DIAG_STATUS bit is not set high.	0x1	R
19	ANA_DIAG_STATUS	This bit represents the result of a logical OR of the contents of Bits[13:0] in the ANALOG_DIAG_RESULTS register. If any bit in the ANALOG_DIAG_RESULTS register is high, the ANA_DIAG_STATUS bit is high.	0x0	R
[18:0]	RESERVED	Reserved.	0x0	R

Chip ID Register

Address: 0x17, Reset: 0x170101, Name: CHIP_ID

The CHIP_ID register contains the chip ID of the die.

Table 39. Bit Descriptions for CHIP_ID

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:11]	RESERVED	Reserved.	0x0	R0
[10:8]	RESERVED	Reserved.	0x0	R0
[7:0]	DIE_CHIP_ID	These bits reflect the revision number of the die.	0x2	R

Frequency Monitor Register

Address: 0x18, Reset: 0x180000, Name: FREQ_MONITOR

An internal frequency monitor uses the MCLK to create a pulse at a frequency of 1 kHz (MCLK/10,000). This pulse increments a 16-bit counter. The value of the counter is available to read in the FREQ_MONITOR register. The user can poll this register periodically and use it as a diagnostic tool for MCLK (to monitor whether the oscillator is running) and to measure the frequency. This feature is enabled by default via the FREQ_MON_EN bit in the DIGITAL_DIAG_CONFIG register and allows a robustness check of MCLK.

Table 40. Bit Descriptions for FREQ_MONITOR

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:0]	FREQ_MONITOR	Internal Clock Counter Value.	0x0	R

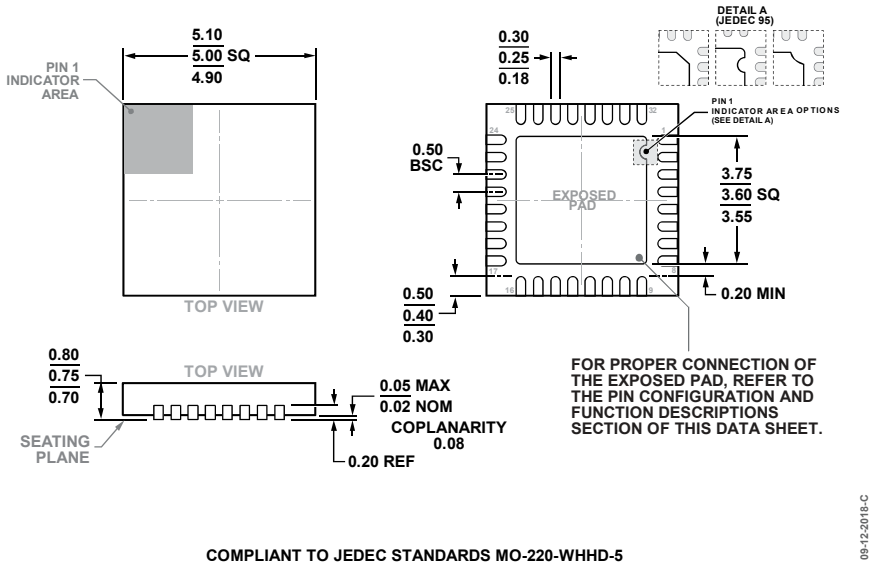
Generic ID Register

Address: 0x1C, Reset: 0x1C0000, Name: DEVICE_ID_3

Table 41. Bit Descriptions for DEVICE_ID_3

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	This bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register Address.	0x0	R
[15:8]	RESERVED	Reserved.	0x0	R
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	GENERIC_ID	Generic ID.	0x0	R
		000: reserved.	0x0	R
		001: reserved.	0x0	R
		010: reserved.	0x0	R
		011: reserved.	0x0	R
		100: reserved.	0x0	R
		101: reserved.	0x0	R
		110: reserved.	0x0	R
		111: AD5413.	0x0	R

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5

Figure 71. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5413BCPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD5413BCPZ-RL7	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
EVAL-AD5413SDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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