19-0545; Rev 0; 6/06

EVALUATION KIT AVAILABLE

12V PWM Controller with Hot-Swap

MAX5950

General Description

The MAX5950 is a 12V pulse-width modulated (PWM), step-down, DC-DC controller with integrated hot-swap controller. The device operates over the 8V to 16V input-voltage range or 5V ±10% and provides an adjustable output from 0.8V to 5.5V. The device delivers up to 10A of load current with excellent load-and-line regulation. The MAX5950 is optimized for PCIe® ExpressModule™ power-management application.

The MAX5950 features a hot-swap controller that provides inrush current control during module insertion and removal, as well as short-circuit protection during normal operation. The MAX5950 features an internal charge pump that provides the gate drive for an external n-channel MOSFET. A DCENO logic output indicates the completion of the inrush cycle.

The MAX5950 PWM section utilizes a voltage-mode control scheme for good noise immunity and offers external compensation, allowing for maximum flexibility with a wide selection of inductor values and capacitor types. The device operates at a fixed switching frequency that is programmable from 100kHz to 1MHz and can be synchronized to an external clock signal through the SYNCIN input. The device includes undervoltage lockout (UVLO) and digital soft-start. Protection features include lossless valley-mode current limit, hiccup-mode output short-circuit protection, and thermal shutdown.

The MAX5950 is available in a space-saving 5mm x 5mm, 32-pin thin QFN package and is specified for operation over the -40°C to +85°C extended temperature range. Refer to the MAX5951 data sheet for a pin-compatible, general-purpose PWM controller.

Applications

PCIe ExpressModule

General 12V-Input PWM Controllers with Hot-Swap

Blade Servers

RAID

Base Stations

Work Stations

PCIe is a registered trademark and ExpressModule is a trademark of PCI-SIG Corp.

Features

- **8V to 16V or 5V ±10% Input-Voltage Range**
- **Integrated Hot-Swap Controller**
- **Lossless Valley-Mode Current Sensing**
- **Output Voltage Adjustable from 0.8V to 5.5V**
- **Voltage-Mode Control**
- **External Compensation for Maximum Flexibility**
- **Digital Soft-Start**
- **Sequencing or Ratiometric Tracking**
- **Startup Synchronization**
- **Programmable PGOOD Output**
- **Programmable Switching Frequency from 100kHz to 1MHz**
- **External Frequency Synchronization**
- **SYNCIN and SYNCOUT Enable 180° Out-of-Phase Operation**
- **Thermal Shutdown and Short-Circuit Protection**
- **Space-Saving 5mm x 5mm, 32-Pin TQFN Package**

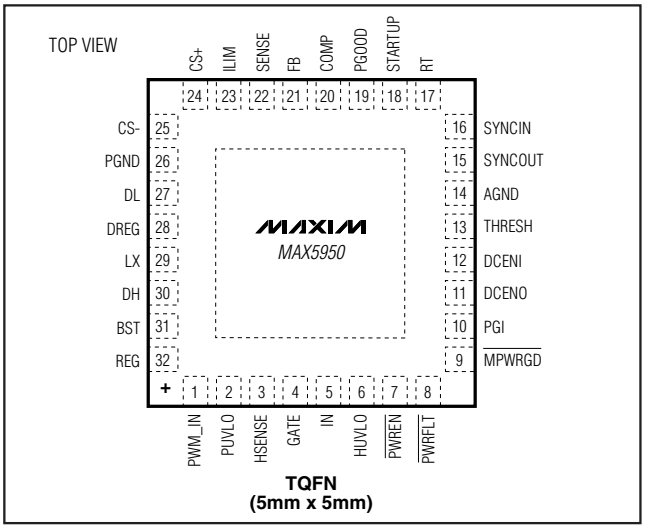
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5950ETJ+	-40°C to +85°C	32 TQFN-EP*	T3255-4

+Denotes lead-free package.

**EP = Exposed pad.*

Pin Configuration



TQFN (5mm x 5mm)

ABSOLUTE MAXIMUM RATINGS

IN to AGND .....-0.3V to +24V
HSENSE, PWM_IN to AGND .....-0.3V to (V_{IN} + 0.3V)
GATE to AGND .....-0.3V to +30V
GATE to PWM_IN .....-0.3V to +6V
PWREN, PWRFLT, MPWRGD, HUVLO, PGI, DCENO to AGND .....-0.3V to +6V
BST to AGND .....-0.3V to +30V
BST to LX .....-0.3V to +6V
CS- to AGND .....-0.3V to (V_{PWM_IN} + 0.3V)
REG, DREG, PUVLO, DCENI, SYNCIN, THRESH, SENSE to AGND .....-0.3V to +6V
RT, ILIM, STARTUP, PGOOD, FB, CS+ to AGND .....-0.3V to +6V
SYNCOUT, COMP to AGND .....-0.3V to (V_{REG} + 0.3V)
DL to PGND .....-0.3V to (V_{DREG} + 6V)
DH to LX .....-0.3V to (V_{BST} + 0.3V)
PGND to AGND .....-0.3V to +0.3V
Input Current (any pin) .....±50mA
Continuous Power Dissipation
32-Pin TQFN (derate 34.5 mW/°C above +70°C) ...2758.6mW
32-Pin TQFN (θ_{JA}) .....+29°C/W
32-Pin TQFN (θ_{JC}) .....2.1°C/W
Operating Ambient Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{PWM_IN} = 12V or V_{IN} = V_{PWM_IN} = V_{REG} = 5V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 100kΩ, R_{ILIM} = 60kΩ, C_{REG} = 2.2µF, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Voltage Range	V_{IN}		8		16	V
		V_{IN} = V_{PWM_IN} = V_{REG} = V_{DREG} (Note 2)	4.5		5.5	
Standby Supply Current		V_{IN} = 16V, V_{PWM_IN} = V_{HUVLO} = 0V		1.0	1.6	mA
Quiescent Supply Current		V_{IN} = V_{PWM_IN} = 16V, V_{FB} = 0.9V		2.3	3.7	mA
Switching Supply Current		V_{IN} = V_{PWM_IN} = 16V, V_{FB} = 0V		6	9	mA
HOT-SWAP UVLO						
Default Hot-Swap Undervoltage Lockout Threshold		V_{IN} rising	6.7		7.3	V
Hot-Swap UVLO Hysteresis				0.7		V
HUVLO Threshold	V_{HUVLO}	V_{HUVLO} rising	1.202	1.220	1.238	V
HUVLO Hysteresis				122		mV
HUVLO Input Impedance			180	310	500	kΩ
HOT-SWAP PWREN CONTROL						
PWREN Input High-Level Voltage			2			V
PWREN Input Low-Level Voltage					0.8	V
PWREN Input Hysteresis				260		mV
PWREN Input Pullup Resistance			50	100	160	kΩ
PWREN Clamp Voltage		I_{PWREN} = 1mA		4.8		V
PWREN High-to-Low Deglitch Time			6.5	10.5	15.0	ms
HOT-SWAP CIRCUIT-BREAKER COMPARATOR						
Circuit-Breaker Threshold	V_{CB}	V_{IN} - V_{HSENSE}	553	613	673	mV
HSENSE Input Bias Current		V_{HSENSE} = 12V	-1		+1	µA
HOT-SWAP GATE CONTROL						
GATE Charge Current	I_{GATE}		4	5	6	µA
GATE High Voltage		V_{GATE} - V_{PWM_IN}, sourcing 1µA	4.7	5.4	6.1	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{PWM_IN} = 12V or V_{IN} = V_{PWM_IN} = V_{REG} = 5V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 100kΩ, R_{ILIM} = 60kΩ, C_{REG} = 2.2µF, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE Pulldown Resistance		Sinking 1mA to AGND			40	Ω
Hot-Swap FET Enhancement Threshold		V_{GATE} rising	3.45	4.0	4.65	V
Hot-Swap FET Enhancement Hysteresis				70		mV
HOT-SWAP LOGIC OUTPUTS						
DCENO Internal Pullup Current				10		µA
$\overline{PWRFLT}$, $\overline{MPWRGD}$ Input Leakage			-1		+1	µA
$\overline{PWRFLT}$, $\overline{MPWRGD}$, DCENO Output Voltage Low		Sinking 2.4mA			50	mV
$\overline{MPWRGD}$ Power-On-Reset Time			100	165	250	ms
HOT-SWAP LOGIC INPUTS						
PGI Input High-Level Voltage			2			V
PGI Input Low-Level Voltage					0.8	V
PGI Input Hysteresis				260		mV
PGI Blanking Time from DCENO High			100	165	250	ms
PWM UVLO						
Default PWM Undervoltage Lockout Threshold		V_{PWM_IN} rising	6.7		7.3	V
PWM Undervoltage Lockout Hysteresis				0.7		V
PUVLO Threshold	V_{PUVLO}	V_{PUVLO} rising	1.202	1.22	1.238	V
PUVLO Hysteresis				122		mV
PUVLO Input Impedance			180	310	500	kΩ
PWM DCENI CONTROL						
DCENI Comparator Input Common-Mode Range			0		3	V
DCENI Comparator Offset		V_{DCENI} - V_{THRESH}	-10		+10	mV
DCENI Comparator Hysteresis				100		mV
DCENI Input Current			-1		+1	µA
THRESH Operating Voltage Range			0.6		2.5	V
THRESH Input Current		V_{THRESH} > 0.6V	-1.5		+1.0	µA
		V_{THRESH} < 0.3V	-5		+1	
Default DCENI Threshold		V_{THRESH} < 0.3V	1.202	1.22	1.238	V
PWM PGOOD OUTPUT						
SENSE Threshold		V_{SENSE} rising	788	800	812	mV
SENSE Hysteresis				100		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{PWM_IN} = 12V or V_{IN} = V_{PWM_IN} = V_{REG} = 5V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 100kΩ, R_{ILIM} = 60kΩ, C_{REG} = 2.2µF, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SENSE Input Bias Current				-1		+1	µA
PGOOD Internal Pullup Current					10		µA
PGOOD Output-Voltage Low		I_{PGOOD} = -2.4mA				50	mV
INTERNAL VOLTAGE REGULATOR							
Output-Voltage Set Point	V_{REG}			4.7		5.3	V
Line Regulation		V_{PWM_IN} = 8V to 16V				1	mV/V
Load Regulation		I_{REG} = 0 to 50mA				150	mV
PWM OSCILLATOR							
Oscillator Frequency Range	f_{SW}	V_{SYNCIN} = 0V, f_{SW} = 5 x 10^{10} / R_{RT} Hz		100		1000	kHz
Oscillator Accuracy		T_A = T_J = +25°C	f_{SW} ≤ 500kHz	-2.5		+2.5	%
			f_{SW} > 500kHz	-4		+4	
		T_A = T_J = -40°C to +85°C	f_{SW} ≤ 500kHz	-3.5		+3.5	
			f_{SW} > 500kHz	-5		+5	
RT Voltage	V_{RT}	50kΩ ≤ R_{RT} ≤ 500kΩ			2		V
Maximum Duty Cycle		V_{SYNCIN} = 0V, V_{PWM_IN} = 12V		82	88		%
SYNCIN High Level Voltage				2.1			V
SYNCIN Low Level Voltage						0.8	V
SYNCIN Pulldown Resistor				50	100	150	kΩ
SYNCIN Rising to SYNCOUT Falling Delay					10		ns
SYNCIN Falling to SYNCOUT Rising Delay					30		ns
Maximum SYNCIN Frequency				1			MHz
SYNCOUT Voltage High	$VH_{SYNCOUT}$	$I_{SYNCOUT}$ = +1.2mA		V_{REG} - 0.1			V
SYNCOUT Voltage Low	$VL_{SYNCOUT}$	$I_{SYNCOUT}$ = -2.4mA				50	mV
PWM ERROR AMPLIFIER							
FB Input Range				0		V_{REF}	V
FB Input Current				-250		+250	nA
COMP Output-Voltage Range		I_{COMP} = -500µA to +500µA		0.25		V_{REG} - 0.5	V
Open-Loop Gain					80		dB
Unity-Gain Bandwidth	f_{GBW}				2.5		MHz
Reference Voltage	V_{REF}	I_{COMP} = -500µA to +500µA		792	800	808	mV
PWM COMPARATOR							
Comparator Offset Voltage					0.3		V
Comparator Propagation Delay					40		ns
PWM DIGITAL SOFT-START							
Soft-Start Duration					1024		Clocks
Reference Voltage Steps					128		Steps
					6.3		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{PWM_IN} = 12V or V_{IN} = V_{PWM_IN} = V_{REG} = 5V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 100kΩ, R_{ILIM} = 60kΩ, C_{REG} = 2.2µF, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM RAMP GENERATOR						
Ramp Amplitude				1.8		V
PWM CURRENT-LIMIT COMPARATOR AND HICCUP MODE						
Cycle-by-Cycle Valley Current-Limit Threshold Adjustment Range		Limit = V_{ILIM} / 10	50		350	mV
Cycle-by-Cycle Valley Current-Limit Threshold Tolerance		V_{ILIM} = 0.5V	44.5		55.5	mV
		V_{ILIM} = 3.5V	330		366	
ILIM Reference Current		V_{ILIM} = 0 to 3.5V, T_A = T_J = +25°C	19	20	21	µA
ILIM Reference Current Tempco				3333		ppm/°C
CS+, CS- Input Bias Current		V_{CS+} = 0V, V_{CS-} = -0.3V, current out of the CS_	-1		+20	µA
PWM HICCUP MODE						
Number of Cumulative Current-Limit Events to Hiccup	N_{CL}			8		Clocks
Number of Consecutive Non-Current Limit Cycles to Clear N_{CL}	N_{CLR}			3		Clocks
Hiccup Timeout	N_{HT}			512		Clocks
PWM STARTUP INPUT						
STARTUP Threshold	V_{SUT}	V_{SUT} rising	1.1		1.9	V
STARTUP Threshold Hysteresis				250		mV
Internal Pullup Current	I_{START}			10		µA
STARTUP Output Voltage Low		$I_{STARTUP}$ = -2.4mA			50	mV
PWM DH DRIVER						
Peak Source Current		$V_{DH,LX}$ = 0V, pulse width < 100ns, $V_{BST, LX}$ = 5V		2		A
Peak Sink Current		$V_{DH,LX}$ = 5V, pulse width < 100ns, $V_{BST, LX}$ = 5V		2		A
DH Resistance Sourcing		I_{DH} = 50mA, $V_{BST, LX}$ = 5V		1	3	Ω
DH Resistance Sinking		I_{DH} = -50mA, $V_{BST, LX}$ = 5V		1	3	Ω
PWM DL DRIVER						
Peak Source Current		V_{DL} = 0V, pulse width < 100ns, V_{DREG} = 5V		2		A
Peak Sink Current		V_{DL} = 5V, pulse width < 100ns, V_{DREG} = 5V		2		A
DL Resistance Sourcing		I_{DL} = 50mA, V_{DREG} = 5V		1	3	Ω
DL Resistance Sinking		I_{DL} = -50mA, V_{DREG} = 5V		1	3	Ω
Break-Before-Make Time				25		ns
THERMAL SHUTDOWN						
Thermal-Shutdown Temperature		T_J rising		+135		°C
Thermal-Shutdown Hysteresis				15		°C

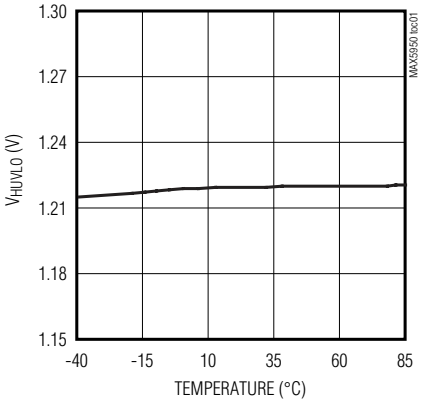
Note 1: Limits at -40°C are guaranteed by design and are not production tested.
Note 2: For 5V applications, connect REG directly to PWM_IN.

12V PWM Controller with Hot-Swap

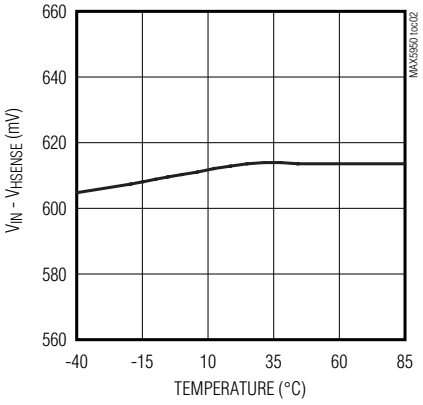
Typical Operating Characteristics

(*Typical Application Circuits.* V_{IN} = V_{PWM_IN} = 12V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 49.9kΩ, R_{ILIM} = 48.7kΩ, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

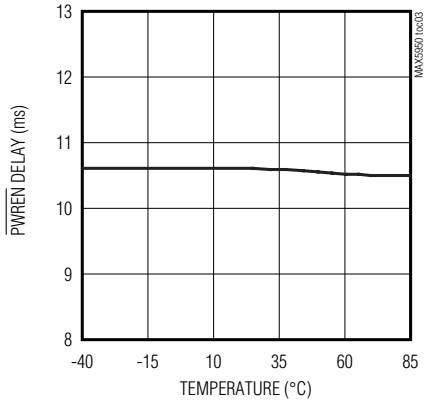
HOT-SWAP UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



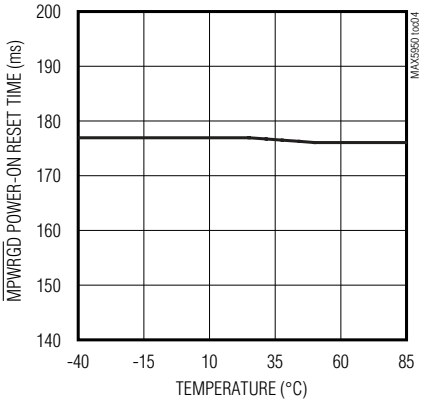
CIRCUIT-BREAKER THRESHOLD vs. TEMPERATURE



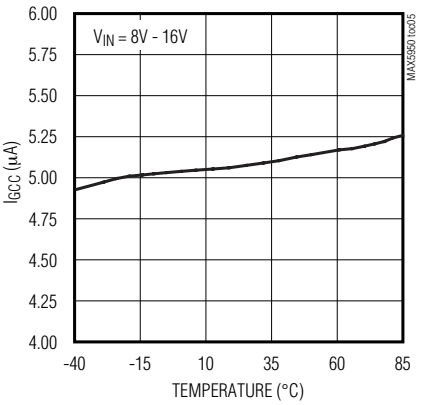
$\overline{PWREN}$ DELAY vs. TEMPERATURE



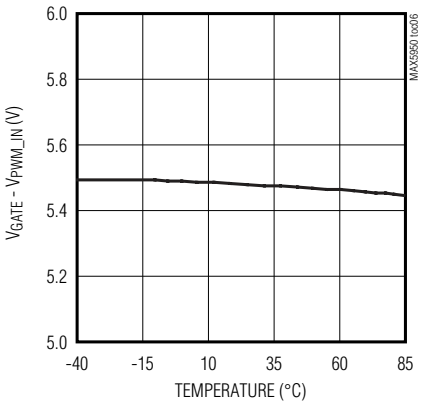
$\overline{MPWRGD}$ POWER-ON RESET TIME vs. TEMPERATURE



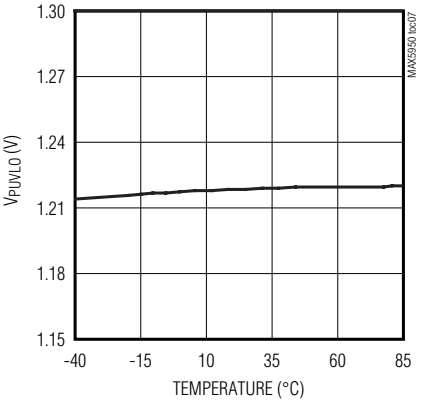
GATE CHARGE CURRENT vs. TEMPERATURE



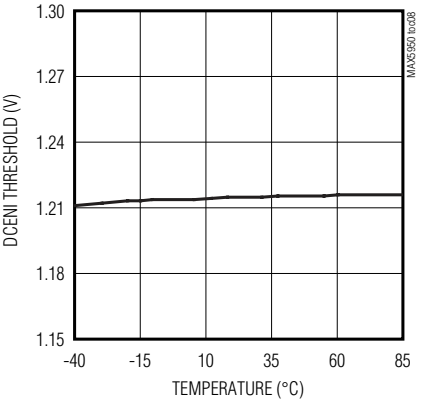
GATE HIGH VOLTAGE vs. TEMPERATURE



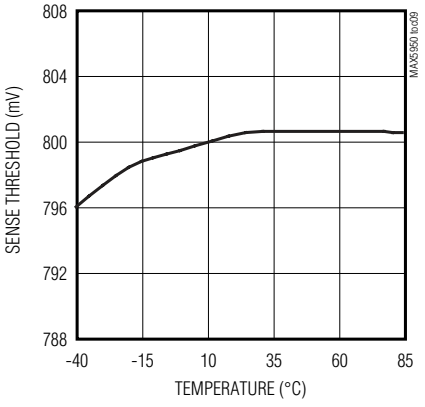
PWM UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



DEFAULT DCENI THRESHOLD vs. TEMPERATURE



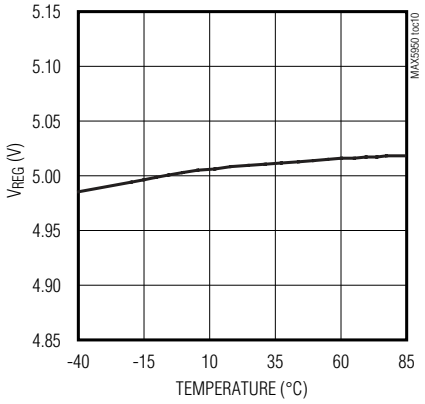
SENSE THRESHOLD vs. TEMPERATURE



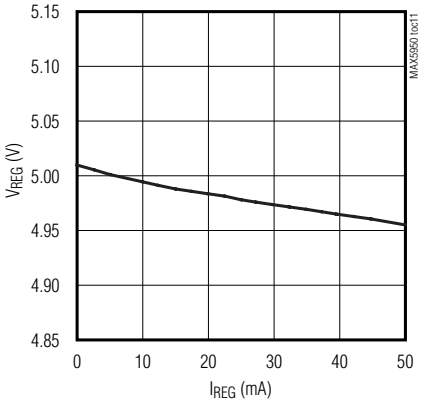
Typical Operating Characteristics (continued)

(*Typical Application Circuits.* V_{IN} = V_{PWM_IN} = 12V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 49.9kΩ, R_{ILIM} = 48.7kΩ, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

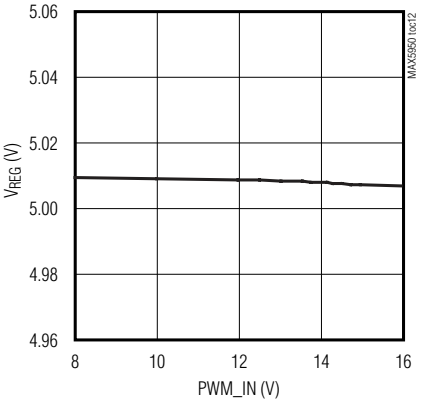
REG OUTPUT VOLTAGE vs. TEMPERATURE



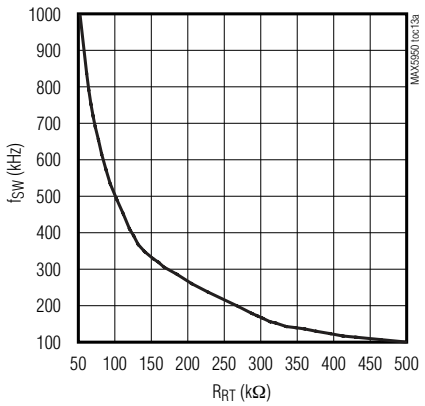
REG OUTPUT VOLTAGE vs. LOAD CURRENT



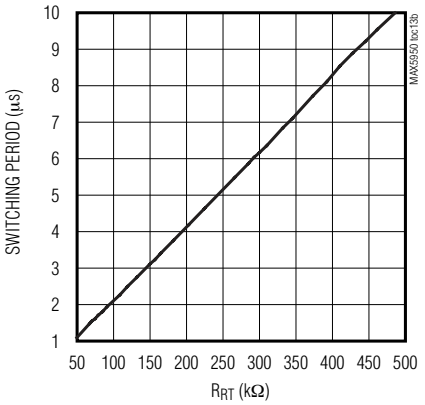
REG OUTPUT VOLTAGE vs. INPUT VOLTAGE



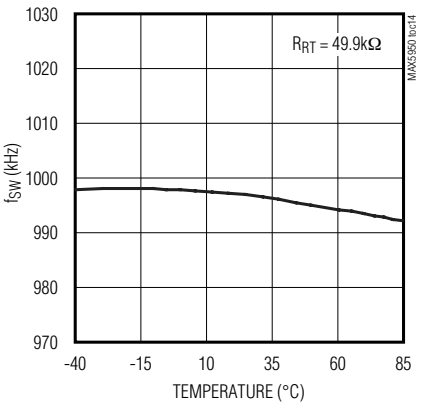
SWITCHING FREQUENCY vs. R_{RT}



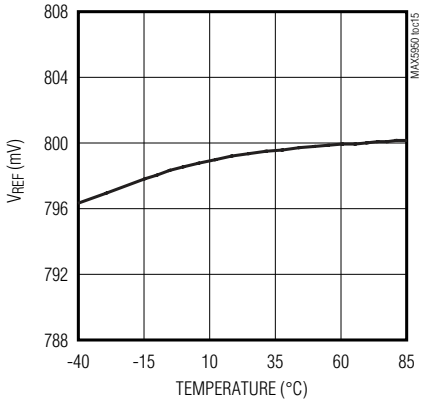
SWITCHING PERIOD vs. R_{RT}



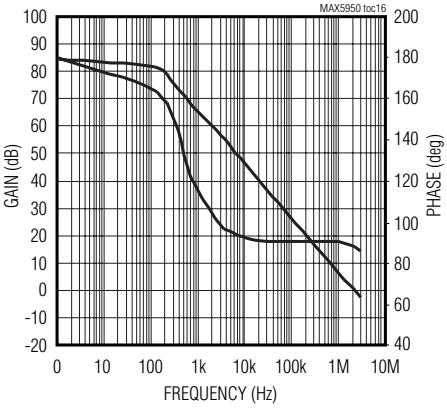
SWITCHING FREQUENCY vs. TEMPERATURE



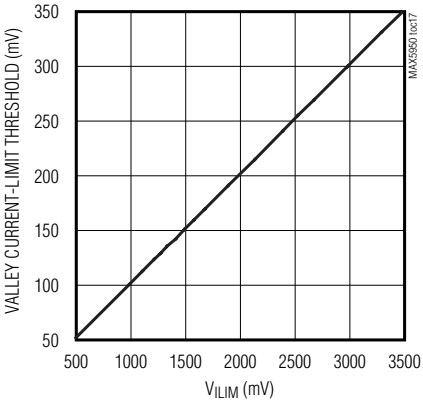
FB REFERENCE VOLTAGE vs. TEMPERATURE



OPEN-LOOP GAIN/PHASE vs. FREQUENCY



VALLEY CURRENT-LIMIT THRESHOLD vs. V_{ILIM}

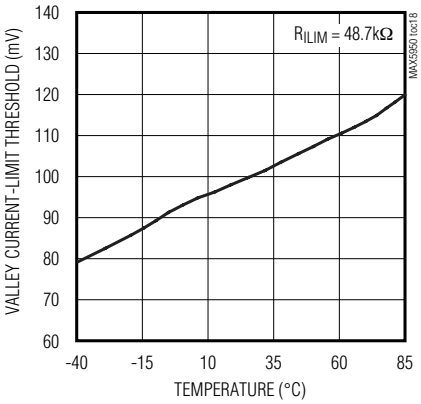


12V PWM Controller with Hot-Swap

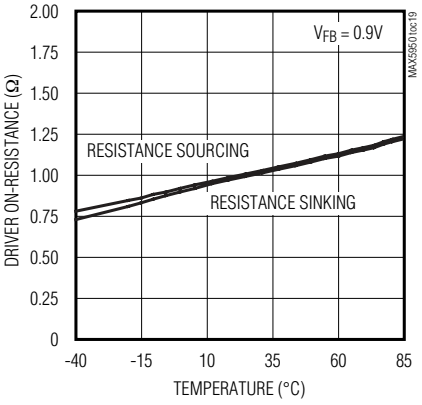
Typical Operating Characteristics (continued)

(*Typical Application Circuits.* V_{IN} = V_{PWM_IN} = 12V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 49.9kΩ, R_{ILIM} = 48.7kΩ, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

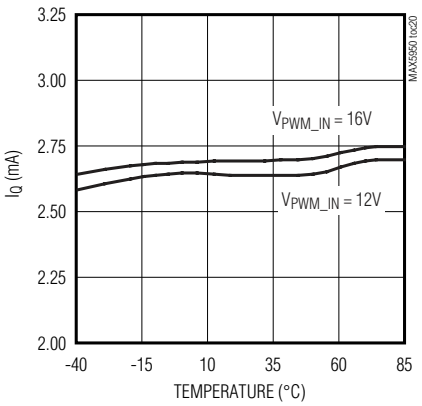
VALLEY CURRENT-LIMIT THRESHOLD vs. TEMPERATURE



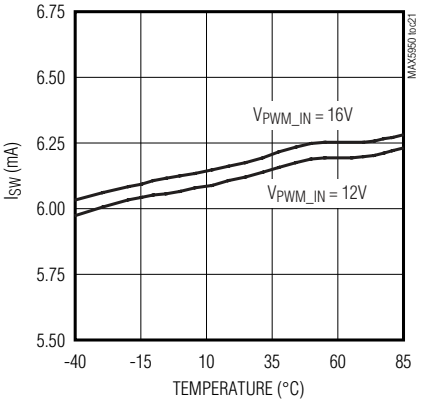
DL, DH DRIVER ON-RESISTANCE vs. TEMPERATURE



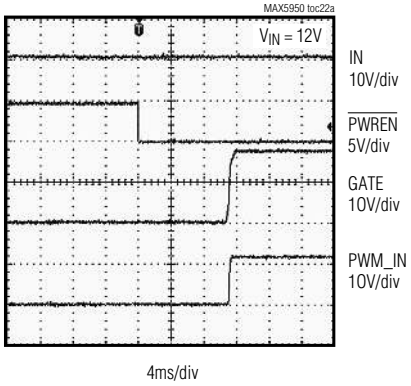
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



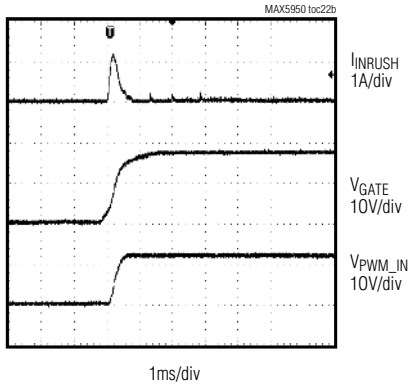
SWITCHING SUPPLY CURRENT vs. TEMPERATURE



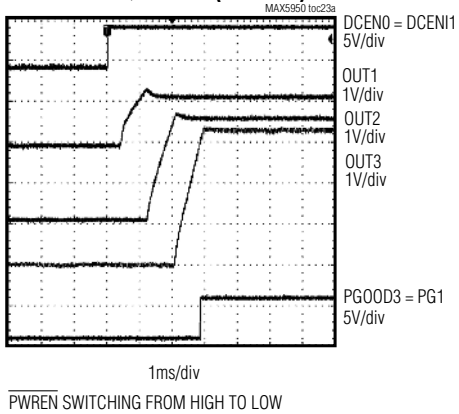
STARTUP WAVEFORM



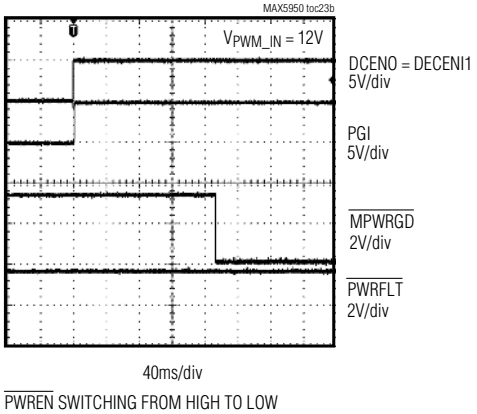
STARTUP WAVEFORM



PGOOD SEQUENCING (FIGURE 1)



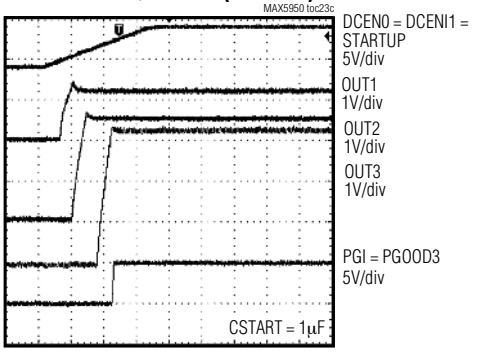
STARTUP



Typical Operating Characteristics (continued)

(*Typical Application Circuits.* V_{IN} = V_{PWM_IN} = 12V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 49.9kΩ, R_{ILIM} = 48.7kΩ, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

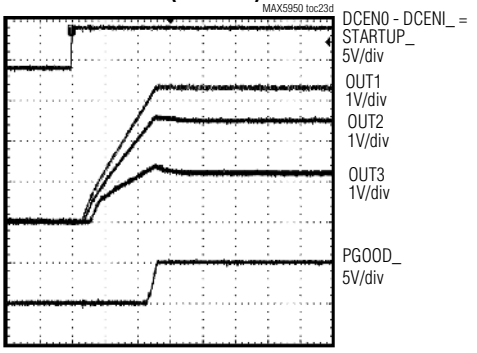
STARTUP SEQUENCING (FIGURE 1)



2ms/div

PWREN SWITCHING FROM HIGH TO LOW

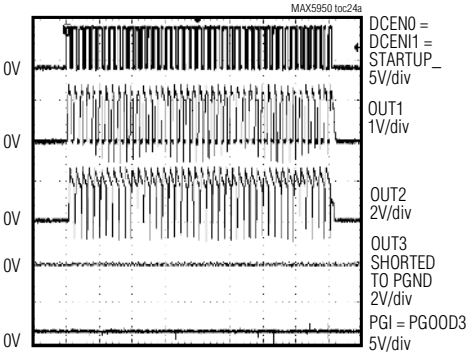
TRACKING (FIGURE 1)



400µs/div

PWREN SWITCHING FROM HIGH TO LOW

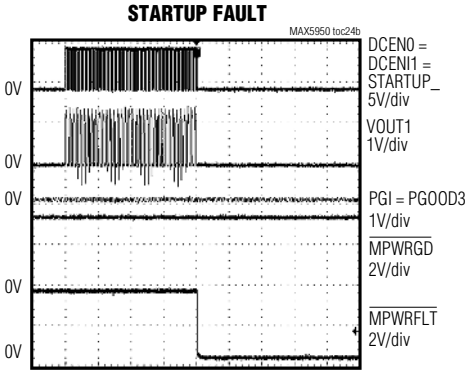
STARTUP FAULT



20ms/div

PWREN SWITCHING FROM HIGH TO LOW

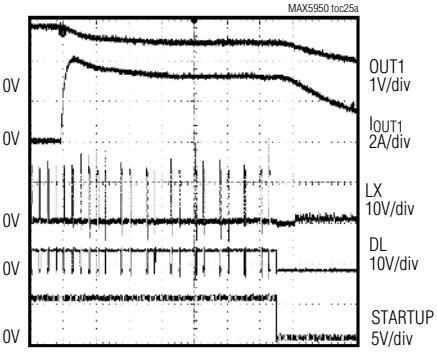
STARTUP FAULT



40ms/div

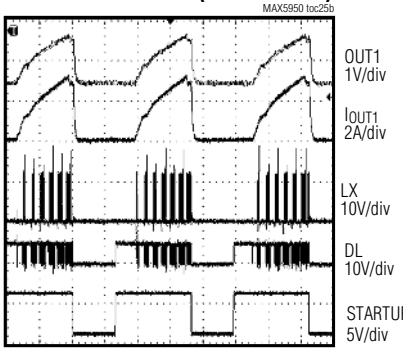
PWREN SWITCHING FROM HIGH TO LOW
OUT3 SHORTED TO PGND

OVERLOAD RESPONSE



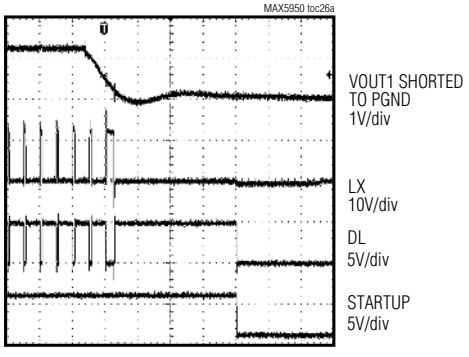
4µs/div

OVERLOAD RESPONSE (HICCUP MODE)



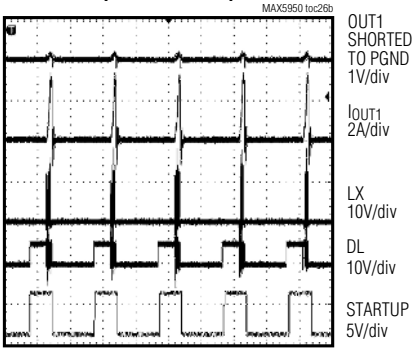
400µs/div

SHORT-CIRCUIT RESPONSE



2µs/div

SHORT-CIRCUIT RESPONSE (HICCUP MODE)



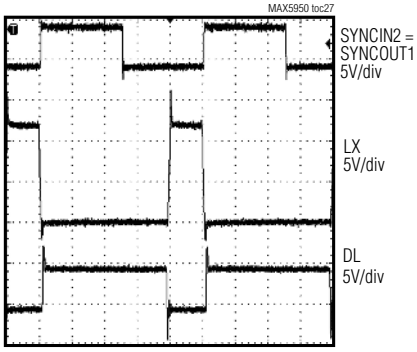
400µs/div

12V PWM Controller with Hot-Swap

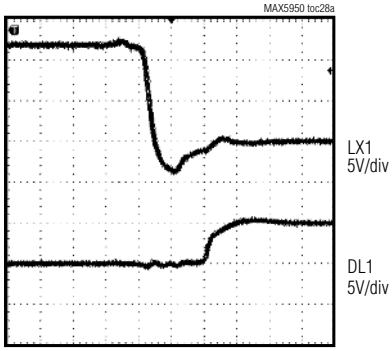
Typical Operating Characteristics (continued)

(*Typical Application Circuits.* V_{IN} = V_{PWM_IN} = 12V, V_{DREG} = V_{REG}, V_{PGND} = 0V, V_{SYNCIN} = 0V, R_{RT} = 49.9kΩ, R_{ILIM} = 48.7kΩ, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

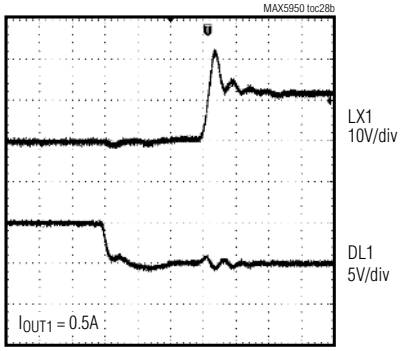
SYNCHRONIZATION



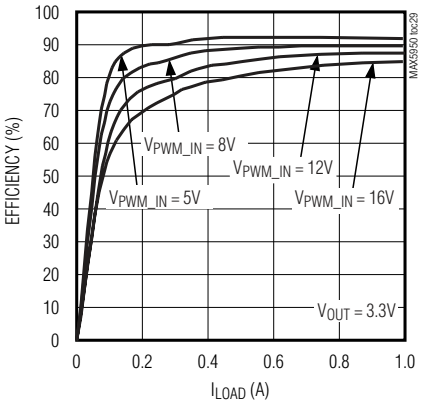
BREAK-BEFORE-MAKE TIME



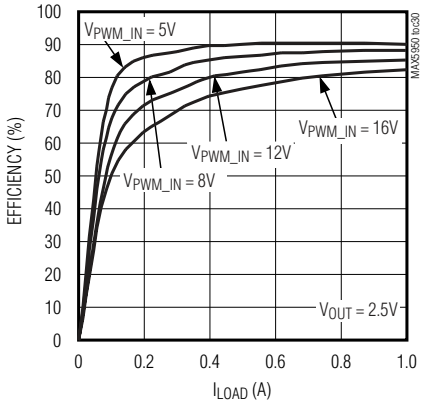
BREAK-BEFORE-MAKE TIME



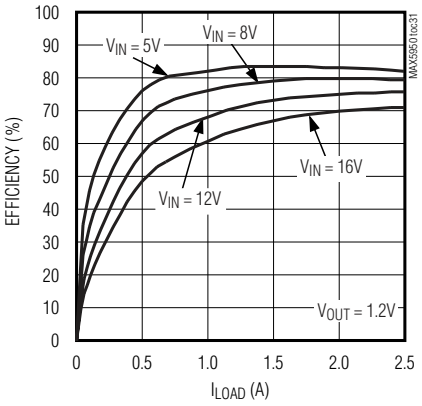
EFFICIENCY vs. LOAD CURRENT



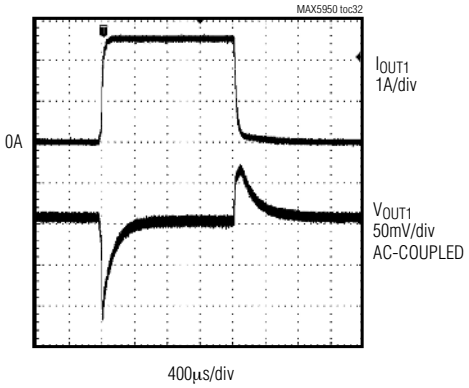
EFFICIENCY vs. LOAD CURRENT



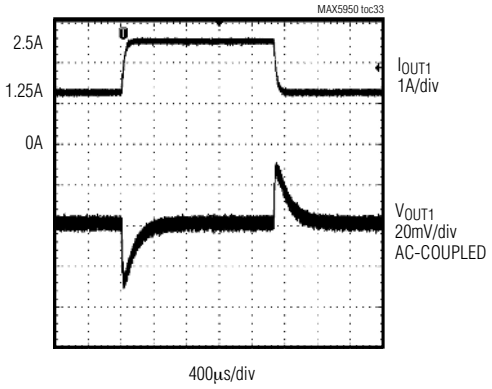
EFFICIENCY vs. LOAD CURRENT



LOAD-TRANSIENT RESPONSE



LOAD-TRANSIENT RESPONSE



Pin Description

PIN	NAME	FUNCTION
1	PWM_IN	PWM Controller Input Voltage
2	PUVLO	PWM UVLO Divider Center Point. Use an external divider to override the internal PWM UVLO divider. The rising threshold is set to 1.220V with 122mV hysteresis. Leave PUVLO unconnected for the default PWM UVLO.
3	HSENSE	Hot-Swap Negative-Sense Input. Connect HSENSE close to the hot-swap FET source.
4	GATE	Hot-Swap Gate-Drive Output. Connect GATE to the gate of an external n-channel MOSFET.
5	IN	Supply Input Connection. Connect to an external voltage source from 8V to 16V. For 5V input application, connect IN = PWM_IN = REG to a 5V ±10% source. Connect an external divider from IN to PUVLO to AGND to lower the startup voltage. Connect an external divider from IN to HUVLO to AGND to override the hot-swap undervoltage lockout threshold.
6	HUVLO	Center Point of the Hot-Swap UVLO Divider. Use an external divider to override the internal hot-swap UVLO divider. The rising threshold is 1.220V with 120mV hysteresis. Leave HUVLO unconnected for the default hot-swap UVLO.
7	$\overline{\text{PWREN}}$	Active-Low Power-Enable Input. Pull $\overline{\text{PWREN}}$ low for at least 10ms for the hot-swap to commence. Active-low $\overline{\text{PWREN}}$ is internally pulled high.
8	$\overline{\text{PWRFLT}}$	Active-Low Power-Fault Output. This open-drain output latches low when a hot-swap or PWM fault occurs. Pulse $\overline{\text{PWREN}}$ high, then low or cycle the power supply to clear the latch.
9	$\overline{\text{MPWRGD}}$	Active-Low Module Power-Good Output. This open-drain output goes low 165ms after the hot-swap is completed. $\overline{\text{MPWRGD}}$ indicates that both hot-swap and downstream DC-DC switchers are operating properly.
10	PGI	Power-Good Input. Connect PGI to the PGOOD outputs of the DC-DC switchers. PGI is used to indicate that all the output voltages of the DC-DC switchers are in range. PGI blanks for 165ms after the hot-swap is completed to allow for DC-DC startup. The hot-swap circuit shuts down if PGI is not pulled high before the blanking period ends.
11	DCENO	DC-DC Enable Output. This output goes high once the hot-swap is completed. Use DCENO to enable downstream DC-DC switchers.
12	DCENI	DC-DC Enable Input. DCENI must be above V_{THRESH} for the PWM controller to start. Connect to REG if not used.
13	THRESH	DC-DC Enable Input Threshold Set. Connect a resistive divider from REG to THRESH to AGND to set the DCENI threshold. Connect to ground for a default threshold of 1.220V.
14	AGND	Analog Ground Connection. Solder the exposed pad to a large AGND plane. Connect AGND and PGND together at one point near the input bypass capacitor return terminal.
15	SYNCOUT	Synchronization Output. SYNCOUT is a synchronization signal to drive the SYNCIN of a second MAX5950/MAX5951, if used. Leave SYNCOUT unconnected when not used.
16	SYNCIN	Synchronization Input. SYNCIN accepts the SYNCOUT from another MAX5950/MAX5951 and shifts switching by 180°, allowing the reduction of the input bypass capacitors. When used, drive with a frequency at least 20% higher than the frequency programmed through the RT pin. If phase staggering is desired, use 50% duty cycle. Connect SYNCIN to AGND when not used.
17	RT	Oscillator Timing Resistor Connection. Connect a 500kΩ to 50kΩ resistor from RT to AGND to program the switching frequency from 100kHz to 1MHz.
18	STARTUP	Startup Input. STARTUP coordinates simultaneous soft-start for multiple converters. See the *Tracking (STARTUP)* section.
19	PGOOD	Power-Good Output. PGOOD output goes high when SENSE is above V_{REF} and STARTUP is high.
20	COMP	Error Amplifier Output. Connect COMP to the compensation feedback network.

12V PWM Controller with Hot-Swap

Pin Description (continued)

PIN	NAME	FUNCTION
21	FB	Feedback Regulation Point. Connect to the center tap of a resistive divider from the converter output to AGND to set the output voltage. The FB voltage regulates to the reference voltage.
22	SENSE	Output Voltage Sense. Connect a resistive divider from the converter output to SENSE to AGND to monitor the programmed output voltage. SENSE is compared to the internal reference, V_{REF}.
23	ILIM	Valley Current-Limit Set Output. Connect a 25kΩ to 175kΩ resistor, R_{ILIM}, from ILIM to AGND to program the valley current-limit threshold from 50mV to 350mV. ILIM sources 20µA out to R_{ILIM}. The resulting voltage divided by 10 is the valley current limit. Alternatively, a resistive divider from REG to ILIM to AGND can be used to set the valley current limit.
24	CS+	Positive Current-Sense Input. Connect CS+ to the synchronous MOSFET source (connected to PGND).
25	CS-	Negative Current-Sense Input. Connect CS- to the synchronous MOSFET drain (connected to LX).
26	PGND	Power-Ground Connection. Connect the input filter capacitor's negative terminal, the source of the synchronous MOSFET, and the output filter capacitor's return to PGND. Connect externally to AGND at a single point near the input capacitor return terminal.
27	DL	Low-Side Gate-Driver Output. DL is the gate-driver output for the synchronous MOSFET.
28	DREG	Gate-Drive Supply for the Low-Side MOSFET Driver. Connect externally to REG and anode of the boost diode.
29	LX	Source Connection of the High-Side MOSFET and Drain Connection of the Synchronous MOSFET. Connect the inductor and the negative side of the boost capacitor to LX.
30	DH	High-Side Gate-Driver Output. DH drives the gate of the high-side MOSFET.
31	BST	High-Side Gate-Driver Supply. Connect BST to the cathode of the boost diode and to the positive terminal of the boost capacitor.
32	REG	5V Regulator Output. Bypass with a 2.2µF ceramic capacitor to AGND.
—	EP	Exposed Pad. Connect the exposed pad to AGND.

Detailed Description

The MAX5950 is a PWM, step-down, DC-DC controller with integrated hot-swap controller. The device operates over the 8V to 16V or 5V ±10% (V_{IN} = V_{PWM_IN} = V_{REG}) input-voltage range and provides an adjustable output from 0.8V to 5.5V. The device delivers up to 10A of load current with excellent load-and-line regulation.

The MAX5950 features a hot-swap controller that provides inrush current control during module insertion and removal, as well as short-circuit protection during normal operation. Normally, when a line card is plugged into a live backplane, the card's discharged filter capacitors provide a low impedance that can momentarily cause the main power supply to collapse. The MAX5950 provides inrush current limiting by slowly enhancing the pass transistor (nMOS) when the board is plugged in, allowing the system to stabilize safely. The device provides short-circuit protection by disconnecting the load in the event of a fault condition. The MAX5950 features an internal charge pump that provides the gate drive for the external n-channel MOSFET.

The MAX5950 PWM controller utilizes a voltage-mode control scheme for good noise immunity and offers external compensation, allowing for maximum flexibility with a wide selection of inductor values and capacitor types. The device operates at a fixed switching frequency that is programmable from 100kHz to 1MHz and can be synchronized to an external clock signal through the SYNC input. The device includes UVLO and digital soft-start. Protection features include valley-mode current limit, hiccup-mode output short-circuit protection, and thermal shutdown.

The MAX5950 is optimized for PCIe ExpressModule power-management application. Table 1 shows the PCIe ExpressModule power-supply rail requirements.

Table 1. PCIe ExpressModule Power-Supply Rail Requirements

POWER RAIL	SINGLEWIDE	DOUBLEWIDE
+12V Bulk		
Voltage Tolerance	±15% (max)	±15% (max)
Continuous Current	2.08A (max)	4.17A (max)
Initial Hot-Plug Capacitance	5000pF (max)	5000pF (max)
Input Capacitance	500µF (max)	500µF (max)

POWER RAIL	SINGLEWIDE	DOUBLEWIDE
+3.3VAUX		
Voltage Tolerance	±10% (max)	±10% (max)
Continuous Current	475mA (max)	950mA (max)
Peak Precharge Current	475mA (peak)	950mA (peak)
Input Capacitance	150µF (max)	300µF (max)
Precharge Pin Timing	3ms (max)	3ms (max)

Notes For Table 1:

1. The +12V power hot-swap circuits are located on the module.
2. Currents during hot insertion do not exceed the module maximum continuous current.
3. The module and connector are not damaged during hot removal or insertion.
4. The +3.3VAUX power precharges the module's +3.3VAUX input capacitors during hot insertion through first precharge pin mating.
5. Peak precharge current during hot insertion is determined by the value of the precharge resistor. Single wide example: precharge resistor = +3.3V/475mA = 7mΩ.
6. +3.3VAUX precharge pin timing is the maximum time guaranteed during hot insertion from the +3.3VAUX precharge pin mating to the main power pin's mating. The time constant with the maximum input capacitance and precharge resistor do not exceed 1/3 of the precharge pin timing.
7. Example: 150µF x 7Ω = 1ms (which is 1/3 the maximum precharge pin timing of 3ms).
8. The maximum current slew rate for each add-in module is no more than 0.1A/µs.
9. Each add-in module limits its capacitance on each power rail at the backplane connector to that listed in the above table.
10. Continuous current = the highest averaged current value over any 1s period.

Hot-Swap Controller

Startup and Undervoltage Lockout

The startup period begins 10ms after V_{IN} exceeds the default hot-swap UVLO threshold (7V typ) and $\overline{PWREN}$ is low. This prevents the MAX5950 from turning on the external MOSFET until V_{IN} exceeds the lockout threshold for 10ms to protect the external MOSFET from insufficient gate-drive voltage. The 10ms timeout ensures that the board is fully plugged into the backplane and that IN is stable. Any negative input-voltage transient at IN below the UVLO threshold resets the device and initiates a new startup cycle.

Override the internal hot-swap UVLO divider by connecting a resistive divider from IN to HUVLO to AGND. The HUVLO threshold is 1.220V with 120mV hysteresis.

During startup, the MAX5950 limits the inrush current by controlling the external n-channel MOSFET gate voltage, thus slowly enhancing the MOSFET.

Normal Operation (Circuit Breaker)

In normal operation, the device provides short-circuit protection by monitoring the voltage drop across the on-resistance of the n-channel MOSFET (V_{IN} - V_{HSENSE}), and comparing the voltage drop to the circuit-breaker threshold, 600mV (typ). The MAX5950 quickly forces and latches the MOSFET off when the circuit-breaker threshold is reached.

DCENO, $\overline{PWRFLT}$, $\overline{MPWRGD}$

The MAX5950 integrates a DC-DC enable-output (DCENO) that goes high after hot-swapping is completed and PGI has been driven high. Use DCENO to enable downstream PWM controllers and allow a smooth transition from inrush to power mode.

The device features an open-drain power-good output ($\overline{MPWRGD}$) that goes low 165ms after hot-swap is completed and PGI has been driven high. $\overline{MPWRGD}$ low indicates that both hot-swap and downstream DC-DC converters are operating properly.

The device includes an open-drain power-fault output ($\overline{PWRFLT}$) that latches low when a fault is detected by the hot-swap controller. Possible faults include a circuit-breaker event, a thermal-shutdown event, or if PGI is not pulled high within 165ms after DCENO goes high. When such a fault is detected, the MAX5950 forces and latches off the inrush-controlled MOSFET, and DCENO goes low to shut down the DC-DC converters. Pulse $\overline{PWREN}$ high, then low or cycle the power supply to clear the latch.

12V PWM Controller with Hot-Swap

$\overline{PWREN}$, PGI

The active-low power-enable input, $\overline{PWREN}$, is internally pulled high. Pull $\overline{PWREN}$ low for at least 10ms for the hot-swap to commence. Connect PGI to the PGOOD outputs of the DC-DC converters. PGI is used to indicate that all the output voltages of the DC-DC converters are in range. PGI blanks for 165ms after the hot-swap is completed to allow for the DC-DC converters to startup.

PWM Controller

PWM UVLO

V_{PWM_IN} must exceed the default PWM UVLO threshold (7V typ) before any PWM operation can commence. The UVLO circuitry keeps the MOSFET drivers, oscillator, and all the internal circuitry shut down to reduce current consumption.

Override the internal PWM UVLO divider by connecting an external resistive divider from IN to PUVLO to AGND. The PUVLO threshold is 1.220V with 120mV hysteresis.

Digital Soft-Start

The MAX5950 soft-start feature allows the load voltage to ramp up in a controlled manner, eliminating output-voltage overshoot. Soft-start begins after V_{PWM_IN} exceeds the UVLO threshold. The soft-start circuitry gradually ramps up the reference voltage. This controls the rate of rise of the output voltage and reduces input surge currents during startup. The soft-start duration is 1024 clock cycles. The output voltage is incremented through 128 equal steps. The output reaches regulation when soft-start is completed, regardless of output capacitance and load.

Internal Linear Regulator (REG)

REG is the output terminal of a 5V LDO, which is powered from PWM_IN and provides power to the IC. Bypass REG to GND with a 2.2µF ceramic capacitor. Place the capacitor physically close to the MAX5950 to provide good bypassing. REG is intended for powering only the internal circuitry and should not be used to supply power to external loads.

Low-Side MOSFET Driver Supply (DREG)

DREG is the supply input for the low-side MOSFET driver. Connect DREG to REG externally. Adding an RC filter (5Ω and 2.2µF ceramic capacitor) from REG to DREG filters out the high-peak currents of the MOSFET drivers.

High-Side MOSFET Driver Supply (BST)

BST supplies the power for the high-side MOSFET drivers. Connect the bootstrap diode from BST to DREG (anode at DREG and cathode at BST). Connect a bootstrap 1µF ceramic capacitor between BST and LX.

MOSFET Gate Drivers (DH, DL)

The high-side (DH) and low-side (DL) drivers drive the gates of the external n-channel MOSFETs. The drivers' 2A peak source-and-sink current capability provides ample drive to assure fast rise and fall times of the switching MOSFETs. Short rise and fall times minimize switching losses. For low-output voltage applications where the duty cycle is less than 50%, choose a high-side MOSFET (Q2) with a moderate $R_{DS(ON)}$. Choose a low-side MOSFET (Q1) with a very low $R_{DS(ON)}$.

The gate-driver circuitry also provides a break-before-make time (25ns typ) to prevent shoot-through currents during transition.

Oscillator/Synchronization Input (SYNCIN)/ Synchronization Output (SYNCOUT)

Use an external resistor at RT to program the MAX5950 switching frequency from 100kHz to 1MHz.

Choose the appropriate resistor at RT to calculate the desired output switching frequency (f_{SW}):

$$f_{SW}\ (Hz) = (5 \times 10^{10}) / R_{RT}\ (\Omega)$$

Connect an external clock (SYNCOUT from another MAX5950/MAX5951) at SYNCIN for external clock synchronization. For proper synchronization, the external frequency must be at least 20% higher than the frequency programmed through the RT input. If SYNCIN is 50% duty cycle, SYNCOUT is shifted by 180°, allowing the reduction of the DC-DC converter input bypass capacitor.

SYNCOUT is a synchronization signal that is used to drive the SYNCIN of a second MAX5950/MAX5951.

Tracking (STARTUP)

The STARTUP input in conjunction with digital soft-start provides simple ratiometric tracking. When using multiple MAX5950s/MAX5951s, in addition to connecting SYNCIN and SYNCOUT signals appropriately, connect the STARTUP of all the devices together. STARTUP synchonizes the soft-start of all the devices' references, and hence their respective output voltages track ratiometrically. See Figure 1 and the *Typical 0perating Circuits*.

The STARTUP input has an internal 10µA pullup current, but can be driven by external logic. When using multiple converters, connect the STARTUP of all the devices together.

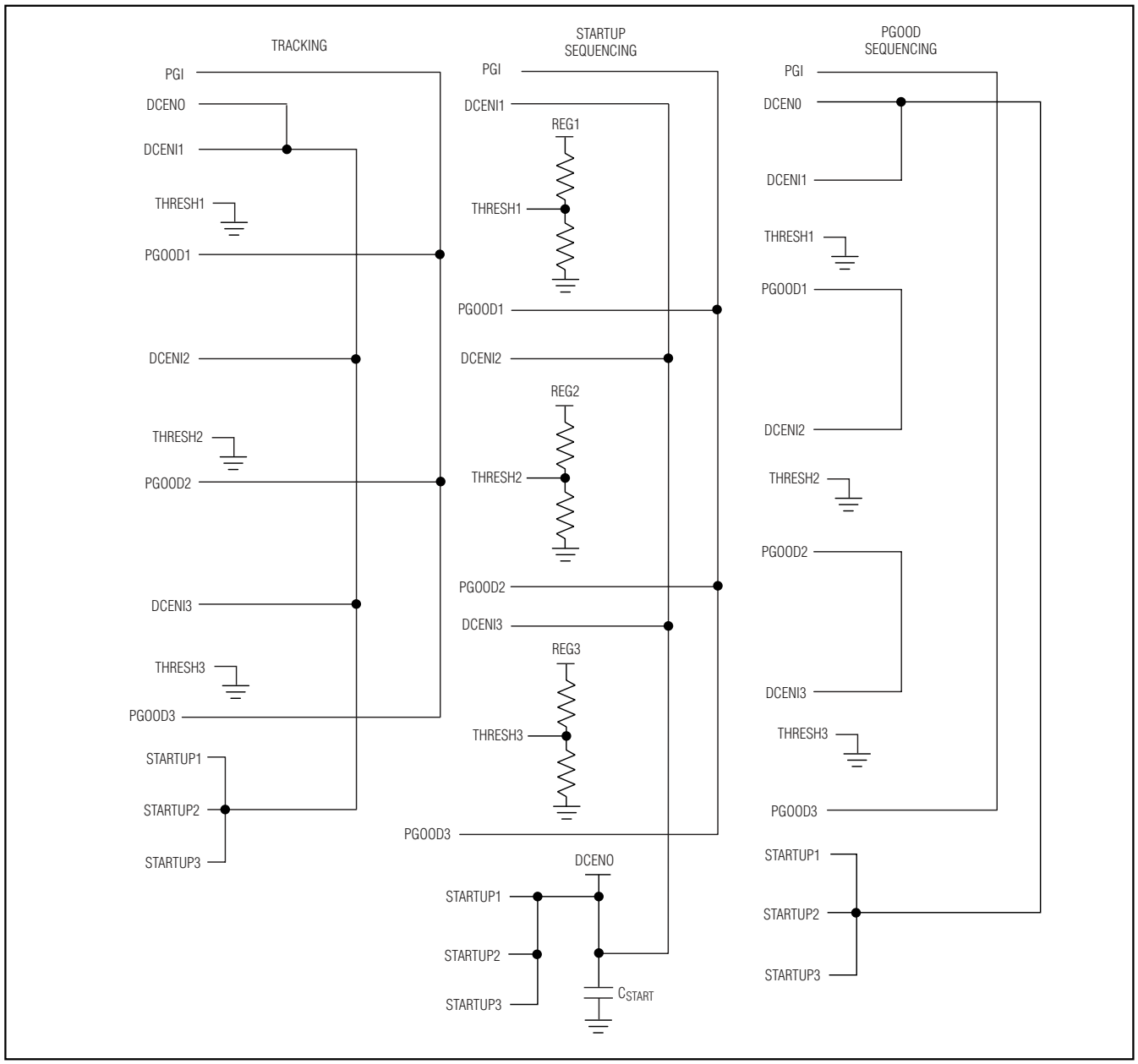


Figure 1. Tracking, STARTUP Sequencing, and PGOOD Sequencing Configurations

Startup Sequencing (DCENI, THRESH)

The DCENI input must be above V_{THRESH} for the PWM controller to start. By connecting the DCENI inputs of multiple devices together and having different start thresholds ($V_{THRESH\_}$), the startup of the PWM controllers can be staggered to provide power sequencing. Connect a resistive divider from REG to THRESH to AGND to set the start thresholds of each device between 0.6V and 2.5V. Connect THRESH to AGND to produce a default 1.220V threshold for DCENI. Connecting THRESH to REG disables the converter. See Figure 1 and the *Typical Operating Circuit*.

12V PWM Controller with Hot-Swap

Power-Good Sequencing (PGOOD, SENSE)

The PGOOD outputs and DCENI inputs can be daisy-chained to generate power sequencing. The PGOOD output is pulled high when the voltage at SENSE is above V_{REF} (800mV typ). Connect a resistive divider from the power-supply output voltage to SENSE to AGND to set the power-good threshold. See Figure 1 and the *Typical Operating Circuits*.

Error Amplifier

The output of the internal error amplifier (COMP) is available for frequency compensation (see the *Compensation Design Guidelines* section). The inverting input is FB; the output is COMP. The error amplifier has an 80dB open-loop gain and a 2.5MHz GBW product. See the *Typical Operating Characteristics* section for the Open-Loop Gain and Phase vs. Frequency graph.

PWM Comparator

An internal ramp is compared against the output of the error amplifier to generate the PWM signal. The amplitude of the ramp, V_{RAMP}, is 1.8V.

Output Short-Circuit Protection (Hiccup Mode)

The current-limit circuit employs a lossless valley current-limiting algorithm that uses the MOSFET's on-resistance as the current-sensing element. Once the high-side MOSFET turns off, the voltage across the low-side MOSFET is monitored. If the voltage across the low-side MOSFET ($R_{DS(ON)}$ x $I_{INDUCTOR}$) does not exceed the current-limit threshold, the high-side MOSFET turns on normally at the start of the next cycle. If the voltage across the low-side MOSFET exceeds the current-limit threshold just before the beginning of a new PWM cycle, the controller skips that cycle. During severe overload or short-circuit conditions, the switching frequency of the device appears to decrease because the on-time of the low-side MOSFET extends beyond a clock cycle.

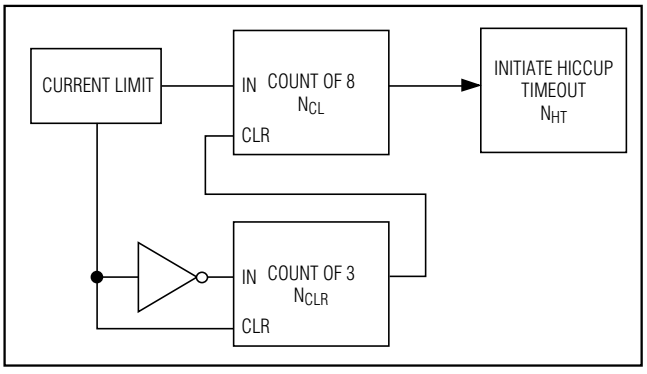


Figure 2. Hiccup-Mode Block Diagram

If the current-limit threshold is exceeded for eight cumulative clock cycles (N_{CL}), the device shuts down (both DH and DL are pulled low) for 512 clock cycles (hiccup timeout) and restarts with a soft-start sequence. If three consecutive cycles pass without a current-limit event, the count of N_{CL} is cleared (Figure 2). Hiccup mode protects against continuous output short circuit.

Thermal-Overload Protection

The MAX5950 features an integrated thermal-overload protection with temperature hysteresis. Thermal-overload protection limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +135°C, an internal thermal sensor shuts down the device, turning off the power MOSFETs and allowing the die to cool. After the die temperature falls by +15°C, the part restarts with a soft-start sequence.

Hot-Swap Controller Design Procedures

Setting the Undervoltage Lockout

Connect an external resistive divider from IN to HUVLO to AGND to override the internal hot-swap UVLO divider. The rising threshold at HUVLO is set to 1.220V with 120mV hysteresis. First, select the HUVLO to AGND resistor (R2), then calculate the resistor from IN to HUVLO (R1) using the following equation:

$$R1 = R2 \times \left[\frac{V_{IN}}{V_{HUVLO}} - 1 \right]$$

where V_{IN} is the input voltage at which the hot-swap controller needs to turn on, V_{HUVLO} = 1.220V, and R2 is chosen to be less than 20kΩ (see Figure 3).

Leave HUVLO unconnected for the default hot-swap UVLO threshold. In this case, an internal voltage-divider monitors the supply voltage at IN and allows startup when IN rises above 7V (typ).

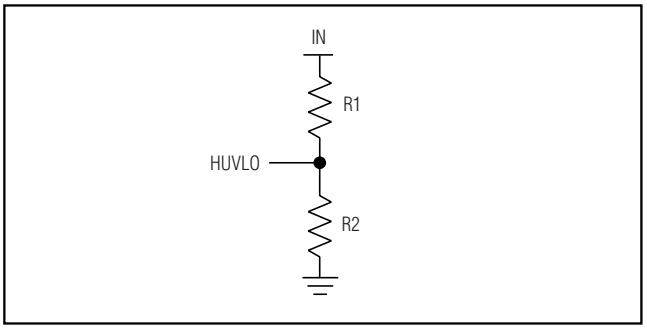


Figure 3. External Hot-Swap UVLO Divider

n-Channel MOSFET Selection

Select the external n-channel MOSFET according to the application's current level. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. High $R_{DS(ON)}$ can cause output ripple if the board has pulsing loads. Determine the device power-rating requirement to accommodate a short circuit on the board at startup.

In normal operation, the product of pass MOSFET $R_{DS(ON)}$ and I_{IN} should not exceed the circuit-breaker threshold (600mV).

PWM Controller Design Procedures

Setting the Undervoltage Lockout

Connect an external resistive divider from PWM_IN to PUVLO to AGND to override the internal PWM UVLO divider. The rising threshold at PUVLO is set to 1.220V with 120mV hysteresis. First, select the PUVLO to AGND resistor (R2), then calculate the resistor from PWM_IN to PUVLO (R1), using the following equation:

$$R1 = R2 \times \left[\frac{V_{PWM\_IN}}{V_{PUVLO}} - 1\right]$$

where V_{PWM_IN} is the input voltage at which the converter needs to turn on, V_{PUVLO} = 1.220V, and R2 is chosen to be less than 20kΩ (see Figure 4).

Leave PUVLO unconnected for the default PWM UVLO threshold. In this case, an internal voltage-divider monitors the supply voltage at PWM_IN and allows startup when PWM_IN rises above 7V (typ).

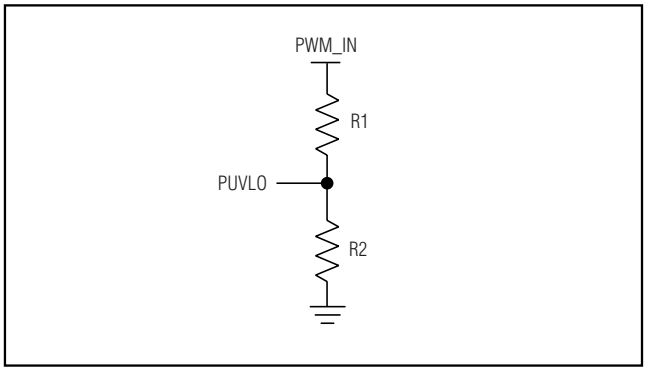


Figure 4. External PWM UVLO Divider

Setting the Output Voltage

Connect a resistive divider from OUT to FB to AGND to set the output voltage. First, calculate the resistor from OUT to FB using the guidelines in the *Compensation Design Guidelines* section. Once R3 is known, calculate R4 using the following equation:

$$R4 = \frac{R3}{\left[\frac{V_{OUT}}{V_{FB}} - 1\right]}$$

where V_{FB} = 0.8V.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX5950: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value. A lower inductance value minimizes size and cost and improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output voltage ripple for the same output capacitor. A higher inductance increases efficiency by reducing the ripple current; however, resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. A good rule of thumb is to choose ΔI_{P-P} equal to 30% of the full-load current. Calculate the inductor using the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_{P-P}}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency is programmable between 100kHz and 1000kHz (see the *Oscillator/Synchronization Input (SYNCIN)/ Synchronization Output (SYNCOUT)* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worst at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output current ripple is acceptable. The inductor saturation current (I_{SAT}) is also important to avoid runaway current during continuous output short-circuit conditions. Select an inductor with an I_{SAT} specification higher than the maximum peak current.

Input-Capacitor Selection

The discontinuous input current of the buck converter causes large input ripple currents, therefore the input capacitor must be carefully chosen to withstand the input ripple current and maintain the input voltage ripple within design requirements. The total voltage ripple is the sum of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor), which peaks at the end of the ON cycle. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN} = \frac{I_{LOAD(MAX)} \times \left(\frac{V_{OUT}}{V_{PWM\_IN}}\right)}{\Delta V_Q \times f_{SW}}$$

where

$$\Delta I_{P-P} = \frac{(V_{PWM\_IN} - V_{OUT}) \times V_{OUT}}{V_{PWM\_IN} \times f_{SW} \times L}$$

$I_{LOAD(MAX)}$ is the maximum output current, ΔI_{P-P} is the peak-to-peak inductor current, and f_{SW} is the switching frequency.

The MAX5950 includes UVLO hysteresis to avoid possible unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. When the input voltage is near the UVLO, additional input capacitance helps avoid possible undershoot below the UVLO threshold during transient loading.

Output-Capacitor Selection

The allowed output voltage ripple and the maximum deviation of the output voltage during load steps determine the required output capacitance and its ESR. The output ripple is mainly composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the voltage drop across the equivalent series resistance (ESR) of the output capacitor). The equations for calculating the peak-to-peak output voltage ripple are:

$$\Delta V_Q = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$\Delta V_{ESR} = ESR \times \frac{\Delta I_{P-P}}{2}$$

ΔV_{ESR} and ΔV_Q are not directly additive since they are out of phase from each other. If using ceramic capacitors, which generally have low ESR, ΔV_Q dominates. If using electrolytic capacitors, ΔV_{ESR} dominates.

The allowable deviation of the output voltage during load transients also affects the choice of output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter (see the *Compensation Design Guidelines* section). The resistive drop across the output capacitor's ESR, the drop across the capacitor's ESL, and the capacitor discharge cause a voltage droop during the load step. Use a combination of low-ESR tantalum/aluminum electrolyte and ceramic capacitors for better load transient and voltage-ripple performance. Surface-mount capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output-voltage deviation below the tolerable limits of the electronics being powered. Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$COUT = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, and $t_{RESPONSE}$ is the response time of the controller.

Setting the Current Limit

Connect a 25kΩ to 175kΩ resistor, R_{ILIM}, from ILIM to AGND to program the valley current-limit threshold from 50mV to 350mV. ILIM sources 20µA out to R_{ILIM}. The resulting voltage divided by 10 is the valley current-limit threshold.

The MAX5950 uses a valley current-sense method for current limiting. The voltage drop across the low-side MOSFET due to its on-resistance is used to sense the inductor current. The voltage drop across the low-side MOSFET at the valley point and at $I_{LOAD(MAX)}$ is:

$$V_{VALLEY} = R_{DS(ON)}(T) \times \left(I_{LOAD(MAX)} - \frac{\Delta I_{P-P}}{2}\right)$$

$R_{DS(ON)}$ is the on-resistance of the low-side MOSFET, which is temperature dependent, $I_{LOAD(MAX)}$ is the maximum DC load current, and ΔI_{P-P} is the peak-to-peak inductor current.

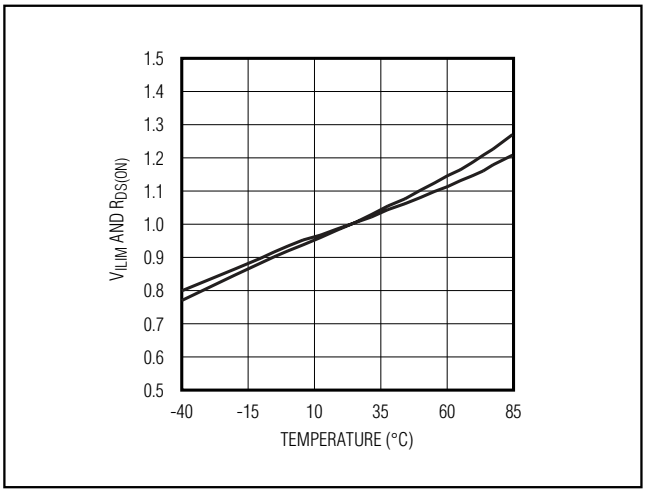


Figure 5. Current-Limit Trip Point and $R_{DS(ON)}$ vs. Temperature

The 20µA current source, ILIM reference current, has a temperature coefficient of 3333ppm/°C. This allows the valley current-limit threshold:

$$\frac{R_{ILIM} \times 20\mu A\ (T)}{10}$$

to track and compensate for the increase in the synchronous MOSFET's $R_{DS(ON)}$ with increasing temperature range. MOSFETs typically have a temperature coefficient of 3000ppm/°C to 7000ppm/°C. Refer to the MOSFET data sheet for a device-specific temperature coefficient.

At a given temperature, the calculated V_{VALLEY} must be less than the minimum valley current-limit threshold specified.

Figure 5 illustrates the effect of the MAX5950 ILIM reference current temperature coefficient to compensate for the variation of the MOSFET $R_{DS(ON)}$ over the operating junction temperature range.

Power-MOSFET Selection

When selecting MOSFETs, consider the total gate charge, $R_{DS(ON)}$, power dissipation, the maximum drain-to-source voltage, package thermal impedance, and desired current limit. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications. The average gate-drive current from the MAX5950's output is proportional to the frequency and gate charge required to drive the MOSFET. The power dissipated in the MAX5950 is proportional to the input voltage and the average drive current (see the *Power Dissipation* section).

Compensation Design Guidelines

The MAX5950 uses a voltage-mode control scheme that regulates the output voltage by comparing the error amplifier output (COMP) with an internal ramp to produce the required duty cycle. The output lowpass LC filter creates a double pole at the resonant frequency, which has a gain drop of -40dB/decade. The compensation network must compensate for this gain drop and phase shift to achieve a stable closed-loop system.

The basic regulator loop consists of a power modulator, an output feedback divider, and a voltage-error amplifier. The power modulator has a DC gain set by V_{IN}/V_{RAMP}, with a double pole and a single zero set by the output inductance (L), the output capacitance (C_{OUT}), and its ESR. Below are equations that define the power modulator:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}$$

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

$$f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

The switching frequency is programmable between 100kHz and 1000kHz by an external resistor at RT. The crossover frequency (f_C), which is the frequency when the closed-loop gain is equal to unity, should be set to f_{SW} / 10 or f_{GBW} / 25, whichever is lower.

The error amplifier must provide a gain-and-phase boost to compensate for the rapid gain-and-phase loss from the LC double pole. This is accomplished by utilizing type 3 compensation (see Figures 6 and 7) that introduces two zeros and three poles into the control loop. The error amplifier has a low-frequency pole (f_{P1}) at the origin; two zeros at:

$$f_{Z1} = \frac{1}{2\pi \times R5 \times C7}$$

and

$$f_{Z2} = \frac{1}{2\pi \times R3 \times C6}$$

and higher frequency poles at:

$$f_{P2} = \frac{1}{2\pi \times R6 \times C6}$$

and

$$f_{P3} = \frac{1}{2\pi \times R5 \times C8}$$

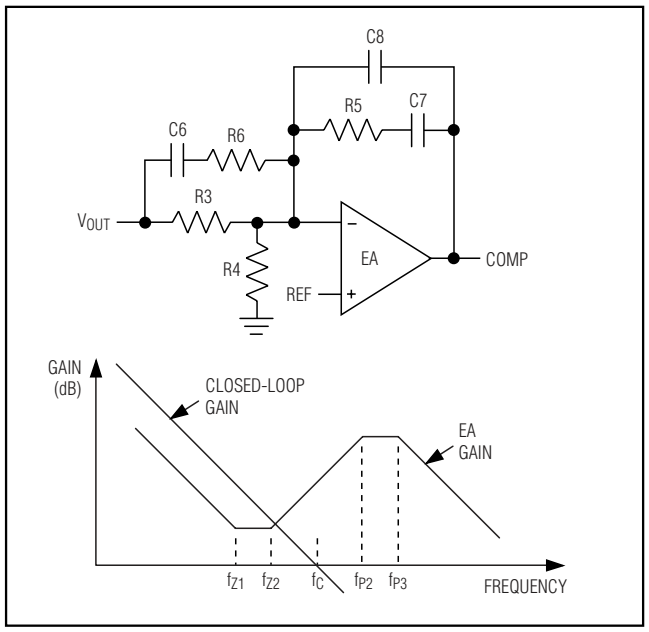


Figure 6. Error Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot) for Ceramic Capacitors

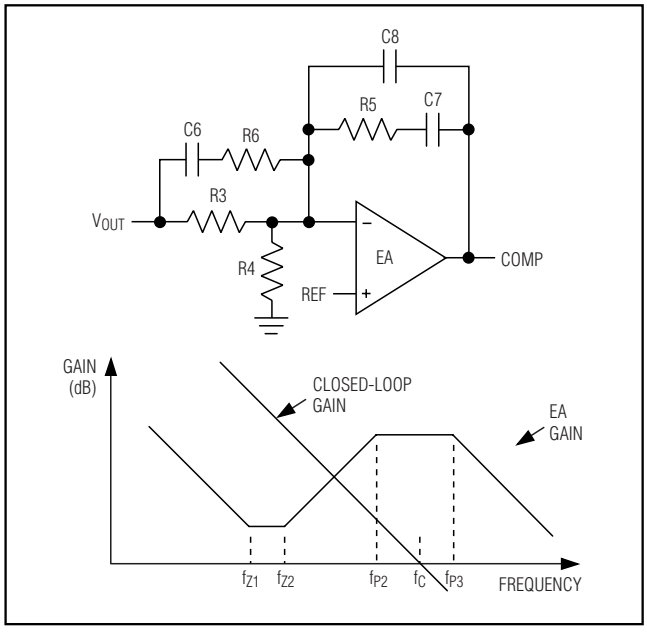


Figure 7. Error-Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot) for Higher ESR Output Capacitors

Compensation when $f_C < f_{ZESR}$

Figure 6 shows the error-amplifier feedback, as well as its gain response for circuits that use low-ESR output capacitors (ceramic). In this case, f_C occurs before f_{ZESR}.

f_{Z1} is set to 0.5 x f_{LC} and f_{Z2} is set to f_{LC} to compensate for the gain-and-phase loss due to the double pole. Choose the inductor (L) and output capacitor (C_{OUT}) as described in the *Inductor Selection* and *Output-Capacitor Selection* sections.

Pick a value for feedback resistor R5 in Figure 6 (values between 1kΩ and 10kΩ are adequate). C7 is then calculated as:

$$C7 = \frac{1}{2\pi \times 0.5 \times f_{LC} \times R5}$$

f_C occurs between f_{Z2} and f_{P2}. The circuit is implemented with C7 > C8 and R3 > R6, in which case the error-amplifier gain (G_{EA}) at f_C is due primarily to C6 and R5. Therefore:

$$G_{EA(fc)} = 2\pi \times f_C \times C6 \times R5$$

The modulator gain at f_C is:

$$G_{MOD(fC)} = \frac{G_{MOD(DC)}}{(2\pi)^2 \times L \times C_{OUT} \times f_C{}^2}$$

Since $G_{EA(fC)} \times G_{MOD(fC)} = 1$, C6 is calculated by:

$$C6 = \frac{f_C \times L \times C_{OUT} \times 2\pi}{R5 \times G_{MOD(DC)}}$$

R3 is then calculated as:

$$R3 \approx \frac{1}{2\pi \times f_{LC} \times C6}$$

f_{P2} is set at 1/2 the switching frequency (f_{SW}). R6 is then calculated by:

$$R6 = \frac{1}{2\pi \times C6 \times 0.5 f_{SW}}$$

f_{P3} is set at 5xf_C. Therefore, C8 is calculated as:

$$C8 = \frac{1}{2\pi \times R5 \times 5 \times f_C}$$

Compensation when $f_C > f_{ZESR}$

For larger ESR capacitors such as tantalum and aluminum electrolytic, f_{ZESR} can occur before f_C. If $f_C > f_{ZESR}$, f_C occurs between f_{P2} and f_{P3}. f_{Z1} and f_{Z2} remain the same as before; however, f_{P2} is now set equal to f_{ZESR}. The output capacitor's ESR zero fre-

quency is higher than f_{LC}, but lower than the closed-loop crossover frequency. The equations that define the error amplifier's poles and zeroes (f_{Z1}, f_{Z2}, f_{P1}, f_{P2}, and f_{P3}) are the same as before. However, f_{P2} is now lower than the closed-loop crossover frequency. Figure 7 shows the error-amplifier feedback, as well as its gain response for circuits that use higher ESR output capacitors (tantalum, aluminum electrolytic, etc.)

Pick a value for feedback resistor R5 in Figure 7 (values between 1kΩ and 10kΩ are adequate). C7 is then calculated as:

$$C7 = \frac{1}{2\pi \times 0.5 \times f_{LC} \times R5}$$

The circuit is implemented with C7 >> C8 and R3 >> R6, in which case the error-amplifier gain between f_{P2} and f_{P3} is approximately equal to:

$$\frac{R5}{R6}$$

The modulator gain at f_C is:

$$G_{MOD(fC)} = \frac{G_{MOD(DC)}}{(2\pi)^2 \times L \times C_{OUT} \times f_C{}^2}$$

Since $G_{EA(fC)} \times G_{MOD(fC)} = 1$, R6 can then be calculated as:

$$R6 \approx \frac{R5 \times G_{MOD(DC)}}{(2\pi)^2 \times L \times C_{OUT} \times f_C{}^2}$$

f_{P2} is set to f_{ZESR}. C6 is then calculated as:

$$C6 = \frac{C_{OUT} \times ESR}{R6}$$

R3 is then calculated as:

$$R3 \approx \frac{1}{2\pi \times f_{LC} \times C6}$$

f_{P3} is set at $5 \times f_C$. Therefore, C8 is calculated as:

$$C8 = \frac{1}{2\pi \times R5 \times 5 \times f_C}$$

Hot-Swap Controller Applications Information

Additional External Gate Capacitance

External capacitance can be added from the gate of the external MOSFET to AGND to reduce the dv/dt of the PWM controller input voltage (V_{PWM_IN}), decreasing the hot-swap inrush current. Add a 10kΩ resistor in series with the added gate capacitor to prevent degrading the device turn-off response to a fault condition.

Layout Considerations

To take advantage of the switch response time to an output fault condition, it is important to keep all traces as short as possible and to maximize the high-current trace width to reduce the effect of undesirable parasitic inductance. Use a ground plane to minimize impedance and inductance. Minimize the trace length that connects to IN and HSENSE (< 10mm), and ensures accurate current sensing with Kelvin connections.

When the output is short circuited, the voltage drop across the external MOSFET becomes large. Hence, the power dissipation in the switch increases, as does the die temperature. An efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the top side of the board.

PWM Controller Applications Information

Power Dissipation

The 32-pin TQFN thermally enhanced package can dissipate 2.7W. Calculate power dissipation in the MAX5950 as a product of the input voltage and the total REG output current (I_{REG}). I_{REG} includes quiescent current (I_Q) and gate-drive current (I_{DREG}):

$$P_D = V_{IN} \times I_{REG}$$

$$I_{REG} = I_Q + [f_{SW} \times (Q_{G1} + Q_{G2})]$$

where Q_{G1} and Q_{G2} represent the total gate charge of the low-side and high-side external MOSFETs, f_{SW} is the switching frequency of the converter, and I_Q is the quiescent current of the device at the switching frequency.

Use the following equation to calculate the maximum power dissipation (P_{DMAX}) in the chip at a given ambient temperature (T_A):

$$P_{DMAX} = 34.5 \times (150 - T_A) \text{.....mW}$$

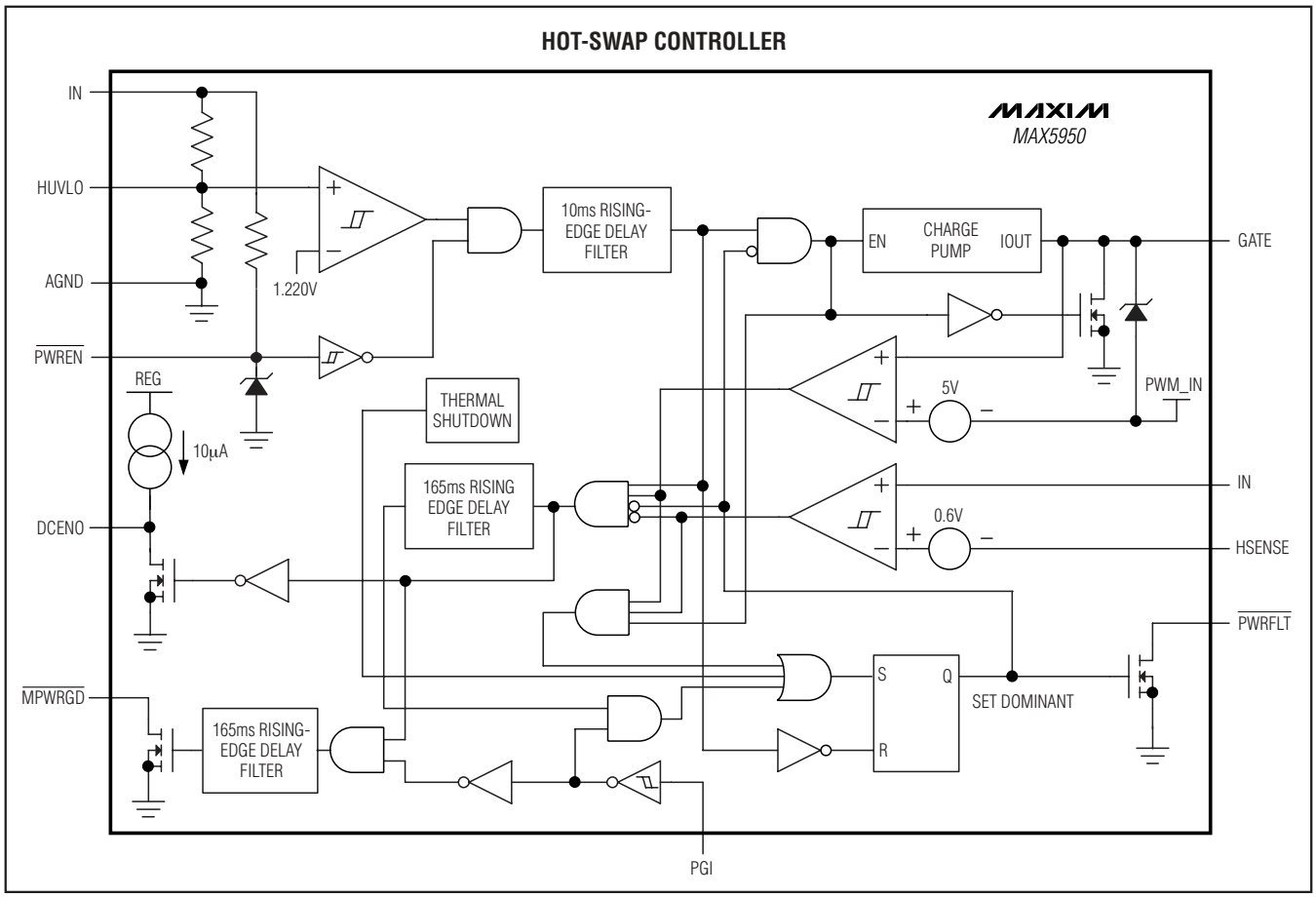
12V PWM Controller with Hot-Swap

PC Board Layout Guidelines

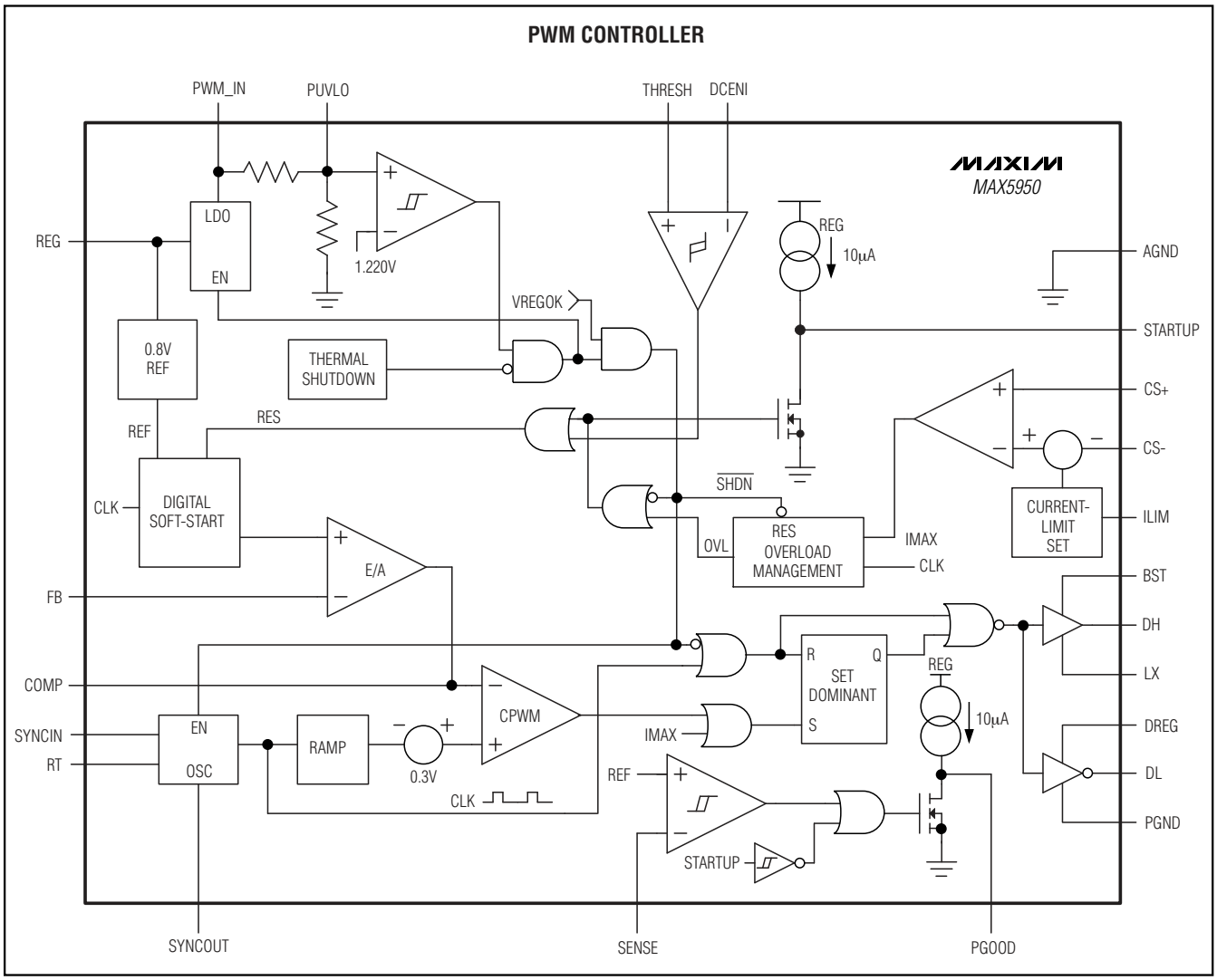
Use the following guidelines to layout the switching voltage regulator:

1) Place the PWM_IN and DREG bypass capacitors close to the MAX5950 PGND pin. Place the REG bypass capacitor close to the AGND pin.
2) Minimize the area and length of the high-current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep short the current loop formed by the lower switching MOSFET, inductor, and output capacitor.
4) Keep AGND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
5) Run current-sense lines CS+ and CS- close to each other to minimize the loop area.
6) Avoid long traces between the REG/DREG bypass capacitors, driver output of the MAX5950, MOSFET gates, and PGND. Minimize the loop formed by the REG bypass capacitors, bootstrap diode, bootstrap capacitor, the MAX5950, and upper MOSFET gate.
7) Place the bank of output capacitors close to the load.
8) Distribute the power components evenly across the board for proper heat dissipation.
9) Provide enough copper area at and around the switching MOSFETs and the inductor to aid in thermal dissipation.
10) Use 2oz copper to keep the trace inductance and resistance to a minimum. Thin copper PC boards can compromise efficiency since high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.

Simplified Block Diagrams

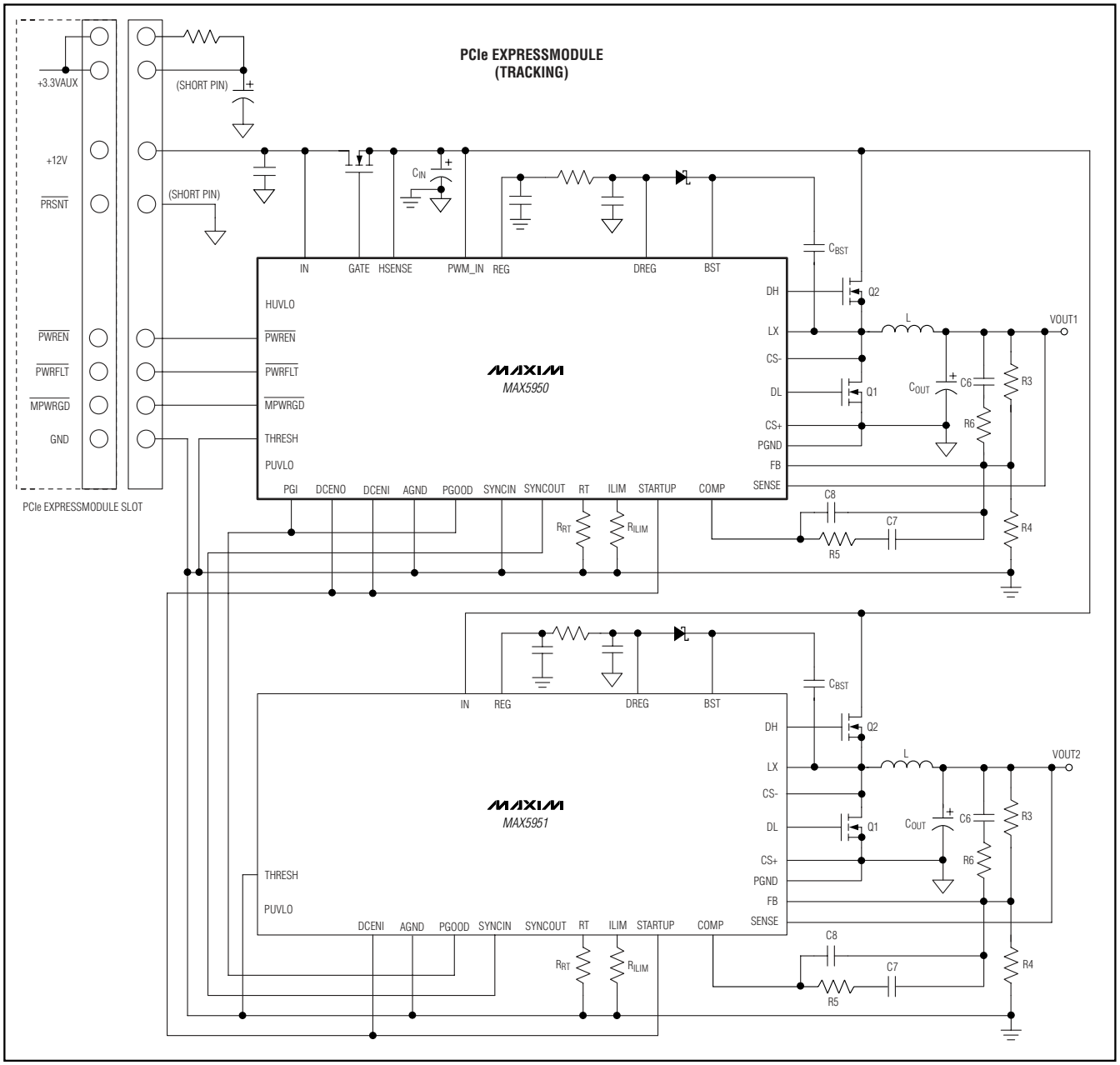


Simplified Block Diagrams (continued)

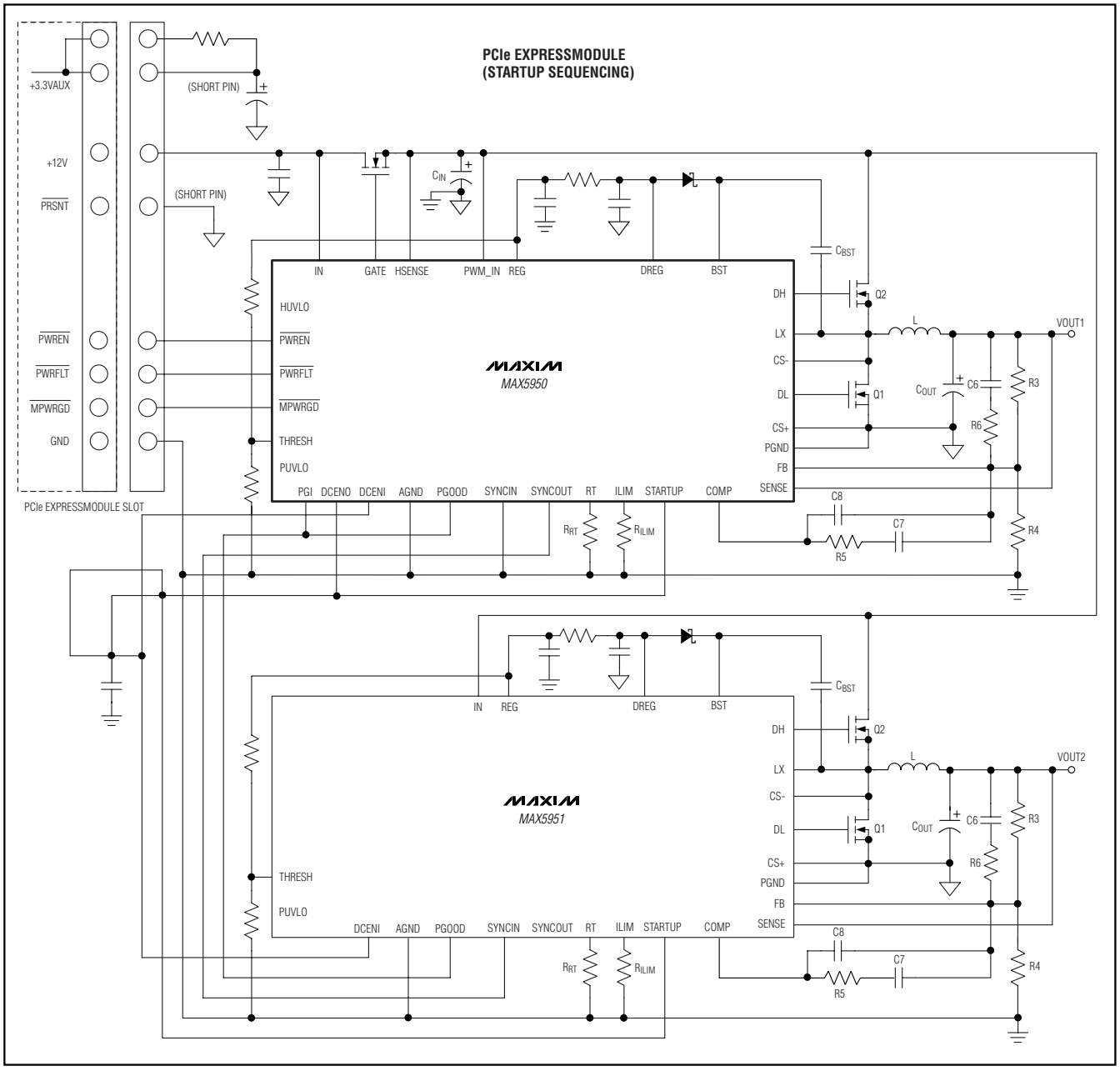


12V PWM Controller with Hot-Swap

Typical Operating Circuits

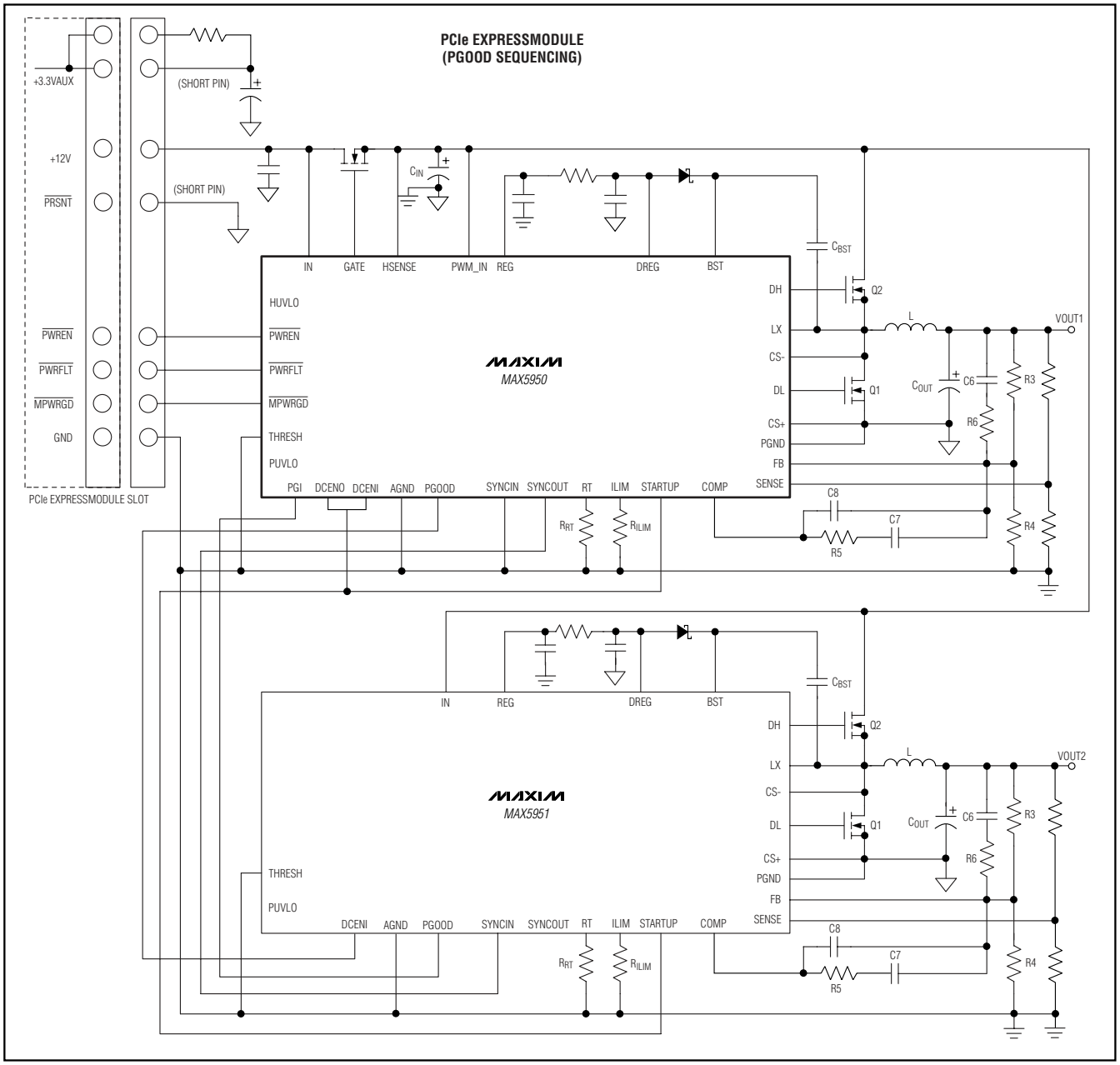


Typical Operating Circuits (continued)

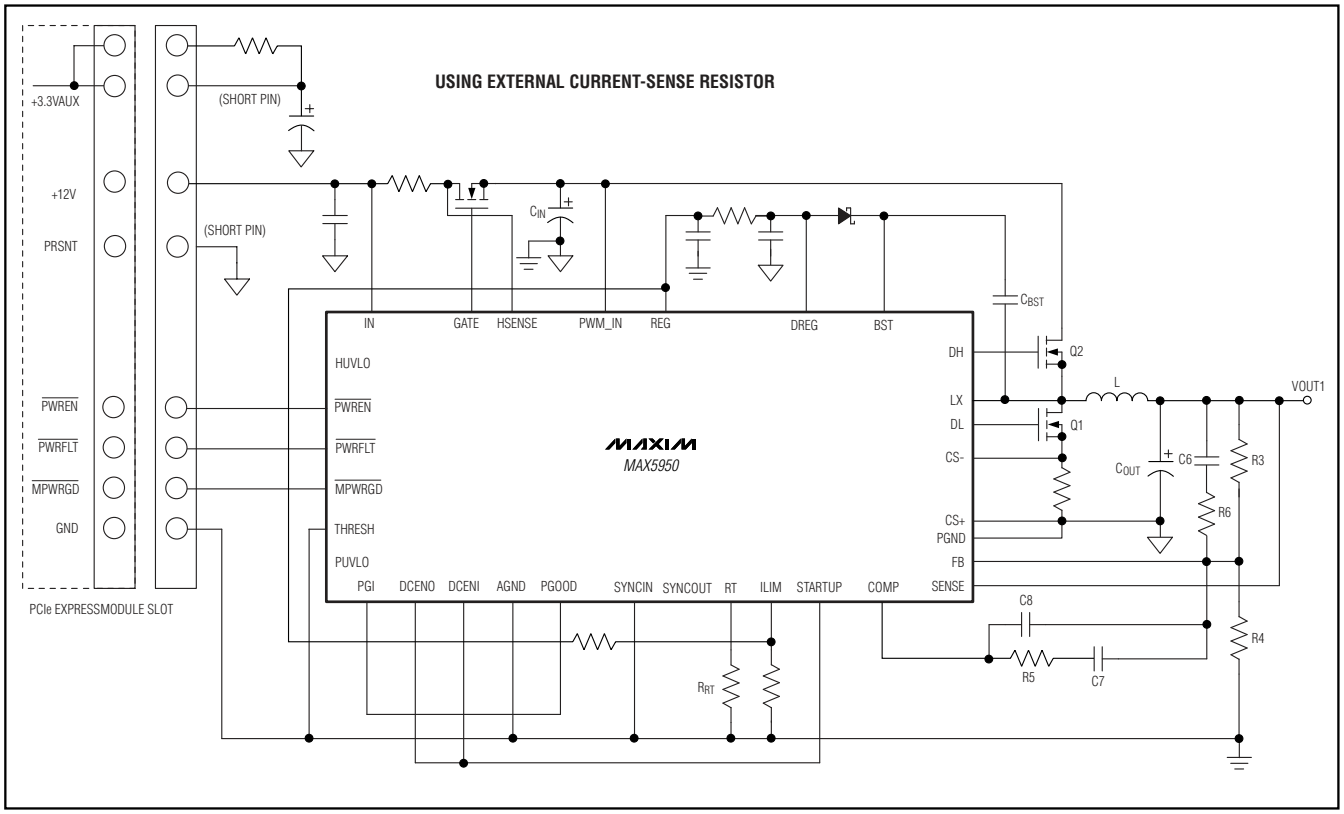


12V PWM Controller with Hot-Swap

Typical Operating Circuits (continued)



Typical Operating Circuits (continued)



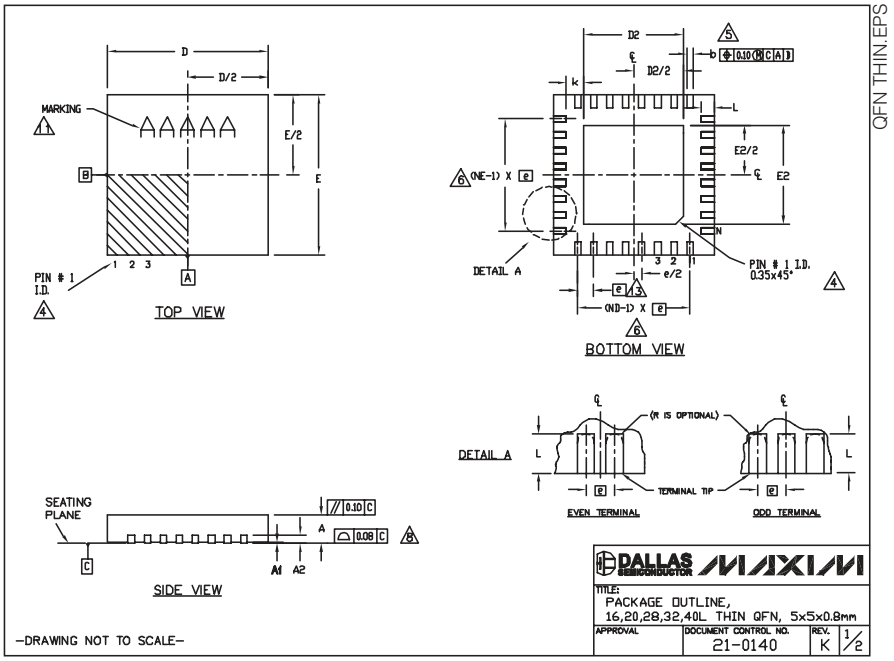
Chip Information

PROCESS: BiCMOS

12V PWM Controller with Hot-Swap

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. K | 1/2

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