BUF802 Wide-Bandwidth, 2.3 nV/√Hz, High-Input Impedance Buffer

1 Features

- Large-signal bandwidth (1 V_{PP}): 3.1 GHz
- Slew rate: 7000 V/µs
- Input voltage noise: 2.3 nV/√Hz
- 1% settling time: 0.7 ns
- Input-impedance: 50 GΩ || 2.4 pF
- Capable of driving 50 Ω load
- Adjustable quiescent current for power and performance trade-off
- Integrated input and output clamp with fast overdrive recovery
- Voltage supply: ±4.5 V to ±6.5 V

2 Applications

- Oscilloscope front-end
- High-frequency data acquisition
- High input-impedance and high slew rate T&M systems
- Oscilloscope encoder and front-end add-on cards
- Active probes
- Non-destructive testing (NDT)

3 Description

The BUF802 device is an open-loop, unity gain buffer with a JFET-input stage that offers low-noise, high-impedance buffering for data acquisition system (DAQ) front-ends. The BUF802 supports DC to 3.1 GHz of bandwidth while offering excellent distortion and noise performance across the frequency range.

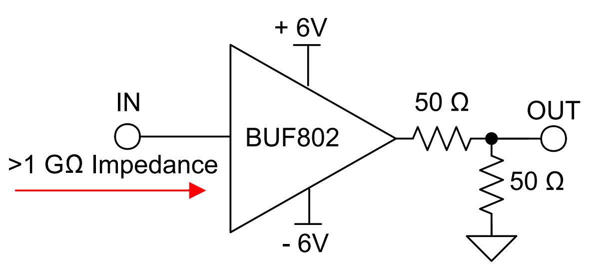
The BUF802 may be used in a composite loop with a precision amplifier in applications where higher precision performance is required. The BUF802 uses an innovative architecture to simplify the design of high-precision, wide-bandwidth composite loops.

The BUF802 features an adjustable quiescent current pin, which enables designers to trade bandwidth and distortion for a lower quiescent current, thus making the part suitable across a wide-frequency range. The BUF802 has integrated input and output clamps to protect the device and its subsequent signal-chain from overdrive voltages.

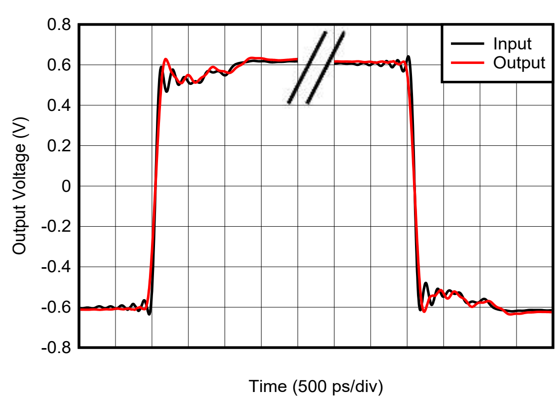
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BUF802	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Impedance Transformation Circuit Using BUF802



Transient Response

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4 Revision History

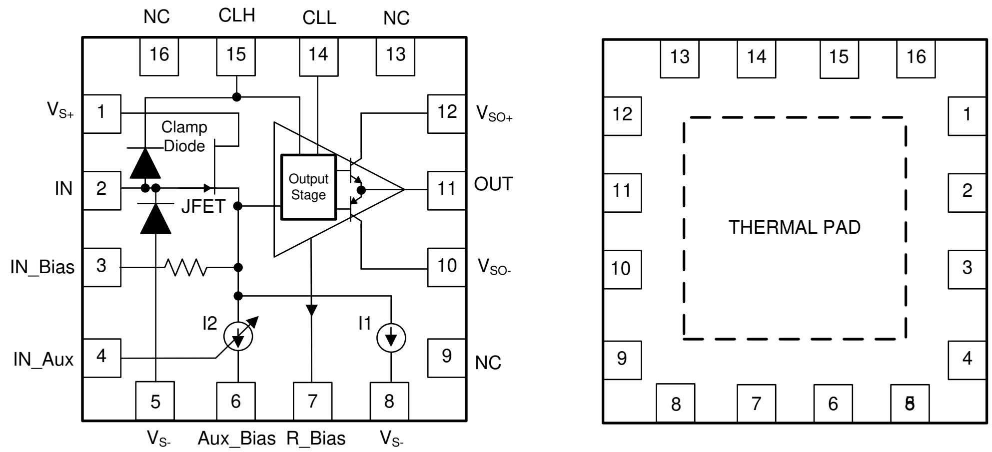
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2022) to Revision C (March 2022)	Page
• Relaxed DC Gain specifications	5
• Relaxed DC Gain specifications	7

Changes from Revision A (December 2021) to Revision B (February 2022)	Page
• Updated the *Application and Implementation* section	24

Changes from Revision * (June 2021) to Revision A (December 2021)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions



*Pin 5 and Pin 8 Internally Shorted

Figure 5-1. RGT Package, 16-Pin VQFN (Top View and Bottom View)

Table 5-1. Pin Functions

PIN		TYPE[4]	Operating Mode[1] [2]	DESCRIPTION
NAME	NO.			
Aux_Bias	6	P	CL	Connect to V_{S-} to enable control of OUT through the In_Aux.
CLH	15	I	BF, CL	Input pin for setting positive clamp voltage
CLL	14	I	BF, CL	Input pin for setting negative clamp voltage
IN	2	I	BF, CL	Signal input
In_Aux	4	I	CL	Auxiliary input for controlling OUT through an external amplifier.
In_Bias	3	I	CL	JFET biasing pin
NC	16, 13, 9	—	—	Do not connect.
OUT	11	O	BF, CL	Signal output
R_Bias	7	I	BF, CL	Output stage bias current setting pin
V_{S+}	1	P	BF, CL	Positive power supply connection for Input Stage.
V_{S-}	5, 8	P	BF, CL	Negative power supply connection for Input Stage. Pin 5 and Pin 8 are internally shorted.
V_{SO+} [3]	12	P	BF, CL	Positive power supply connection for Output Stage.
V_{SO-} [3]	10	P	BF, CL	Negative power supply connection for Output Stage.
Thermal Pad		—	—	The thermal pad is electrically isolated from the die and pins. Connect the thermal pad to any potential.

(1) See Section 8.4 for more information on *Buffer Mode (BF)* and *Composite Loop Mode (CL)* functional modes.
(2) Pins specified as *CL* should only be used when operating in *Composite Loop Mode* and left floating when operating in *Buffer Mode*.
(3) V_{SO} and V_S should be tied to the same potential since they are internally connected to each other through back-to-back diodes.
(4) I = input, O= output, P= power, NC = no connect.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
$V_S = (V_{S+}) – (V_{S–})$	Supply voltage[2]		14	V
$V_{SO} = (V_{SO+}) – (V_{SO–})$				
	Maximum dV_S/dT for supply turn-on and turn-off		0.1	V/µs
IN	Input	(V_{S+}) to $(V_{S–}) – 0.5$		V
CLH	Positive Clamp	Mid-supply	V_{S+}	
CLL	Negative Clamp	$V_{S–}$	Mid-supply	V
	Input Clamp Diode		100	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) V_{SO} and V_S should be tied to the same potential. V_{SO} and V_S are internally connected to each other through back to back diodes.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_S = (V_{S+}) – (V_{S–})$[1]	Dual Supply voltage	±4.5	±5	±6.5	V
	Single Supply voltage	9	10	13	V
T_A	Ambient temperature	–40	25	85	°C

(1) BUF802 can be used with any possible combination of V_{S+} and $V_{S–}$, provided the recommended operating condition is not exceeded

6.4 Thermal Information

THERMAL METRIC[1]		BUF802 RGT (VQFN) 16 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	53	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	61	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	27	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	2.7	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	27	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	13	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics: Wide Bandwidth Mode

at T_A = 25°C, V_S = ±6V, R_L = 100 Ω || 400 fF, R_S = 25 Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and V_{S-} respectively, Wide Bandwidth Mode unless otherwise specified (R_Bias = 17.8 kΩ)

PARAMETER		Test Condition		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-Signal Bandwidth	V_{OUT} = 100 mV_{PP}			3.1		GHz
LSBW	Large-Signal Bandwidth	V_{OUT} = 1 V_{PP}			3.1		GHz
		V_{OUT} = 2 V_{PP}			1.6		GHz
	Bandwidth for 0.1 dB flatness	V_{OUT} = 1 V_{PP}			0.6		GHz
	Bandwidth for -1 dB flatness	V_{OUT} = 1 V_{PP}			1.8		GHz
	Bandwidth for -2 dB flatness	V_{OUT} = 1 V_{PP}	R_L = 50 Ω		2.4		GHz
SR	Slew rate	V_{OUT} = 1.2-V step, V_{IN}-SR = 13000 V/µs			7000		V/µs
	Rise and fall time	V_{OUT} = 1.2-V step (10% to 90%)			0.16		ns
		V_{OUT} = 0.25-V step (10% to 90%)			0.15		ns
	Settling time to 0.1%	V_{OUT} = 1.2-V step, V_{IN}-SR = 13000 V/µs			1.3		ns
	Settling time to 1%	V_{OUT} = 1.2-V step, V_{IN}-SR = 13000 V/µs			0.7		ns
e_n	Voltage noise	1/f corner			18		kHz
		f = 100 MHz in *BF Mode* and *CL Mode*			2.3		nV/√Hz
i_n	Current noise	f = 10 kHz			1.5		pA/√Hz
HD2/HD3	Harmonic distortion	V_{OUT} = 2 V_{PP}	f = 500 MHz		–68/–58		dBc
		V_{OUT} = 1 V_{PP}	f = 1 GHz		–55/–59		dBc
		V_{OUT} = 1 V_{PP}	f = 2 GHz		–45/–49		dBc
		V_{OUT} = 1 V_{PP}	f = 2 GHz, R_L = 50 Ω		–43/–41		dBc
DC PERFORMANCE							
V_{OS}	Input offset voltage	V_{OUT} – V_{IN}			–600	–800	mV
		T_A = –40℃ to 85℃				–900	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40℃ to 85℃			±700	±1330	µV/℃
I_B	Input bias current				3	25	pA
		T_A = –40℃ to 85℃				220	pA
I_{AB}	Auxiliary Input bias current				44	140	µA
		T_A = –40℃ to 85℃				200	µA
G	DC Gain	V_{OUT} = ± 0.5 V	R_L = 200 Ω	0.97	0.978	0.99	V/V
		V_{OUT} = ± 0.5 V	R_L = 100 Ω	0.96	0.971	0.98	V/V
		V_{OUT} = ± 0.5 V	R_L = 50 Ω	0.95	0.961	0.97	V/V
		V_{OUT} = ± 0.5 V ,T_A = –40℃ to 85℃	R_L = 200 Ω	0.97		0.99	V/V
		V_{OUT} = ± 0.5 V ,T_A = –40℃ to 85℃	R_L = 100 Ω	0.96		0.98	V/V
		V_{OUT} = ± 0.5 V ,T_A = –40℃ to 85℃	R_L = 50 Ω	0.94		0.97	V/V

6.5 Electrical Characteristics: Wide Bandwidth Mode (continued)

at T_A = 25°C, V_S = ±6V, R_L = 100 Ω || 400 fF, R_S = 25 Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and V_{S-} respectively, Wide Bandwidth Mode unless otherwise specified (R_Bias = 17.8 kΩ)

PARAMETER		Test Condition		MIN	TYP	MAX	UNIT
INPUT							
Z_{IN}	Input impedance	f = 100 MHz			50 || 2.4		GΩ || pF
	Input Clamp current rating	Continous Current Rating			100		mA
	V_{CLH} range[(1)]			0		V_{S+}	V
	V_{CLL} range[(1)]			V_{S-}		0	V
	CLH Clamping Time	Time taken to clamp V_{OUT} to V_{CLH} during overdrive			0.2		nsec
	CLL Clamping Time	Time taken to clamp V_{OUT} to V_{CLL} during overdrive			0.2		nsec
	Input Voltage Range	THD = – 40 dBc	f = 500 MHz		4.5		V_{PP}
			f = 1 GHz		2.1		
			f = 2 GHz		1.2		
OUTPUT							
	Output Swing	T_A = 25°C		V_{S+} – 1.9			V
						V_{S-} + 3.4	
		T_A = –40°C to 85°C		V_{S+} – 2.0			
						V_{S-} + 3.4	
Z_O	Output impedance	f = 100 MHz			1.2		Ω
AUXILIARY INPUT							
G_{AUX}	V_{OUT} to In_Aux Gain			0.18	0.26		V/V
			T_A = –40°C to 85°C		0.23		V/V
	Default voltage at In_Aux			V_{S-} + 2.3	V_{S-} + 3	V_{S-} + 3.8	V
	In_Aux Input Voltage Range			V_{S-} + 1.0		V_{S-} + 5.0	V
	V_{OUT} to In_Aux Bandwidth				800		MHz
	RHF	Resistance between In_Bias to JFET source			100		kΩ
POWER SUPPLY							
V_S	Operating voltage range			±4.5		±6.5	V
I_Q	Quiescent current	I_{OUT} = 0 (R_bias = 17.8 kΩ)			34	37	mA
			T_A = –40°C to 85°C		35.5		
			CL Mode enabled		36	40	
PSRR	Power-supply rejection ratio	PSRR at 100 kHz on V_{S+}			49		dB
		PSRR at 100 kHz on V_{S-}			38		

(1) The 0-V limits are for bipolar and balanced power supplies. For other supply configurations mid-supply will set the minimum limit for V_{CLH} and maximum limit for V_{CLL}

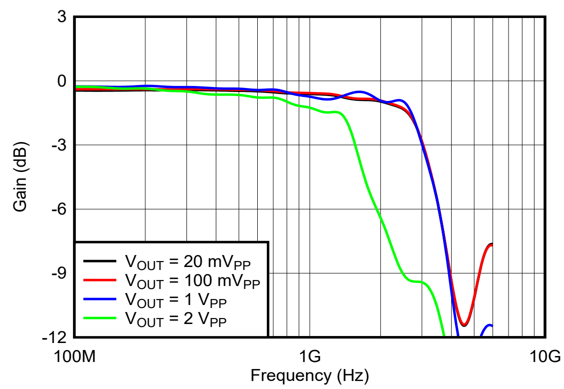
6.6 Electrical Characteristics: Low Quiescent Current Mode

at T_A = 25°C, V_S = ±6 V, R_L = 100 Ω || 400 fF. R_S = 25 Ω, V_{OCM} = 0 V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$ respectively, Low Quiescent Current Mode unless otherwise specified (R_Bias = 35.7 kΩ)

PARAMETER		Test Condition		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-Signal Bandwidth	V_{OUT} = 100 mV_{PP}			2.6		GHz
LSBW	Large-Signal Bandwidth	V_{OUT} = 1 V_{PP}			2		GHz
		V_{OUT} = 2 V_{PP}			0.7		GHz
	Bandwidth for 0.1 dB flatness	V_{OUT} = 1 V_{PP}			0.45		GHz
	Bandwidth for -1 dB flatness	V_{OUT} = 1 V_{PP}			1.4		GHz
SR	Slew rate	V_{OUT} = 1.2-V step, V_{IN}-SR = 13000 V/µs			5500		V/µs
	Rise and fall time	V_{OUT} = 1.2-V step (10% to 90%)			0.3		ns
		V_{OUT} = 0.25-V step (10% to 90%)			0.16		ns
	Settling time to 0.1%	V_{OUT} = 1.2-V step, V_{IN}-SR = 13000 V/µs			1.4		ns
	Settling time to 1%	V_{OUT} = 1.2-V step, V_{IN}-SR = 13000 V/µs			0.8		ns
e_n	Voltage noise	1/f corner			10		kHz
		f = 100 MHz			2.2		nV/√Hz
i_n	Current noise	f = 10 kHz			1.5		pA/√Hz
HD2/HD3	Harmonic distortion	V_{OUT} = 2 V_{PP}	f = 500 MHz		–35/–32		dBc
		V_{OUT} = 1 V_{PP}	f = 100 MHz		–80/–77		dBc
			f = 500 MHz		–56/–54		dBc
DC PERFORMANCE							
G	DC Gain	V_{OUT} = ± 0.5 V	R_L = 200 Ω	0.96	0.975	0.99	V/V
			R_L = 100 Ω	0.95	0.963	0.98	V/V
		V_{OUT} = ± 0.5 V ,T_A = –40℃ to 85℃	R_L = 200 Ω	0.96		0.99	V/V
			R_L = 100 Ω	0.95		0.98	V/V
INPUT							
	CLH Clamping Time	Time taken to clamp V_{OUT} to V_{CLH} during overdrive			0.3		nsec
	CLL Clamping Time	Time taken to clamp V_{OUT} to V_{CLL} during overdrive			0.7		nsec
OUTPUT							
Z_O	Output impedance	f = 100 MHz			1.2		Ω
POWER SUPPLY							
V_S	Operating voltage range			±4.5		±6.5	V
I_Q	Quiescent current	I_{OUT} = 0 (R_bias = 35.7 kΩ)			21	24	mA
			T_A = –40℃ to 85℃		22		mA

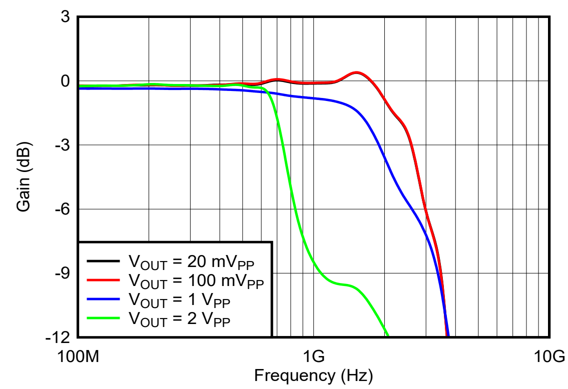
6.7 Typical Characteristics

At T_A = 25°C, V_S = ±6 V, R_L = 100 Ω || 400 fF, R_S = 25 Ω, V_{OCM} = 0 V (mid-supply), V_{OUT} = 1 V_{PP}, CLH and CLL tied to V_{S+} and V_{S-} respectively, Wide Bandwidth Mode unless otherwise specified (R_Bias = 17.8 kΩ).



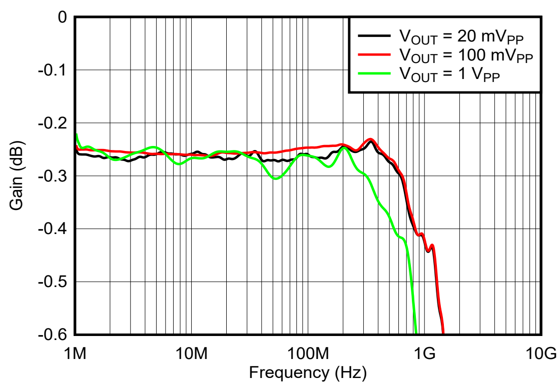
Wide Bandwidth Mode

Figure 6-1. Frequency Response vs Output Voltage



Low Quiescent Current Mode

Figure 6-2. Frequency Response vs Output Voltage



Wide Bandwidth Mode

Figure 6-3. Frequency Response vs Output Voltage, 0.1 dB Flatness

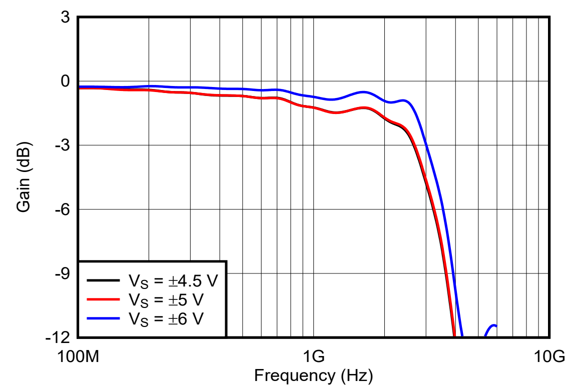


Figure 6-4. Frequency Response vs Supply Voltage

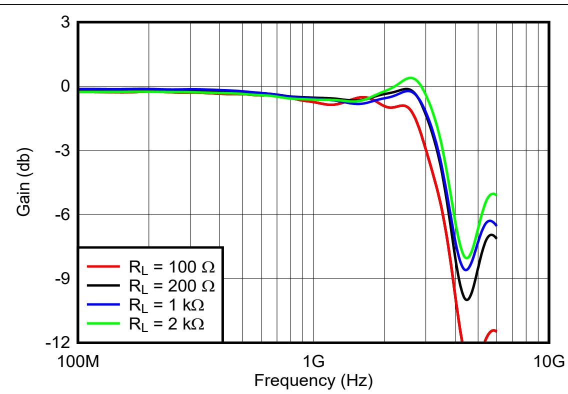


Figure 6-5. Frequency Response vs Output Load

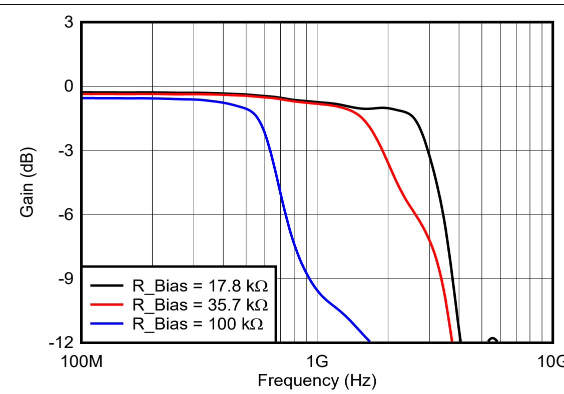


Figure 6-6. Frequency Response vs R_Bias Resistance

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = ±6 V, R_L = 100 Ω || 400 fF, R_S = 25 Ω, V_{OCM} = 0 V (mid-supply), V_{OUT} = 1 V_{PP}, CLH and CLL tied to V_{S+} and V_{S-} respectively, Wide Bandwidth Mode unless otherwise specified (R_Bias = 17.8 kΩ).

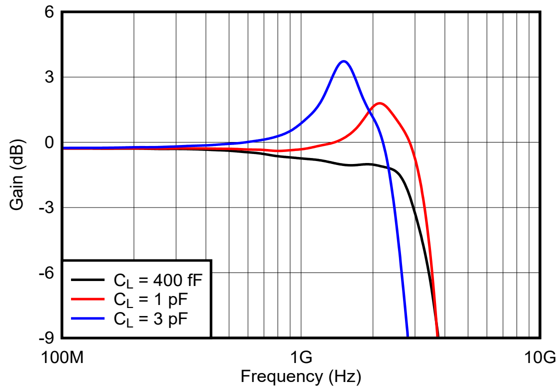


Figure 6-7. Frequency Response vs Capacitive Load

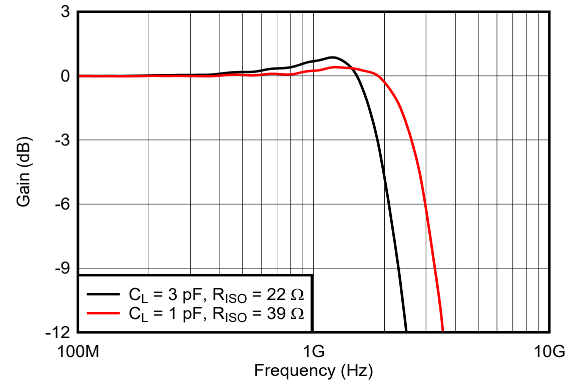
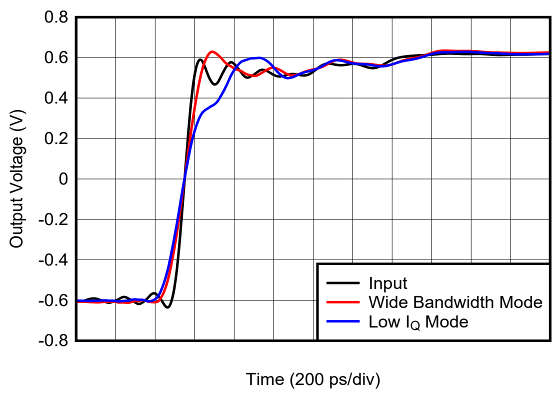
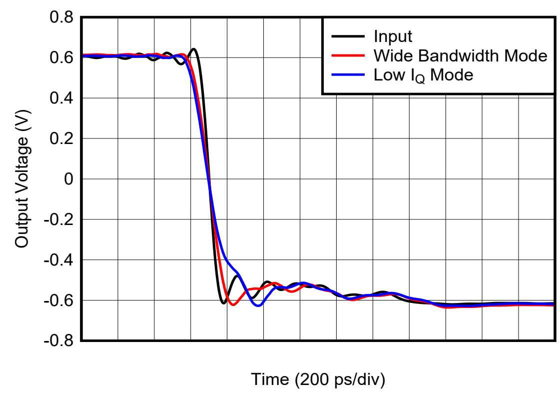


Figure 6-8. Frequency Response vs Cap Load with Recommended R_{ISO}



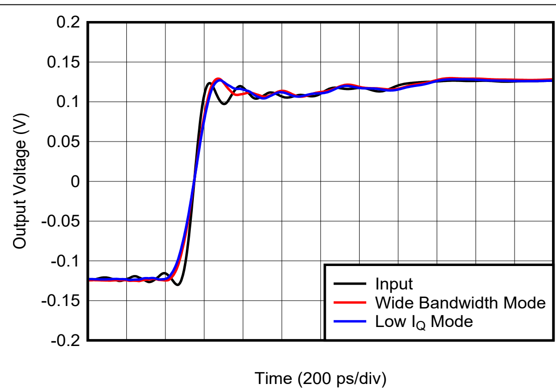
Rising edge, V_{OUT} = 1.2 V_{PP}

Figure 6-9. Large-Signal Transient Response



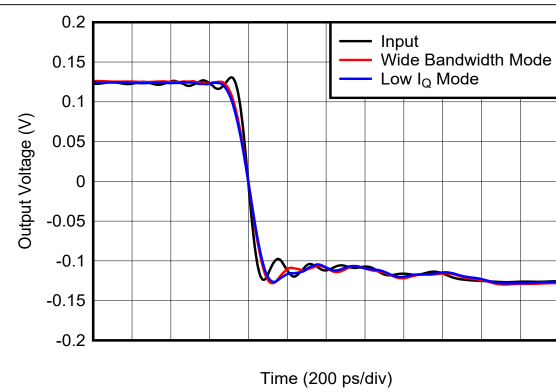
Falling edge, V_{OUT} = 1.2 V_{PP}

Figure 6-10. Large-Signal Transient Response



Rising edge, V_{OUT} = 250 mV_{PP}

Figure 6-11. Small-Signal Transient Response

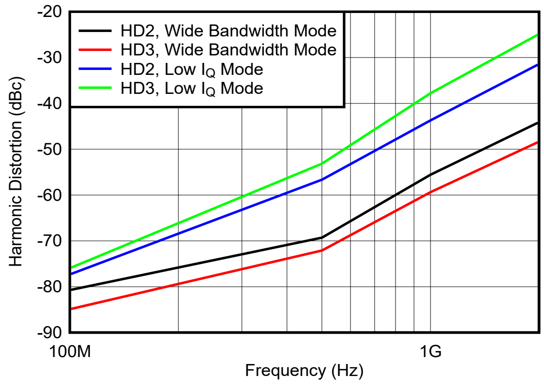


Falling edge, V_{OUT} = 250 mV_{PP}

Figure 6-12. Small-Signal Transient Response

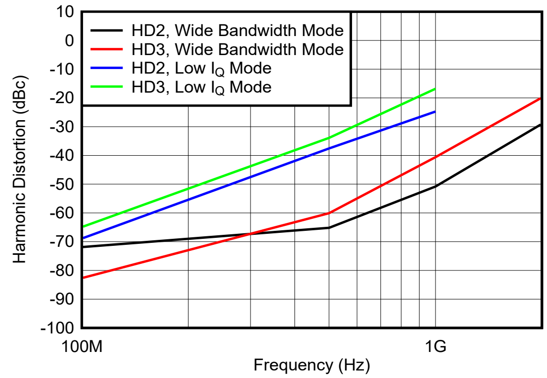
6.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = ±6 V, R_L = 100 Ω || 400 fF, R_S = 25 Ω, V_{OCM} = 0 V (mid-supply), V_{OUT} = 1 V_{PP}, CLH and CLL tied to V_{S+} and V_{S-} respectively, Wide Bandwidth Mode unless otherwise specified (R_Bias = 17.8 kΩ).



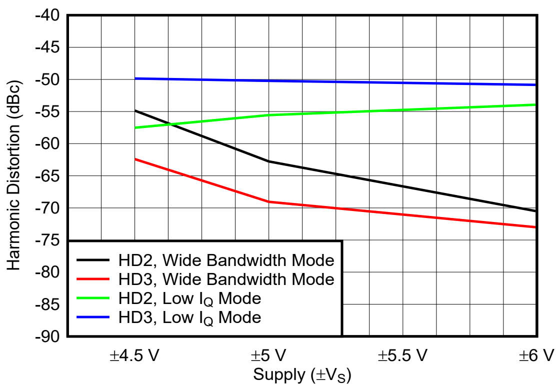
V_{OUT} = 1 V_{PP}

Figure 6-13. Harmonic Distortion vs Frequency



V_{OUT} = 2 V_{PP}

Figure 6-14. Harmonic Distortion vs Frequency



f = 500 MHz

Figure 6-15. Harmonic Distortion vs Supply Voltage

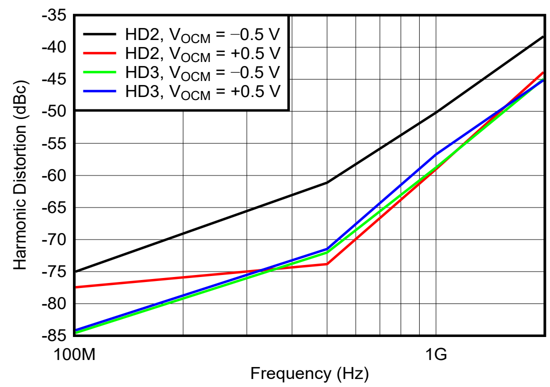
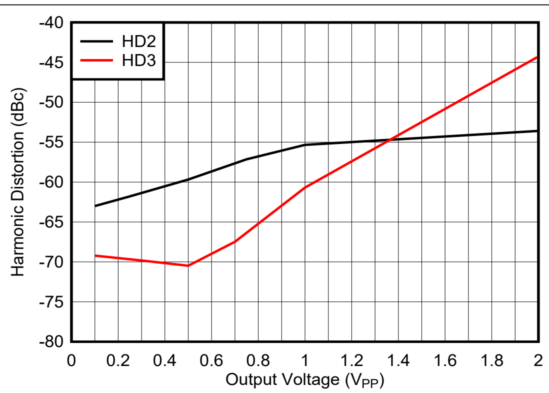
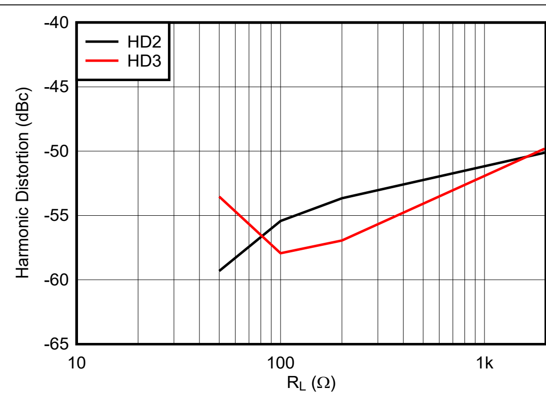


Figure 6-16. Harmonic Distortion vs Output Common Mode Voltage



f = 1 GHz

Figure 6-17. Harmonic Distortion vs Output Voltage



f = 1 GHz

Figure 6-18. Harmonic Distortion vs Output Load

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = ±6 V, R_L = 100 Ω || 400 fF, R_S = 25 Ω, V_{OCM} = 0 V (mid-supply), V_{OUT} = 1 V_{PP}, CLH and CLL tied to V_{S+} and V_{S-} respectively, Wide Bandwidth Mode unless otherwise specified (R_Bias = 17.8 kΩ).

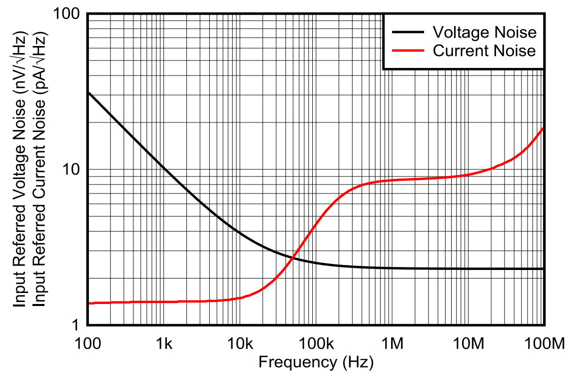
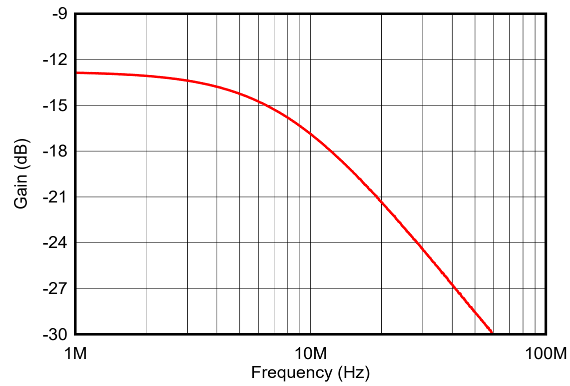


Figure 6-19. Voltage and Current Noise Density vs Frequency



With RC pole of 2 kΩ and 10 pF at IN_Aux pin

Figure 6-20. Auxiliary Path Frequency Response

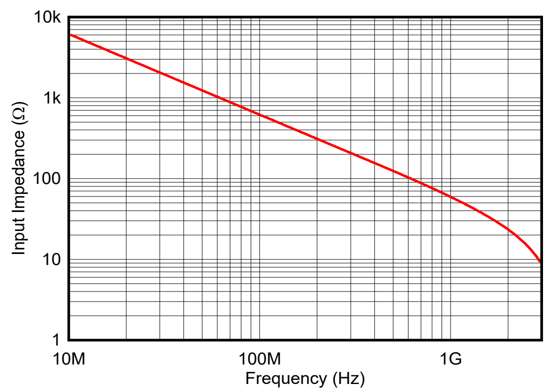


Figure 6-21. Input Impedance vs Frequency

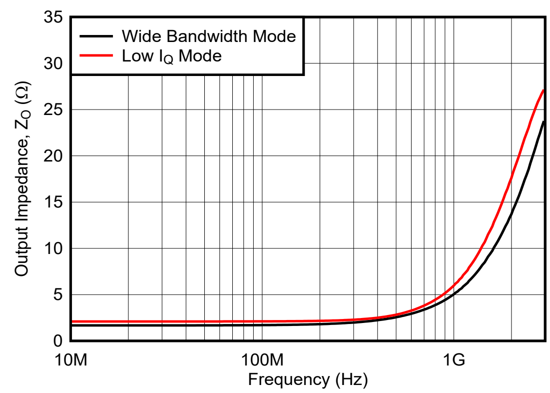
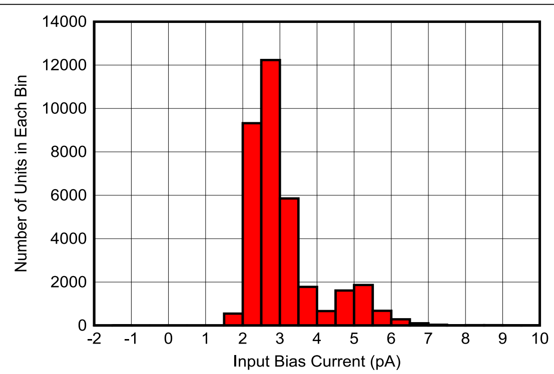
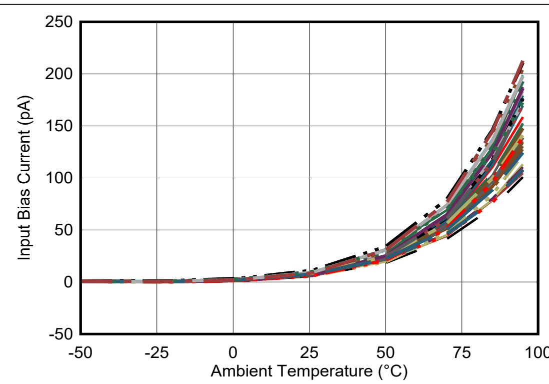


Figure 6-22. Output Impedance vs Frequency



μ = 3.1 pA, σ = 1.03 pA

Figure 6-23. Input Bias Current Distribution



40 units

Figure 6-24. Input Bias Current vs Temperature

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = ±6 V, R_L = 100 Ω || 400 fF, R_S = 25 Ω, V_{OCM} = 0 V (mid-supply), V_{OUT} = 1 V_{PP}, CLH and CLL tied to V_{S+} and V_{S-} respectively, Wide Bandwidth Mode unless otherwise specified (R_Bias = 17.8 kΩ).

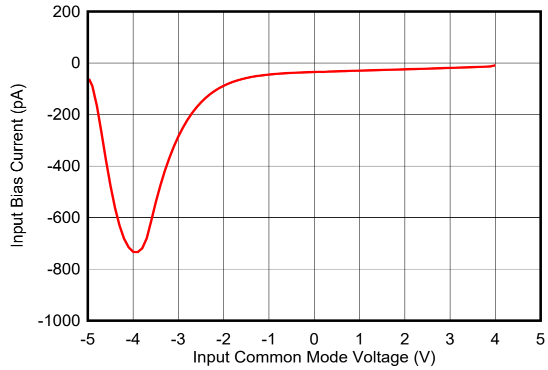
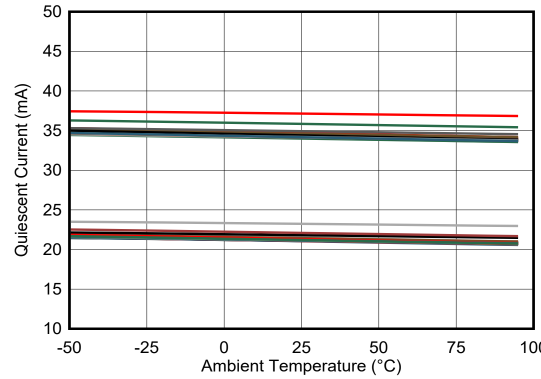
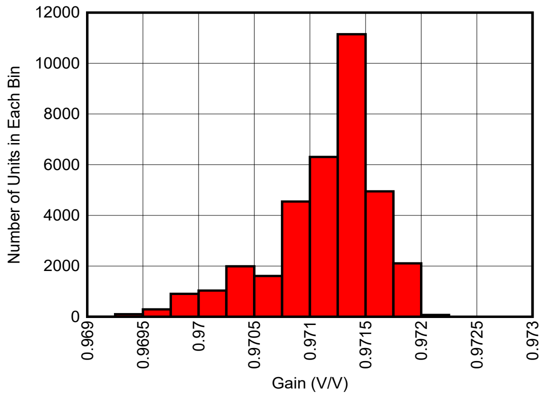


Figure 6-25. Input Bias Current vs Input Common Mode Voltage



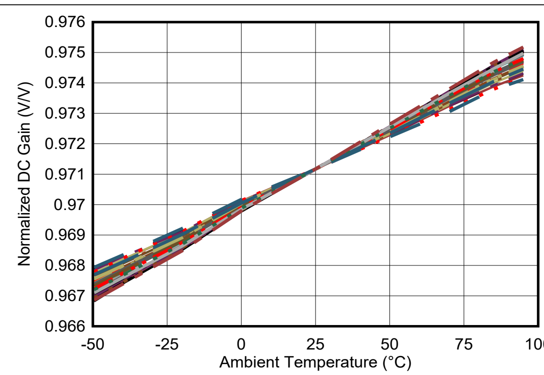
Wide Bandwdith Mode and Low I_Q Mode

Figure 6-26. Quiescent Current vs Temperature



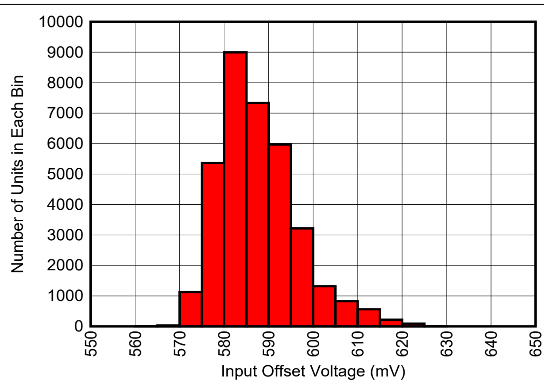
μ = 0.971 V/V, σ = 0.000485 V/V

Figure 6-27. DC Gain Histogram



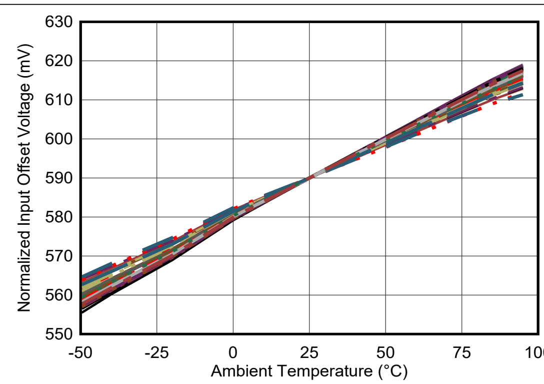
Normalized to 25 °C values, 40 units

Figure 6-28. DC Gain vs Temperature



μ = 587.668 mV, σ = 8.80778 mV

Figure 6-29. Offset Voltage Histogram



Normalized to 25 °C values, 40 units

Figure 6-30. Offset Voltage vs Temperature

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = ±6 V, R_L = 100 Ω || 400 fF, R_S = 25 Ω, V_{OCM} = 0 V (mid-supply), V_{OUT} = 1 V_{PP}, CLH and CLL tied to V_{S+} and V_{S-} respectively, Wide Bandwidth Mode unless otherwise specified (R_Bias = 17.8 kΩ).

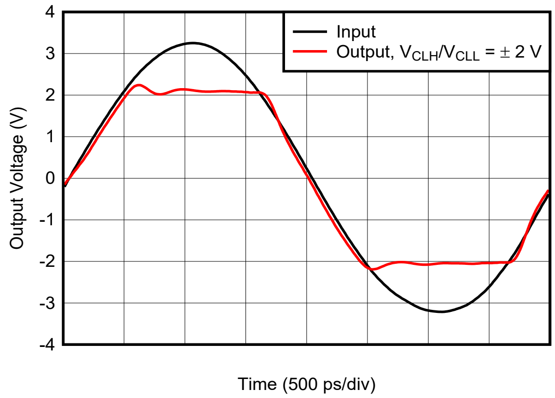


Figure 6-31. Transient Clamp Response

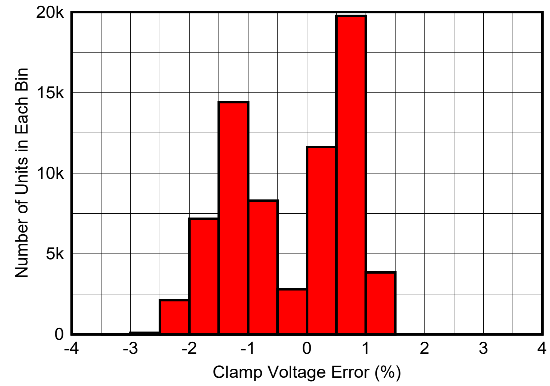


Figure 6-32. Clamp Voltage Error Histogram

7 Parameter Measurement Information

Figure 7-1 through Figure 7-3 show the various test setup configurations for the BUF802.

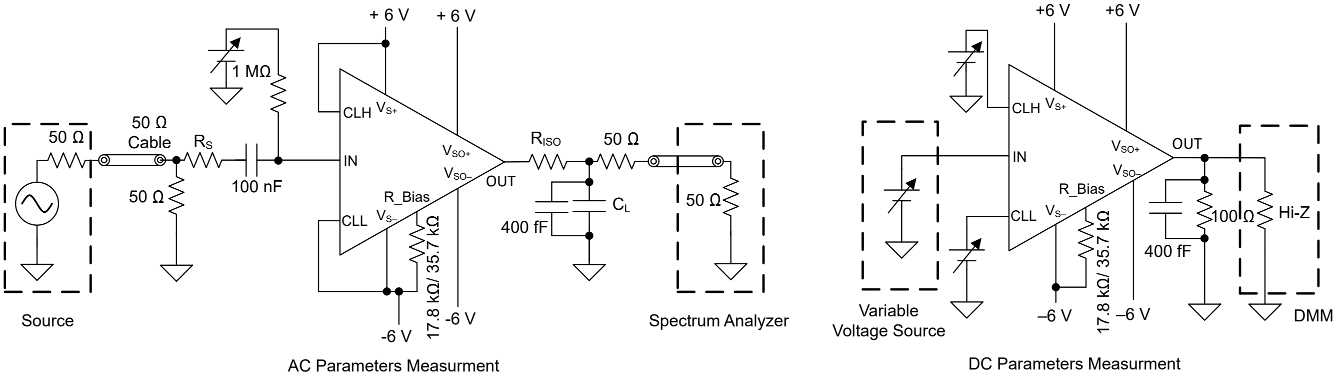


Figure 7-1. Main Path Electrical Characteristics Measurement

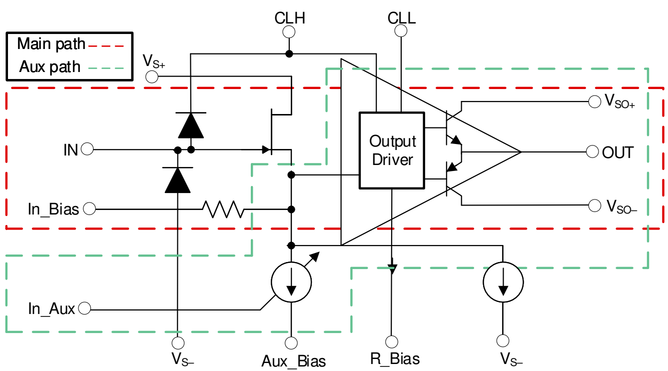


Figure 7-2. Main Path and Auxiliary Path

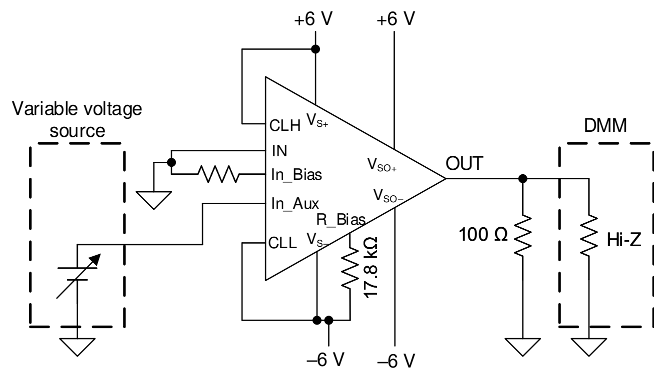


Figure 7-3. Auxiliary Path Electrical Characteristics Measurement

Figure 7-2 shows the two inputs for BUF802 (IN and In_Aux) which control the output. The IN pin controls the output of BUF802 through the Main Path, whereas the In_Aux pin controls the output through the Auxiliary Path. Either the Main Path or the Auxiliary Path, can be used to steer the output. The electrical characteristics of the Main Path and the Auxiliary Path is specified in Section 6.7.

8 Detailed Description

8.1 Overview

The BUF802 device is a high input-impedance, open-loop buffer that can be used in signal acquisition front-end applications. The BUF802 can be used as a standalone buffer, *Buffer Mode (BF Mode)*, or in a composite loop with a precision amplifier, *Composite Loop Mode (CL Mode)*, to achieve DC precision and a wide, large-signal bandwidth. The low output impedance and high output current drive strength enables the BUF802 to drive loads as high as 50 Ω. The BUF802 comes with adjustable quiescent current to customize system level power and performance trade-off.

8.2 Functional Block Diagram

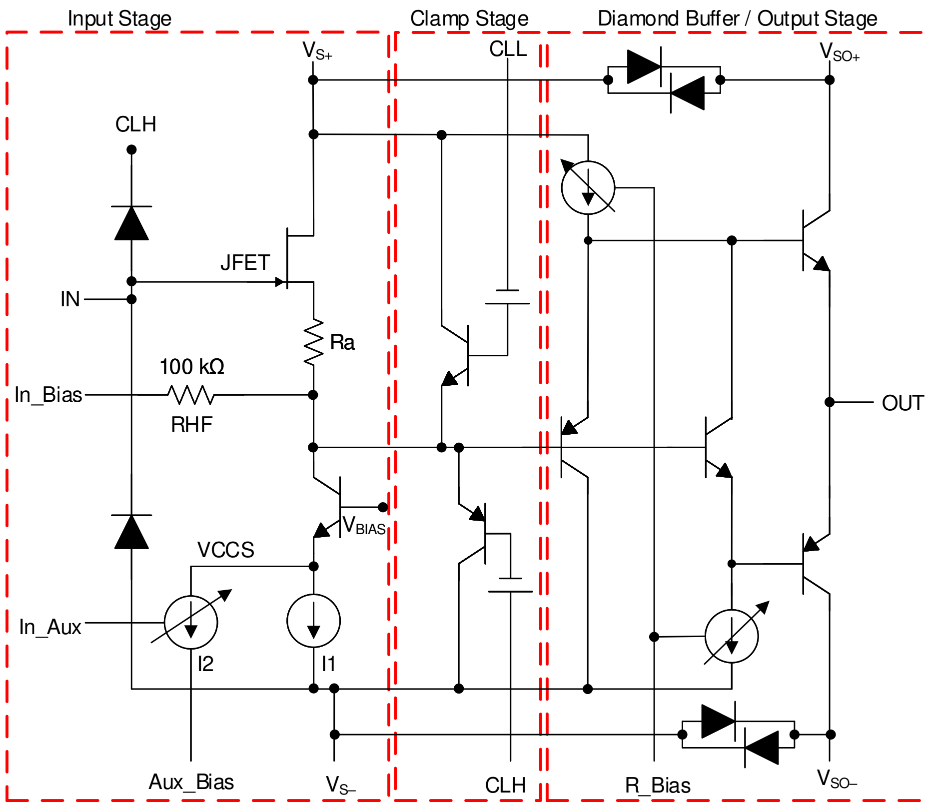


Figure 8-1. Functional Block Diagram

Figure 8-1 shows an overview of the internal structure of the BUF802. The internal schematic of the BUF802 can be divided into the following 3 parts:

- **Input Stage**, which consists of a low noise JFET and its biasing circuitry. The Input Stage can be configured in two modes, *BF Mode* and *CL Mode*. Choosing one of the two modes affects the circuit operation of the Input Stage. The Clamp and Output Stage operation are unaffected by the mode selection. Section 8.4 describes the two modes in greater detail.
- **Clamp Stage**, which provides the following functions:
  1. Protects the input of the BUF802 against large input signal transients through diode clamps to V_{S-} and CLH respectively.
  2. Ensures the output voltage of the BUF802 does not exceed the voltage at the CLH and CLL.
- **Output Stage**, which tracks the JFET source voltage and is optimized to drive a 50 Ω and 100 Ω load while maintaining signal fidelity.

8.3 Feature Description

8.3.1 Input and Output Over-Voltage Clamp

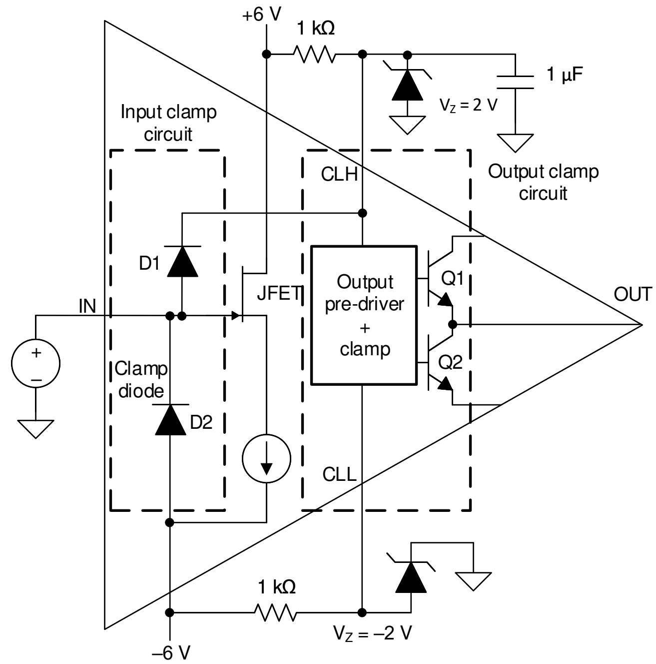


Figure 8-2. Internal Input and Output Over-Voltage Clamp

The BUF802 device integrates an input and output clamp circuit. The input clamp protects the BUF802 from large input transients and the output clamp protects the subsequent stages from being overdriven.

- **Input Clamp Circuit**:
  – Figure 8-2 shows the input of the BUF802 tied to pins CLH and V_{S-} through two internal clamp diodes, D1 and D2. The diodes are rated for 100 mA of continuous current but can withstand much higher transient currents. If the JFET input voltage exceeds the voltage at CLH or V_{S-}, the diodes get forward biased, clamping the JFET to CLH and V_{S-}. A 1 µF capacitor connected in parallel to the zener diode, helps in transient absorption travelling through the D1 diode.
  – Figure 8-3 shows how the external clamping diodes can be used in cases where the 100 mA current rating of D1 and D2 is insufficient. When using external clamping, disable the internal protection of the BUF802 by connecting CLH and CLL to V_{S+} and V_{S-}.

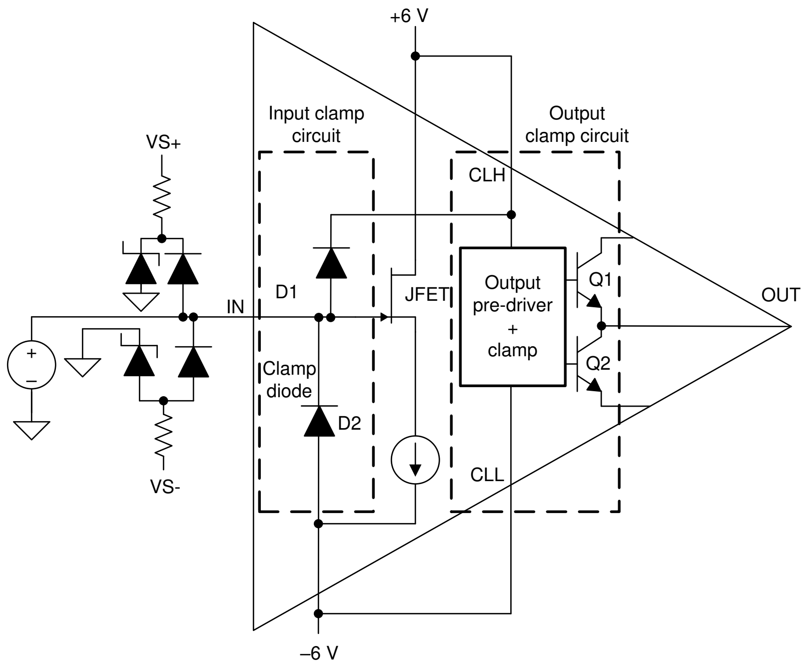


Figure 8-3. External Input Clamp Circuit

- **Output Clamp Circuit**:
  – The output protection circuit prevents the stages following the BUF802 from being overdriven and also ensures that the BUF802 recovers rapidly from a saturated state resulting from an input or output overdrive condition. In a typical data-acquisition system, the BUF802 would be followed by a variable gain amplifier (VGA). High-speed VGAs are typically designed on 5 V processes making it susceptible to potential damage from the 12 V BUF802. The voltage applied to the CLH and CLL pins dictate the maximum output swing of the BUF802.
  – As shown in Figure 8-3, the internal clamps can be disabled by connecting CLH and CLL to V_{S+} and V_{S-} respectively. When the clamps are disabled, the maximum output swing is limited by the output swing specification described in Section 6.5. The response time and accuracy of the output clamp is shown in Section 6.7.
  – The output THD of the BUF802 degrades when V_{CLH} and V_{CLL} are set close to the expected V_{OUT} peak value. To prevent signal degradation, maintain at least a 1.5 V difference between the expected peak output voltage and the clamp voltage applied at the CLH and CLL pins. Figure 8-4 shows the relation between the absolute clamp voltage value and THD for a 1 V_{PP} output.

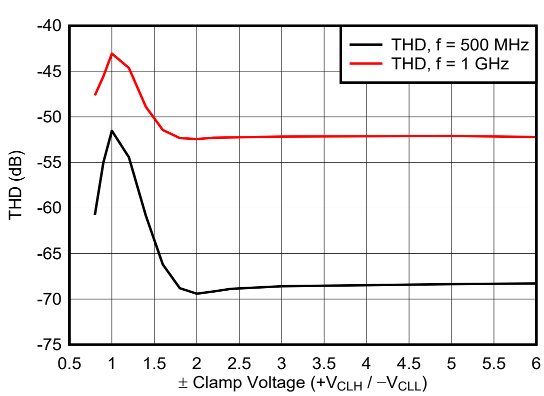


Figure 8-4. THD vs V_{CLH} / V_{CLL} for V_{OUT} = 1 V_{PP}

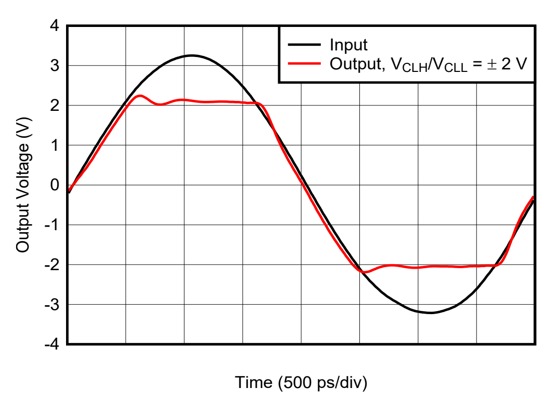


Figure 8-5. Transient Clamp Response

8.3.2 Adjustable Quiescent Current

The BUF802 includes an adjustable quiescent current feature to allow the system designer to trade-off the current consumed versus the distortion performance obtained. As shown in Figure 8-1, connect a resistor between R_Bias and V_{S-} to set the bias point operating current of the output stages. Figure 8-6 shows the quiescent current variation as a function of R_Bias value.

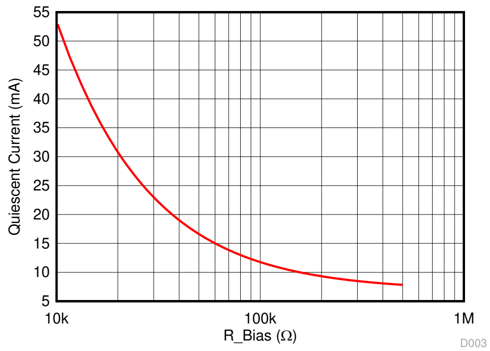


Figure 8-6. Quiescent Current vs R_Bias

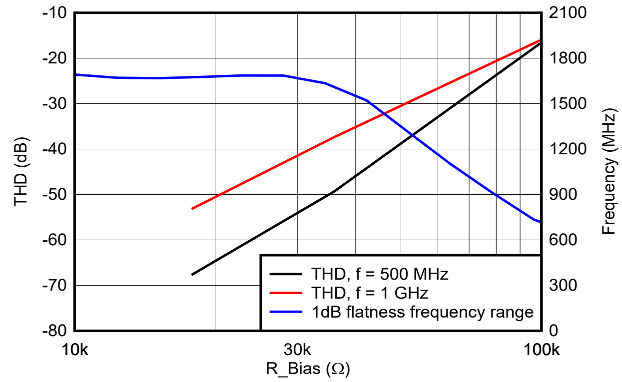


Figure 8-7. THD and Bandwidth vs R_Bias

Figure 8-7 shows that changing the resistor between R_Bias and V_{S-} primarily affects the THD of the output signal. Section 6.5 and Section 6.6 specify the AC and DC parameters of the BUF802 at two different R_Bias values. The DC parameters are independent of the quiescent current setting.

8.3.3 ESD Structure

Figure 8-8 shows the internal ESD structure of the BUF802. V_{SO} and V_S supply pins are internally shorted to each other through back-to-back diodes. Refer to Section 10 for further information. The input ESD diodes D1 and D2 are optimized to carry 100 mA of continuous current while the remaining ESD diodes are rated for 10 mA.

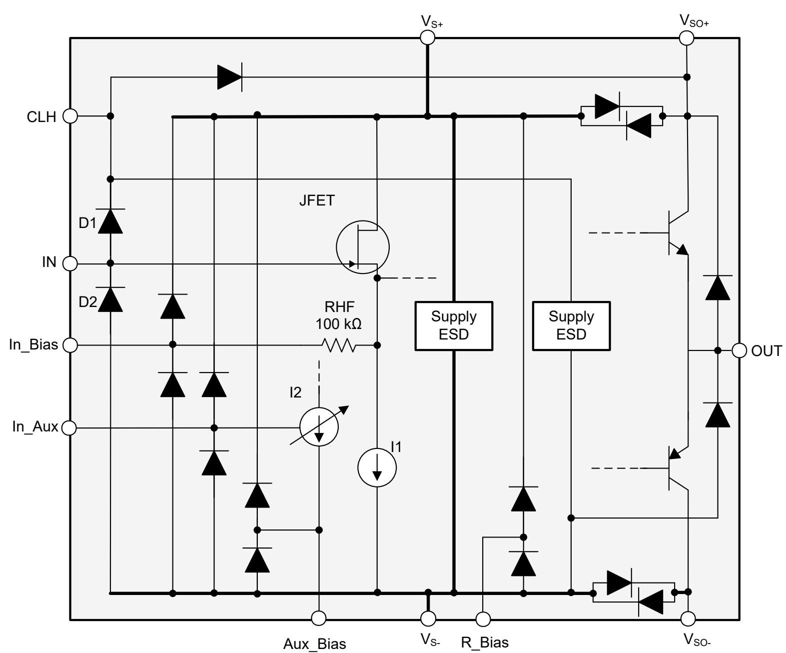


Figure 8-8. Internal ESD Structure

8.4 Device Functional Modes

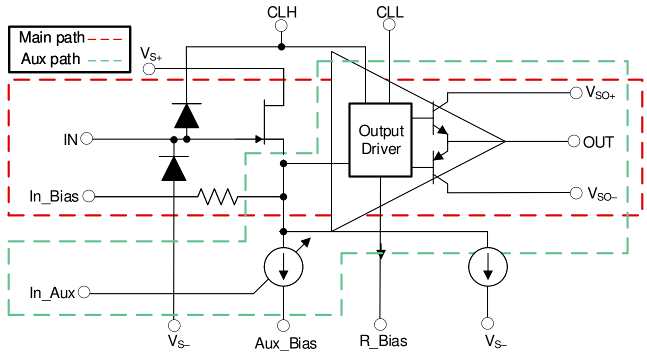


Figure 8-9. Main Path and Auxiliary Path

The BUF802 has been designed to operate in two modes, *Buffer Mode (BF Mode)* and *Composite Loop Mode (CL Mode)*:

In *BF Mode*, the BUF802 uses the JFET, output driver and bipolar transistors in the Main Path to reproduce the signal, applied on IN, at the output of the BUF802. Figure 8-9 shows the Main Path and the Auxiliary Path of the BUF802. The BUF802 can operate from DC to high-frequency and can therefore be used as a standalone buffer. While being used in *BF Mode*, only the Main Path of the BUF802 is used.

In *CL Mode*, the BUF802 utilizes the Auxiliary signal path and the Main Path to control the output voltage. As the name suggests in the *Composite Loop Mode*, the BUF802 is used in a composite loop with a precision amplifier to achieve DC precision and a wide, large-signal bandwidth simultaneously. The composite loop splits the applied signal to low-frequency and high-frequency components and passes them over to different circuits with suitable transfer function. The low-frequency and high-frequency signal components then recombine inside the BUF802 and are repoduced at the OUT pin.

8.4.1 Buffer Mode (BF Mode)

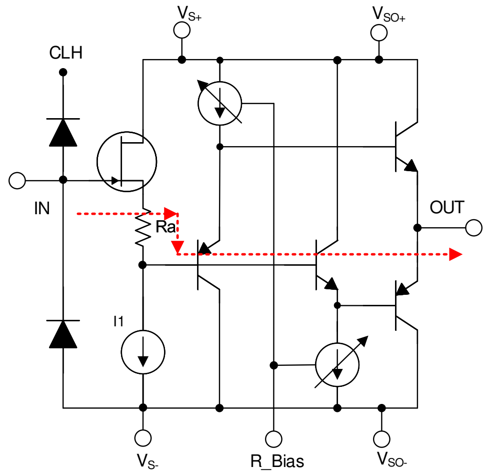


Figure 8-10. Internal Schematic – *BF Mode*

The wide large-signal bandwidth and fast slew rate of the BUF802 coupled with Hi-Z input are useful in a variety of high-frequency signal chain applications. As shown in Figure 8-10 the BUF802 uses the Main Path and operates the JFET and transistors as source follower and emitter followers to reproduce signal applied on IN, at the output of BUF802. The pins associated with only *CL Mode* (Pin No. 6, 4, and 3) are left floating while operating in *BF Mode*.

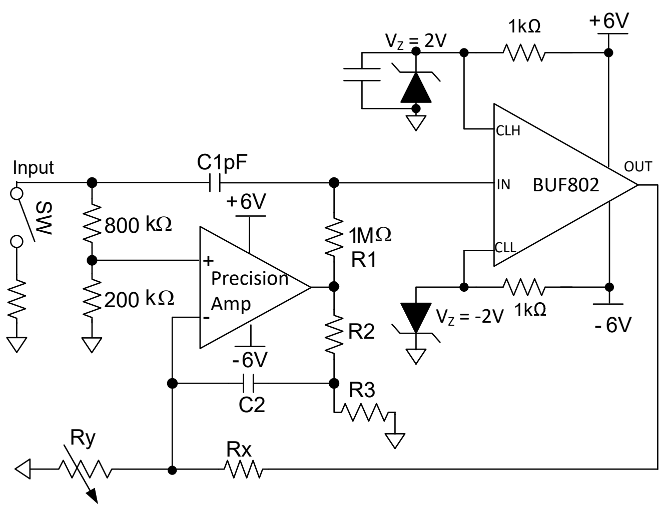


Figure 8-11. Composite Loop Using *BF Mode*

Figure 8-11 shows how the BUF802 can also be used in a composite loop while being operated in *BF Mode*. The operation of BUF802 in Figure 8-11 would still be called *BF Mode* since the signal is being transferred through the Main Path only. The Auxiliary path and the pins associated with the Auxiliary path and *CL Mode* are kept disabled. The low-frequency and high-frequency signal components are combined externally through the discrete components R1 and C1 prior to being applied at the IN pin.

8.4.2 Composite Loop Mode (CL Mode)

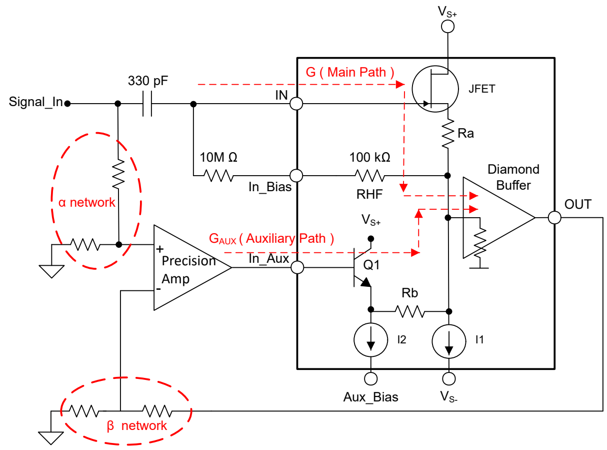


Figure 8-12. Internal Schematic – *CL Mode*

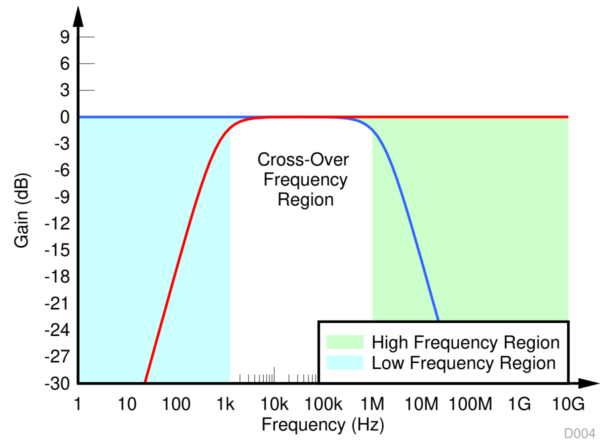


Figure 8-13. *CL Mode* Frequency Response

The 330 pF input series capacitor shown in Figure 8-12 splits the input signal into a low-frequency and high-frequency component. These signals are applied to In_Aux and IN respectively. The IN pin controls the output of BUF802 through the Main Path, whereas the In_Aux pin controls the output through the Auxiliary Path.

The transfer function of the composite loop in *CL Mode* can be split into the following 3 frequency regions:

1. **Low Frequency Region**: The gain of the composite loop in the low-frequency region is α/β (determined by α and β network). In the low-frequency region the 330 pF input capacitor presents a high-impedance in the Main Path, causing the signal to flow through the precision amplifier and the In_Aux pin. This region spans from DC to f_{LF}. f_{LF} is the pole resulting from the gain bandwidth of the precision amplifier, the Auxiliary Path bandwidth, and parasitic capacitance of the components along the path.
2. **High Frequency Region**: In the high-frequency region, the precision amplifier and the Auxiliary Path run out of bandwidth. The net gain of the composite loop in this region is determined solely by the Main Path gain of the BUF802, which is denoted by G. This region spans from the pole created at f_{HF} till the LSBW of the BUF802. The f_{HF} is the pole resulting from the 330 pF series capacitor and the 10 MΩ resistor on the In_Bias pin.
3. **Cross-over Frequency Region**: the Main Path and Auxiliary Path work in conjunction to determine the gain in the crossover region. To maintain a flat frequency response in this region, the following conditions have to be met:
   a. $\alpha/\beta = G$
   b. High frequency response pole $f_{HF} << $ Low frequency pole f_{LF}

   A detailed analysis of discrete component selection to achieve a flat frequency response is discussed further in Section 9.1.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The BUF802 offers a wide large-signal bandwidth, high-slew rate along with high-input impedance making it ideal for data acquisition systems. In applications where DC precision is not needed or in cases where the input is AC coupled, the BUF802 can be used as a standalone input buffer in *BF Mode*. In case the precision required is higher than that offered by the BUF802, operate the BUF802 in *CL Mode* with a precision amplifier in a composite loop.

9.2 Typical Application

9.2.1 Oscilloscope Front-End Amplifier Design

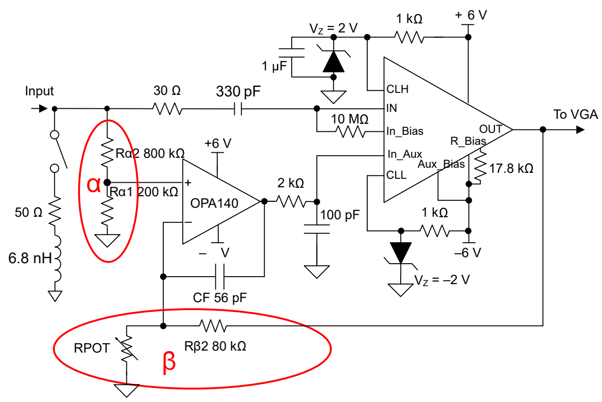


Figure 9-1. Oscilloscope Front-End Amplifier

9.2.1.1 Design Requirements

The following table shows the target specification for a 1-GHz oscilloscope front-end and precision amplifier.

Specification	Value
Input Impedance	1 MΩ / 50 Ω
S Parameters (f = 1 GHz)	S11 = –15 dB, S21 = –1.5 dB
Offset Drift	1 µV/°C maximum
Noise at Highest Resolution (50 Ω Input)	80 μV_{RMS}

9.2.1.2 Detailed Design Procedure

- **Input Impedance**: The JFET-input stage of the BUF802 offers giga ohm's of input impedance and therefore enables the front-end to be terminated with a 1 MΩ resistor without affecting performance. A 50 Ω resistance can also be switched in offering matched termination for high-frequency signals. The BUF802 therefore enables the designer to use both 1 MΩ and 50 Ω termination in the same signal chain.
- **Noise**: The total noise of the front-end amplifier is the function of the voltage and current noise of the BUF802, OPA140, and the resistors thermal noise. The dominant noise source, however, is contributed by the voltage noise of the BUF802 due to its presence across the complete bandwidth. Thus, the total RMS noise of the front-end amplifier shall be approximately equal to the voltage noise of BUF802 over 1 GHz.

The specified input referred voltage noise of the BUF802, as shown in Section 6.5, is 2.3 nV/√Hz. The total input referred RMS noise in a bandwidth of 1 GHz is given by the following equation:

$$En_{RMS} = 2.3\ nV/\sqrt{Hz} \times \sqrt{(1\ GHz \times 1.22)} = 80\ \mu V_{RMS}. \tag{1}$$

1.22 = Brickwall correction factor. Detailed calculations can be found on TI Precision Labs – Op Amps: Noise – Spectral Density.

Total input refered spot noise as a function of frequency is shown in Figure 9-3. Assuming the oscilloscope has 8 divisions on the screen and a highest resolution of 1 mV, the full-scale reading is 8 mV_{PP} or 2.82 mV_{RMS}. Thus, the SNR of the front-end amplifier stage at the highest-resolution setting is:

$$20 \times \log (2.82\ mV_{RMS} / 80\ \mu V_{RMS}) = 31\ dB. \tag{2}$$

- **S11 Optimzation**: The front-end amplifier circuit should have a perfect 50 Ω termination to achieve the required S11 parameter of -15 dB across the frequency. While it is possible to mount an exact 50 Ω resistance at the input of the front-end composite loop circuit, the parasitic capacitance of the BUF802 appears in parallel to this 50 Ω resistance resulting in a net imperfect termination.

  The parasitic input capacitance of BUF802 (IN pin) is 2.4 pF. At 1 GHz this parasitic capacitance reduces down to an impedance of 66.3 Ω. Thus, the net input impedance as seen by the signal at the input is the following:

$$66.3\ \Omega \parallel 50\ \Omega = 28.5\ \Omega \tag{3}$$

  This results in an imperfect termination for the 50 Ω source resulting in poor S11. The addition of a 30 Ω resistance in series with the input trace and a 6.8 nH inductor in series with the onboard 50 Ω termination helps isolate the input parasitic capacitance as well as ensures the net input impedance is maintained at 50 Ω. The S11 response of this modified circuit is shown in Figure 9-4.

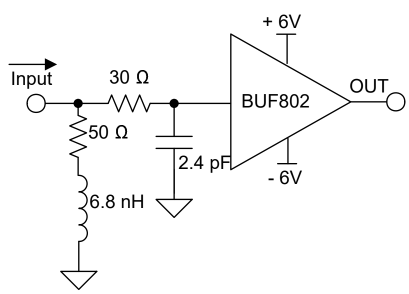


Figure 9-2. Net Input Impedance

- **Uniform Gain Across Frequency**: The front-end amplifier circuit is designed with BUF802 and OPA140 connected in a composite loop. The loop splits the input signal into low- and high-frequency components, taking both components to the output through two different circuits (transfer functions) and recombining them to reproduce a net output signal. The end goal is to achieve a smooth transition between the two circuits and ensure a flat frequency response from DC till the frequency of interest.

  CL Mode of BUF802 simplifies this design for achieving a flat frequency response from DC till the frequency of interest (1 GHz in this case). To achieve a flat response, the following two conditions have to be met:

  1. $\alpha/\beta = G$
  2. High frequency response pole f_{HF}<< low frequency pole f_{LF}

  α is the input attenuation factor and β is the inverse of the non-inverting gain of the precision amplifier. G is the DC gain of the Main Path of the BUF802. Since G can vary from device-to-device, trimming either α or β is recommended to achieve a flat frequency response. In Figure 9-1, β may be trimmed using the RPOT. Since G is ≈1 V/V and α is 1/5 (200 kΩ / (200 kΩ + 800 kΩ)), RPOT should be trimmed so that β ≈ 1/5.

  For the β network, it is recommended to use resistors which are an order of magnitude of resistance lower than the resistors used in the α network. Therefore β resistor values of 80 kΩ and ≈20 kΩ have been chosen.

f_{HF} is the pole resulting from the 330 pF series capacitor and the 10 MΩ resistor on the In_Bias pin.

$$f_{HF} = 1/(2 \times pi \times R \times C) = 1/(2 \times 3.14 \times 10\ M\Omega \times 330\ pF) = 48\ Hz \quad (4)$$

f_{LF} is the pole resulting from the gain bandwidth of the precision amplifier (OPA140), the Auxiliary Path bandwidth and other parasitic capacitance of the resistor network.

$$f_{LF} = GBW \times G_{AUX} \times \beta = 440\ kHz \quad (5)$$

Where GBW is the gain bandwidth product of the precision amplifier (OPA140) = 11 MHz. G_{AUX} is the gain from In_Aux to OUT = 0.2 V/V. 1/β is the external non-inverting gain set for the precision amplifier = 5 V/V.

Based on the above value of f_{HF} and f_{LF}, the required condition of $f_{HF} << f_{LF}$ is met. CF, connected across the precision amplifier, is required to compensate for the parasitic capacitance and to make the overall poles and zeros cancel each other. The value of CF can be found by using the following equation:

$$CF = C_{INPA} \times ((G \times R_{\alpha 2} / R_{\beta 2}) - 1)). \quad (6)$$

Where C_{INPA} is the common mode input capacitance of the precision amplifier, OPA140 in this case.

Plugging in the value of these components arrives at CF = 56 pF. In the final system, based on the quality of the flat band response needed, CF may or may not be trimmed along with RPOT in the final production flow.

9.2.1.3 Application Curves

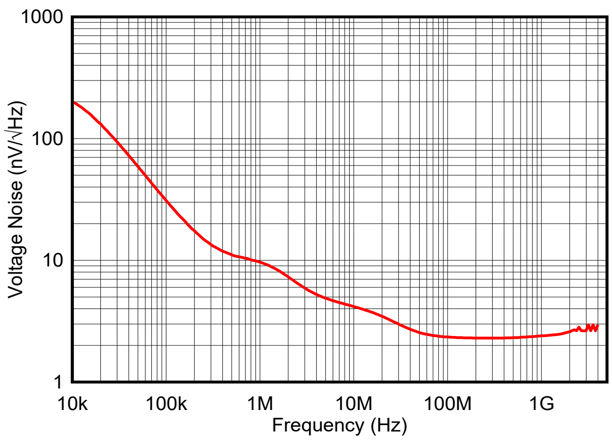


Figure 9-3. Front-End Composite Loop Noise

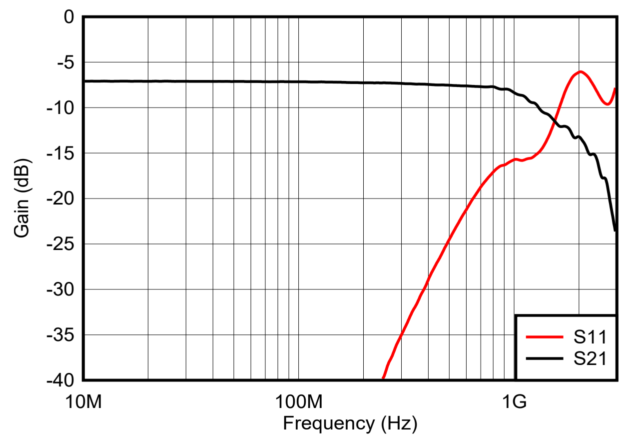


Figure 9-4. S11 and S21 Response

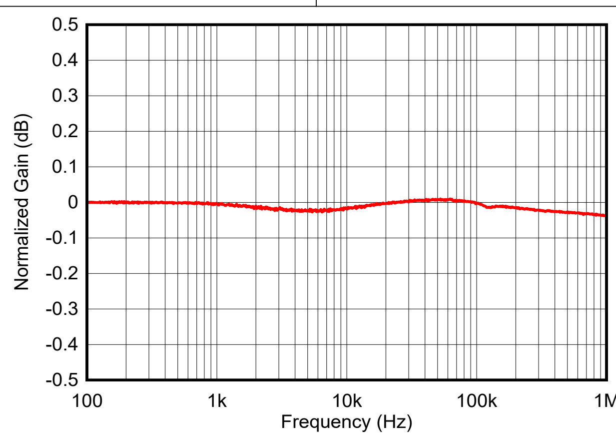


Figure 9-5. Frequency Response Flatness: Cross-Over Frequency Region

9.2.2 Transforming a Wide-Bandwidth, 50 Ω Input Signal Chain to High-Input Impedance

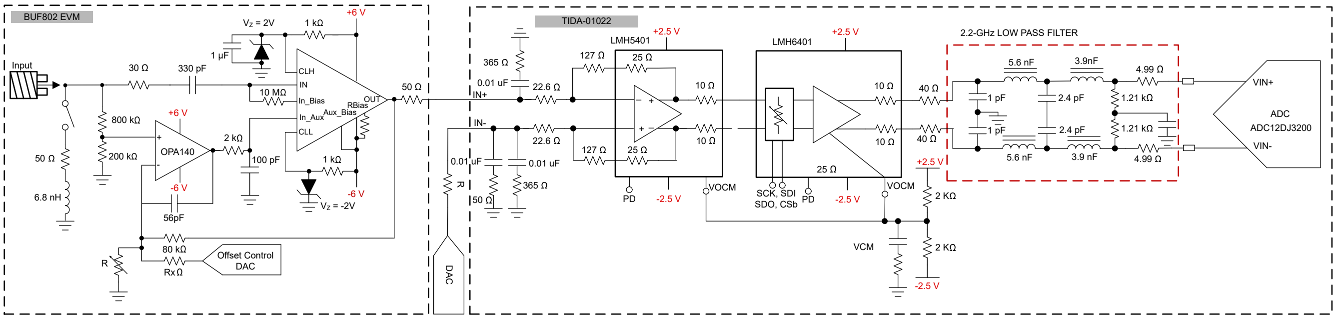


Figure 9-6. BUF802 + TIDA-01022: Signal Chain

9.2.2.1 Detailed Design Results

TIDA-01022 reference design primarily focuses on a multichannel high-speed analog front-end, which is typically used in end equipment like a digital storage oscilloscope (DSO), wireless communication test equipment (WCTE), and radars. A 50 Ω input data acquisition (DAQ) signal chain like that of TIDA-01022 can be converted into a high-input impedance DAQ system by inserting the BUF802 at the front.

TIDA-01022 orginally features the following:

- LMH5401 is a high-performance, differential amplifier with an usable bandwidth from DC to 2 GHz. It is used as single to differential conversion amplifier in this signal chain. The device offers excellent linearity performance at a fixed 12-dB gain.
- LMH6401 is a wideband digitally controlled variable gain, differential in and differential out, amplifier. The noise and distortion performance are optimized to drive ultra-wideband ADCs. The device offers DC to 4.5-GHz bandwidth with a gain range from –6 dB to 26 dB in 1-dB steps. The gain can be controlled using a standard serial peripheral interface (SPI).
- The ADC12DJ5200RF device is a 12 bit, giga-sample, analog-to-digital converter (ADC) that can directly sample input frequencies from DC to above 10 GHz. ADC12DJ5200RF can be configured as a dual-channel, 5.2 GSPS ADC or single-channel, 10.4 GSPS ADC.

The BUF802 along with offering high-input impedance and low-noise for the front-end amplifier, holds capability of driving matched loads of 50 Ω, making it easy to retrofit with predesigned analog front-end signal chains. Figure 9-7 to Figure 9-9 shows the comparison of native performance of the TI design TIDA-01022 and performance achieved post addition of BUF802 at the front-end. Adding BUF802 at the input of TIDA-01022 translates the original 50 Ω input imepdance TI design to a high-input impedance DAQ signal chain. A simplified schematic of BUF802 + TIDA-01022 is shown in Figure 9-6.

9.2.2.2 Application Curves

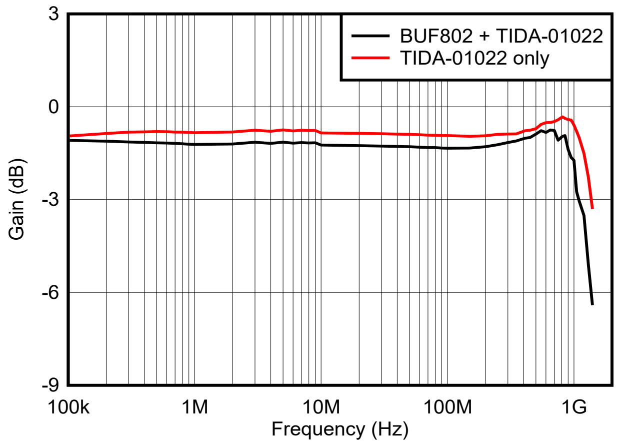


Figure 9-7. Gain vs Frequency

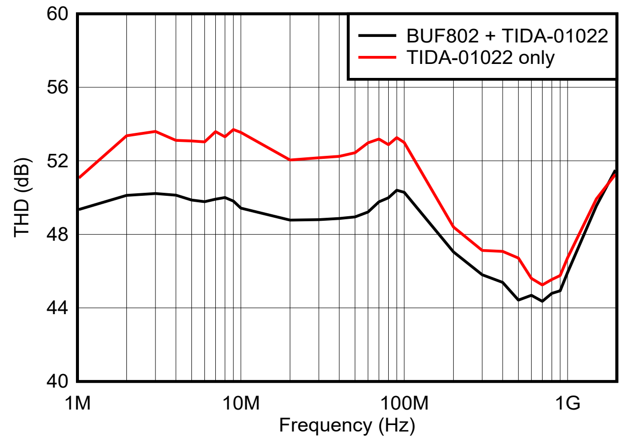


Figure 9-8. Total Harmonic Distortion (THD) vs Frequency

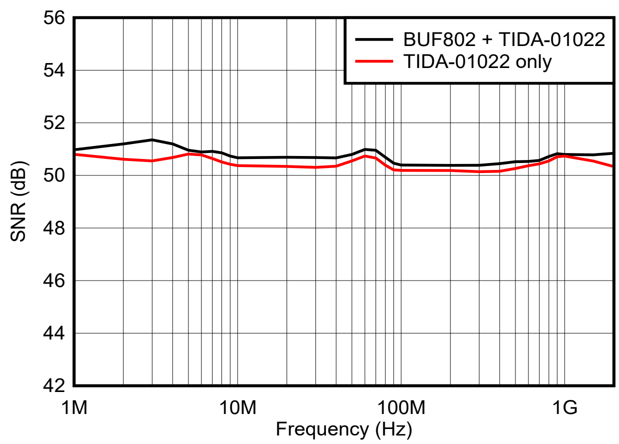


Figure 9-9. Signal To Noise Ratio (SNR) vs Frequency

10 Power Supply Recommendations

The BUF802 is intended to operate with supplies ranging from ±4.5 V to ±6.5 V. The BUF802 can operate on either single-sided supplies or split supplies. When using split supplies, the supplies may be symmetrically balanced around GND or asymmetric. For best AC performance, the input and output signal should be centered around the mid-supply.

Minimize the distance between the power-supply pins and decoupling capacitors. The high frequency capacitors (< 0.1 µF) should be placed close to the supply-pins on the same side of the PCB as the BUF802. Larger capacitors (> 1 µF) can be placed further away from the device. Section 11 has additional details on decoupling capacitor layout and routing.

The BUF802 has two sets of supply pins: V_{S+} and V_{S-}; V_{SO+} and V_{SO-}. The separation of the input and output stage supply pins minimize spurious cross-talk and maximizes transient decoupling between the two stages. Figure 8-1 shows how both sets of supply pins are internally connected through back-to-back diodes. It is therefore imperative that the supply pins for the input and output stages are connected to the same potential. As shown in Section 11, maintain separate and individual decoupling capacitors for all the supply pins.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with the BUF802 requires careful attention to board layout, parasitics, and passive component selection. Consider the following:

- **Peaking in the S21 transfer function**: keeping the trace length minimum is of prime importance to ensure no peaking occurs in the S21 transfer function of the BUF802. The trace inductance can form a resonant circuit with the input capacitance of the BUF802, causing peaking in the S21 response. Add a small resistor (R5 in Figure 11-1) in series with the DC blocking capacitor to dampen the LC resonance created by the trace inductance and the input capacitance of the BUF802. Choose series capacitors (C7 in Figure 11-1) with low equivalent series inductance (ESL) to minimize total inductance.
- **Power-supply bypass capacitors**: mount the power-supply bypass capacitors as close to the supply pins as possible and on the same side of the PCB as the BUF802. As shown in Figure 11-1, choose low-inductance LICC capacitors (C5, C6, C13, and C10) to minimize high frequency impedance between the BUF802 and the bypass capacitors. Use multiple vias between the bypass capacitor and GND to reduce series inductance. As shown in Figure 11-1, also use multiple vias to GND on the 50 Ω input termination resistor (R3). Connect the bypass and termination vias to a solid GND plane.
- **High precision signal path**, consisting of the precision op amp along with discrete components, can be adjusted and moved around to give precedence to the above two points. In the Figure 11-3, the precision components were placed on the opposite side of the PCB as the BUF802.
- **Thermal pad** of the BUF802 is thermally conductive but electrically insulated to the die. This gives the circuit designer flexibility in connecting the thermal pad to any voltage. Choose a power or GND plane with the highest thermal mass for effective heat dissipation.

11.2 Layout Example

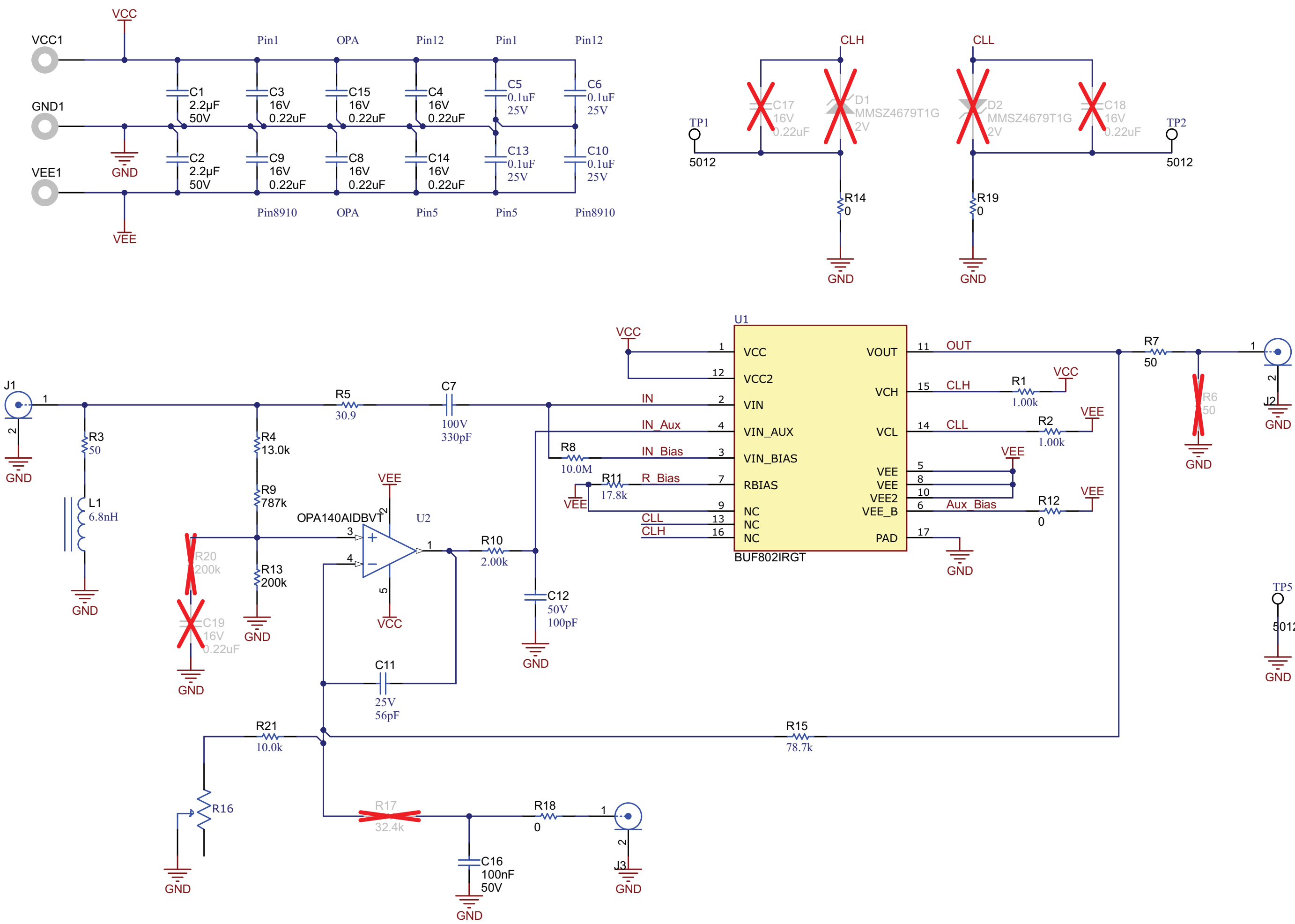


Figure 11-1. Layout Example: Schematic for Layout Reference

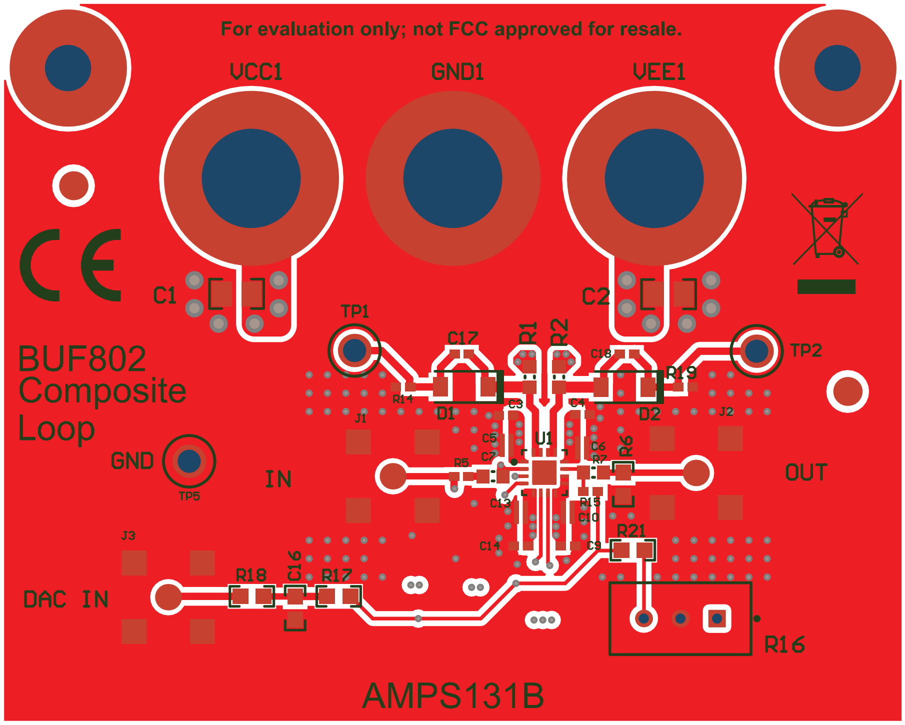


Figure 11-2. Layout Example: Top Layer

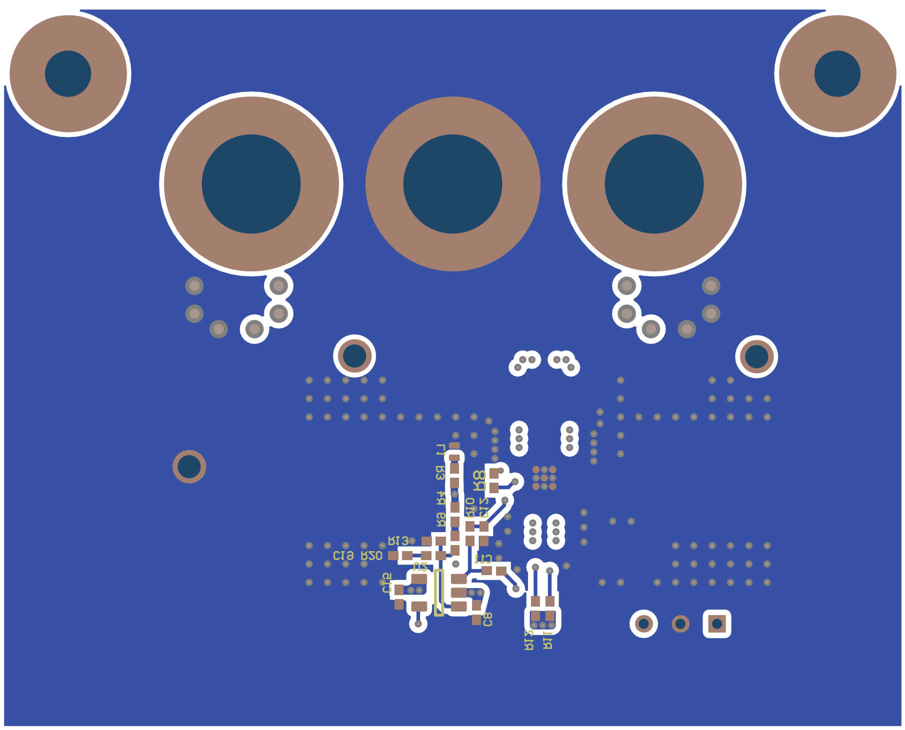


Figure 11-3. Layout Example: Bottom Layer

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Flexible 3.2-GSPS multi-channel AFE reference design for DSOs, radar and 5G wireless test systems* reference designs

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF802IRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUF802	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

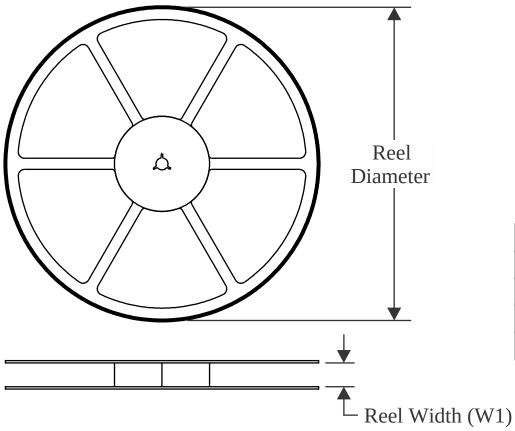
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

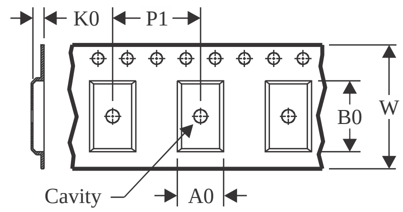
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

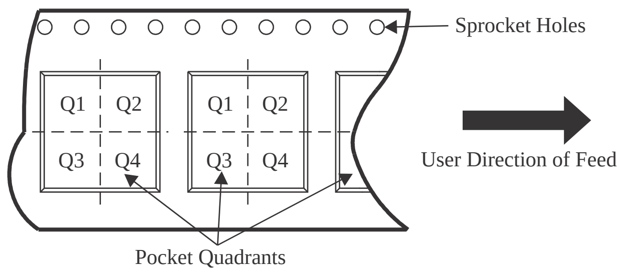


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

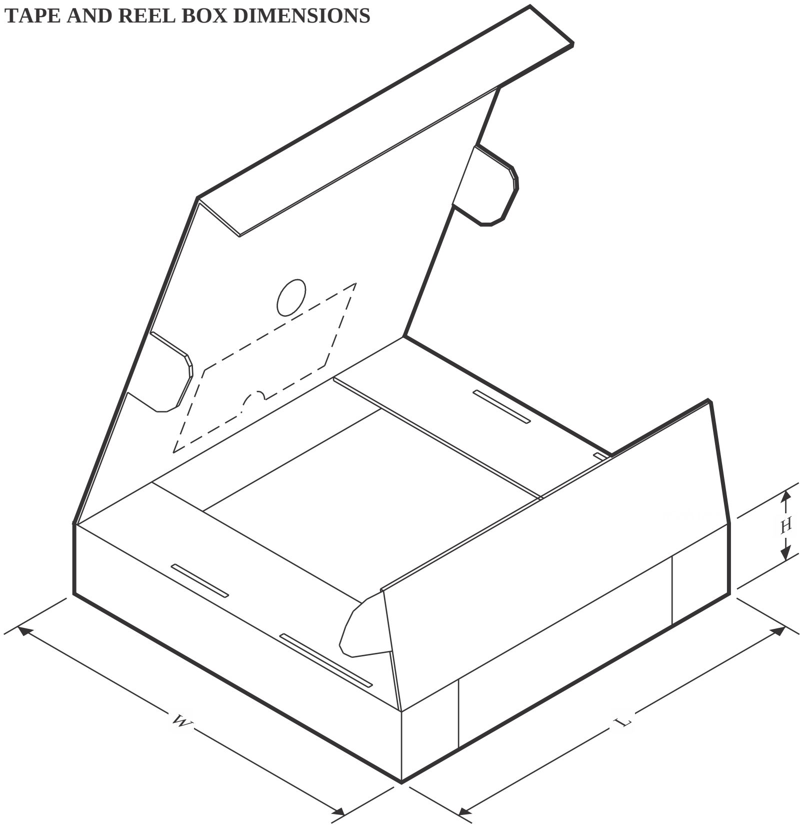
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

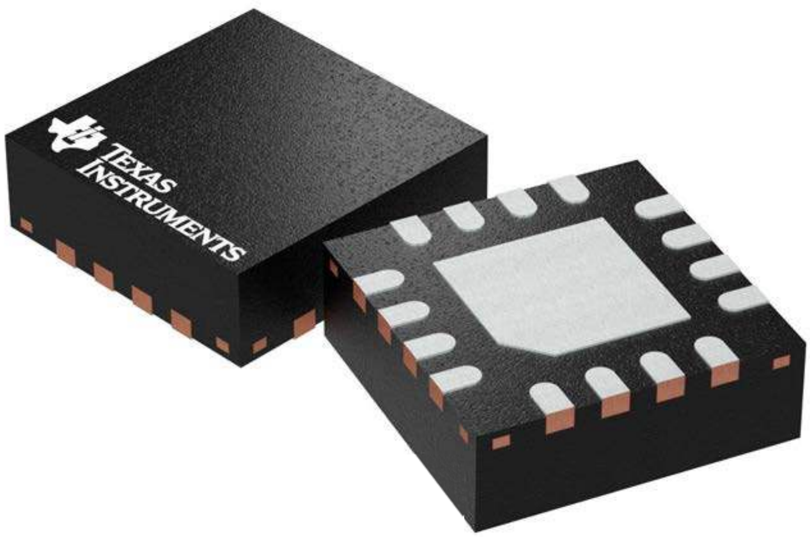
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF802IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

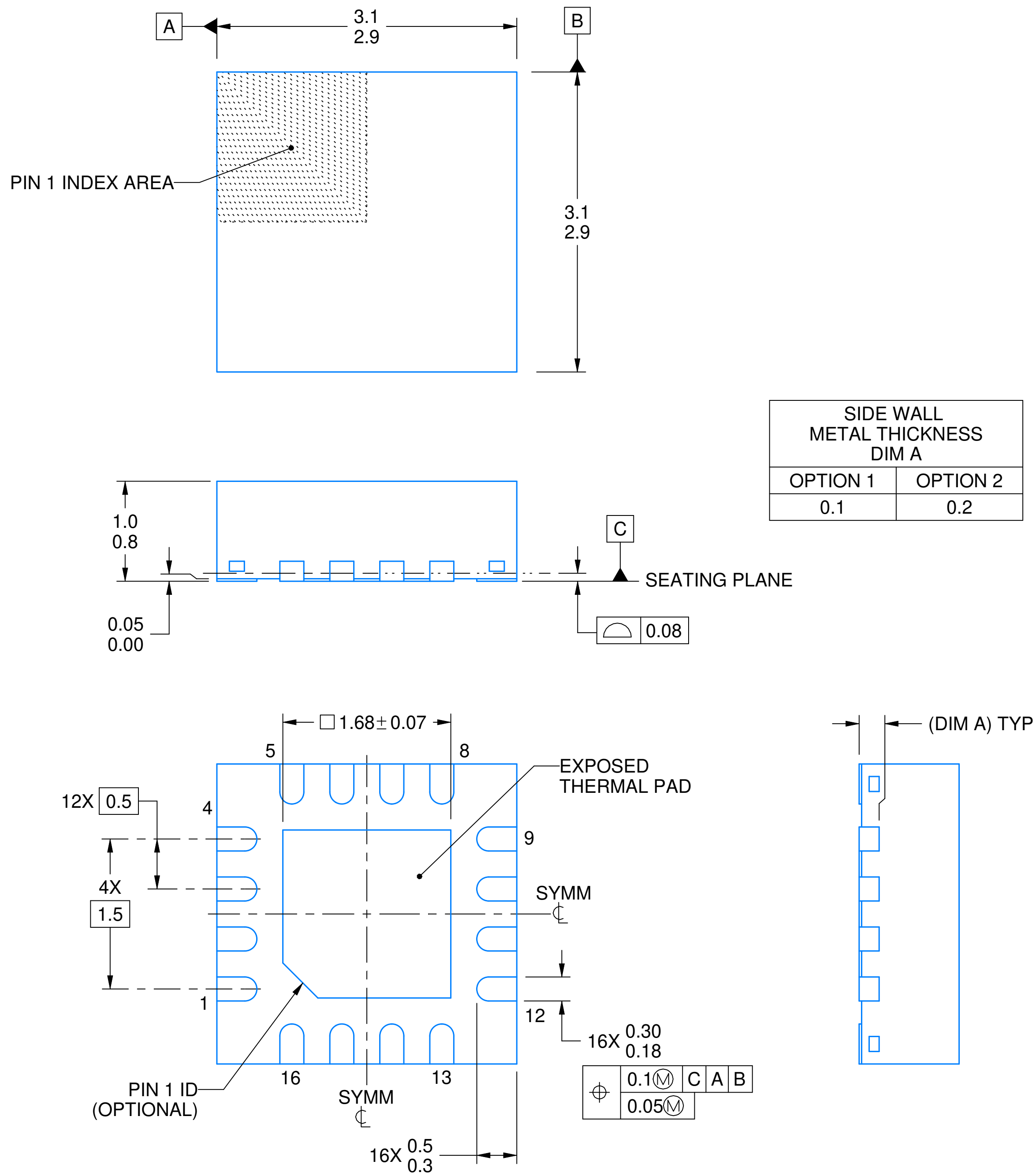


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF802IRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

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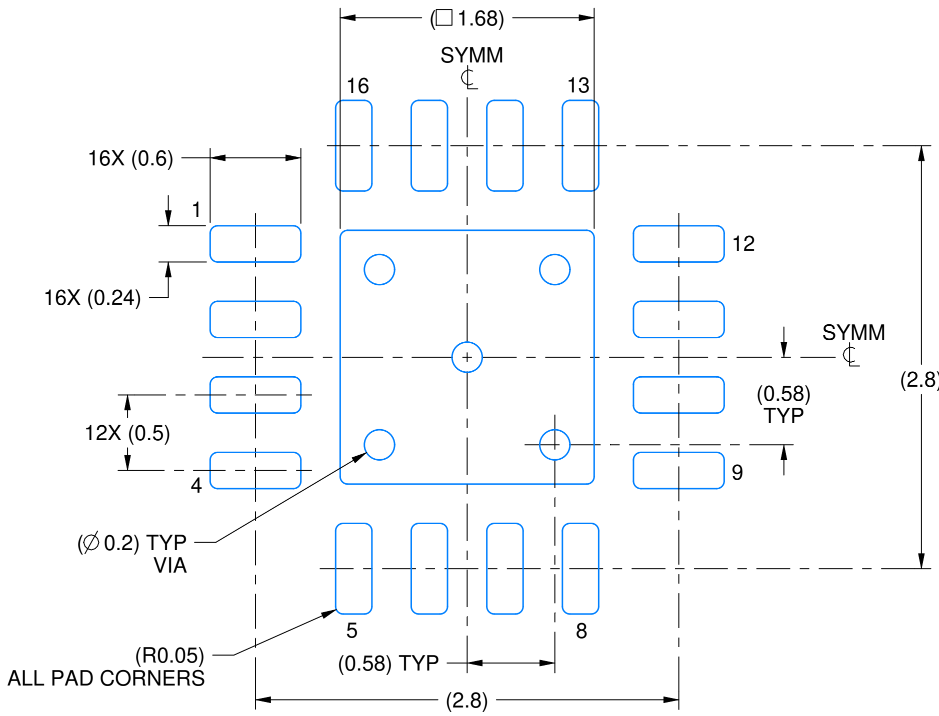
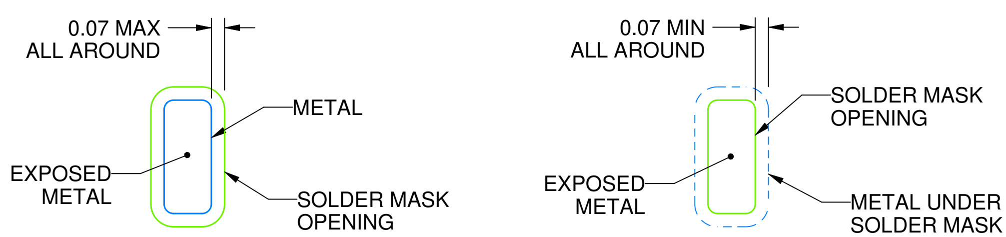
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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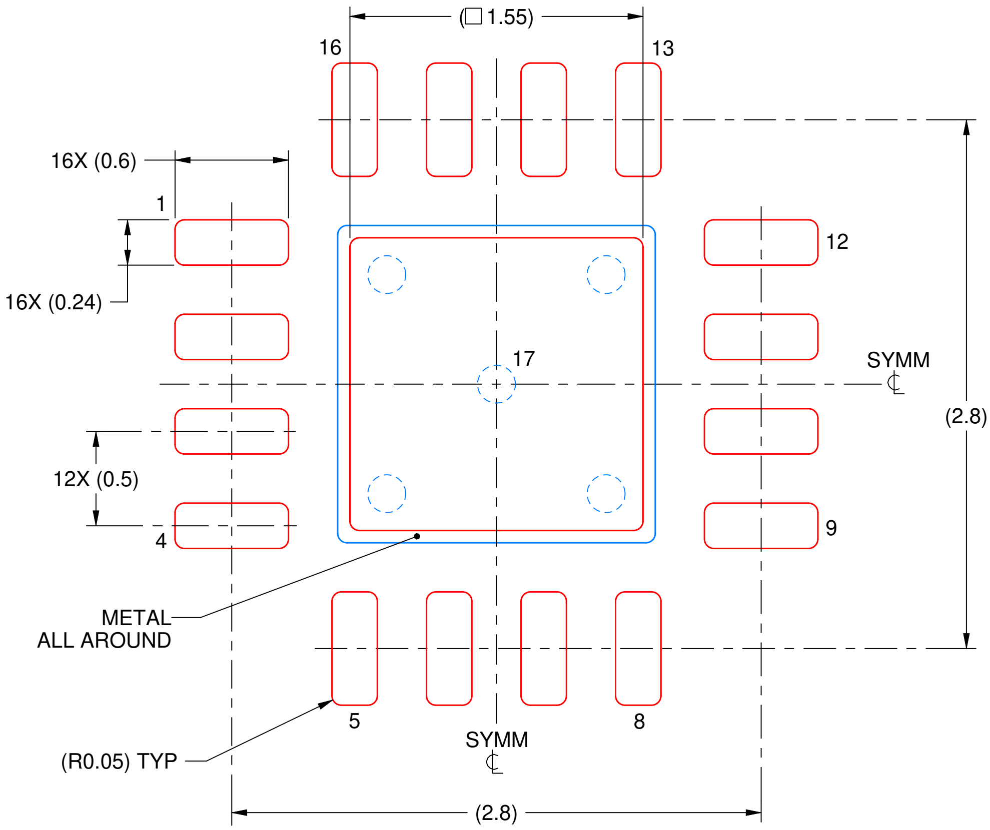
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.