

IRFP150/151/152/153 IRFP150R/151R/152R/153R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

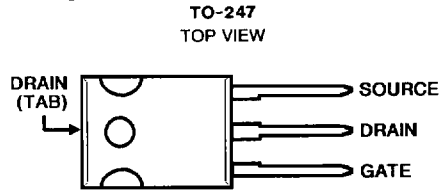
- 34A and 40A, 60V - 100V
- $r_{DS(on)} = 0.055\Omega$ and 0.08Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFP150, IRFP151, IRFP152, and IRFP153 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP150R, IRFP151R, IRFP152R, and IRFP153R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

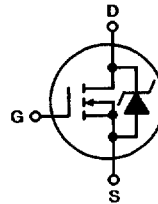
The IRFP types are supplied in the JEDEC TO-247 plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRFP150 IRFP150R	IRFP151 IRFP151R	IRFP152 IRFP152R	IRFP153 IRFP153R	UNITS	
Drain-Source Voltage (1)	V_{DS}	100	60	100	60	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR}	100	60	100	60	V
Continuous Drain Current						
$T_C = +25^\circ\text{C}$	I_D	40	40	34	34	A
$T_C = +100^\circ\text{C}$	I_D	26	26	22	22	A
Pulsed Drain Current (3)	I_{DM}	160	160	140	140	A
Gate-Source Voltage	V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation						
$T_C = +25^\circ\text{C}$	P_D	180	180	180	180	W
Linear Derating Factor		1.44	1.44	1.44	1.44	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM}	170	170	140	140	A
(See Figure 14, $L = 100\mu\text{H}$)						
Single Pulse Avalanche Energy Rating (4)	E_{as}^*	150	150	150	150	mJ
Operating and Storage Junction	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range						
Maximum Lead Temperature for Soldering	T_L	300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)						

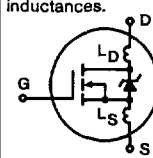
NOTES:

1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. $V_{DD} = 10\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 170\mu\text{H}$, $R_{GS} = 50\Omega$, $I_{PEAK} = 40\text{A}$. See Figure 15.

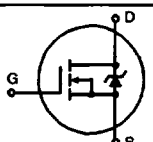
* R Suffix Types Only

IRFP150, IRFP151, IRFP152, IRFP153 IRFP150R, IRFP151R, IRFP152R, IRFP153R

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Drain-Source Breakdown Voltage IRFP150/152, IRFP150R/152R IRFP151/153, IRFP151R/153R	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	100	-	-	V	
			60	-	-	V	
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0	-	4.0	V	
Gate-Source Leakage Forward	I _{GSS}	V _{GS} = 20V	-	-	500	nA	
Gate-Source Leakage Reverse	I _{GSS}	V _{GS} = -20V	-	-	-500	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Max Rating, V _{GS} = 0V	-	-	250	μA	
		V _{DS} = Max Rating x 0.8, V _{GS} = 0V, T _C = +125°C	-	-	1000	μA	
On-State Drain Current (Note 2) IRFP150/151, IRFP150R/151R IRFP152/153, IRFP152R/153R	I _{D(ON)}	V _{DS} > I _{D(ON)} x r _{DS(ON)} Max, V _{GS} = 10V	40	-	-	A	
			34	-	-	A	
Static Drain-Source On-State Resistance (Note 2) IRFP150/151, IRFP150R/151R IRFP152/153, IRFP152R/153R	r _{DS(ON)}	V _{GS} = 10V, I _D = 22A	-	0.045	0.055	Ω	
			-	0.06	0.08	Ω	
			-	-	-	-	
Forward Transconductance (Note 2)	g _{fs}	V _{DS} = 2 x V _{GS} , I _D = 20A	13	20	-	S(Ω)	
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz See Figure 10	-	2000	-	pF	
Output Capacitance	C _{OSS}		-	1000	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	350	-	pF	
Turn-On Delay Time	t _{d(ON)}		V _{DD} = 50V, I _D = 40A, R _G = 6.8Ω	-	15	24	ns
Rise Time	t _r	See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	140	210	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	60	89	ns	
Fall Time	t _f		-	90	140	ns	
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g		V _{GS} = 10V, I _D = 40A, V _{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	110	nC
Gate-Source Charge	Q _{gs}		-	20	-	nC	
Gate-Drain ("Miller") Charge	Q _{gd}		-	30	-	nC	
Internal Drain Inductance	L _D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die.		-	5.0	-	nH
Internal Source Inductance	L _S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.		-	12.5	-	nH
Junction-to-Case	R _{θJC}		-	-	0.70	°C/W	
Case-to-Sink	R _{θCS}	Mounting surface flat, smooth and greased	-	0.1	-	°C/W	
Junction-to-Ambient	R _{θJA}	Free air operation	-	-	30	°C/W	

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.		-	-	40	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}			-	-	170	A
Diode Forward Voltage (Note 2)	V _{SD}	T _J = +25°C, I _S = 40A, V _{GS} = 0V	-	-	2.5	V	
Reverse Recovery Time	t _{rr}	T _J = +25°C, I _F = 40A, dI _F /dt = 100A/μs	98	-	530	ns	
Reverse Recovered Charge	Q _{RR}	T _J = +25°C, I _F = 40A, dI _F /dt = 100A/μs	0.41	-	2.5	μC	
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-	

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width < 300μs,
Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max.
junction temperature. See Transient Thermal
Impedance Curve (Figure 5)

4. V_{DD} = 10V, Start T_J = +25°C, L = 170μH,
R_{GS} = 50Ω, I_{PEAK} = 40A (See Figure 15)

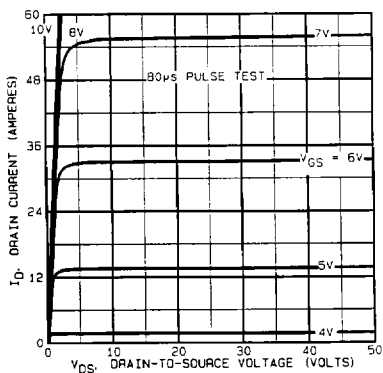


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

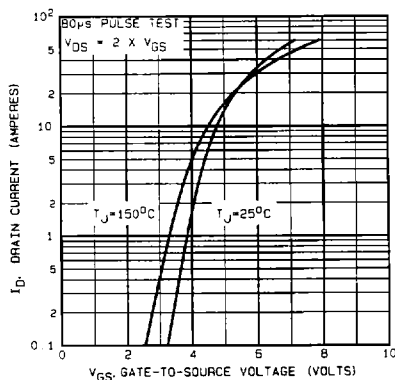


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

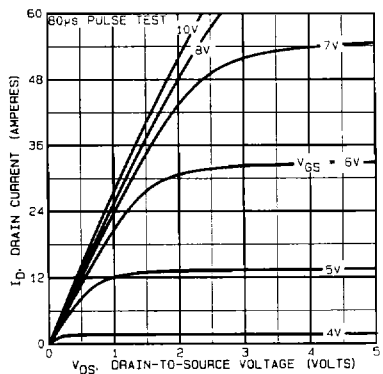


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

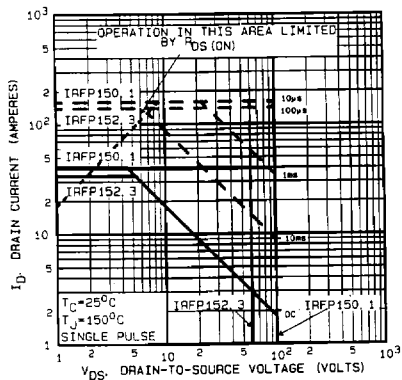


FIGURE 4. MAXIMUM SAFE OPERATING AREA

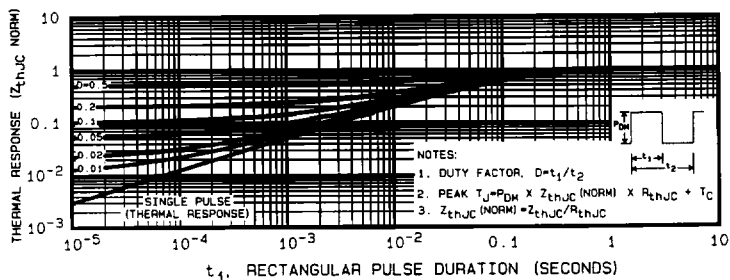


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

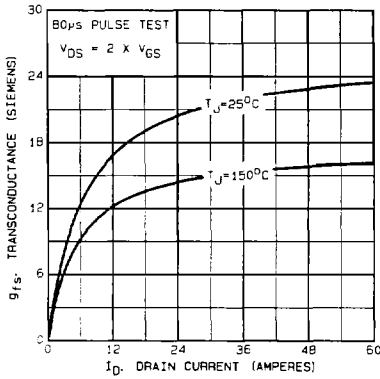


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

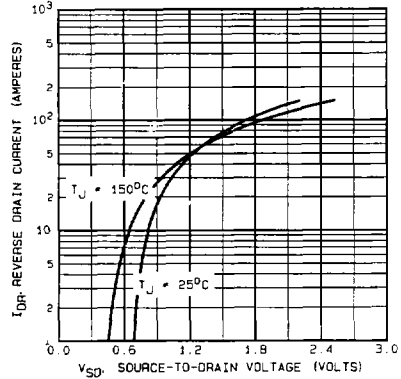


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

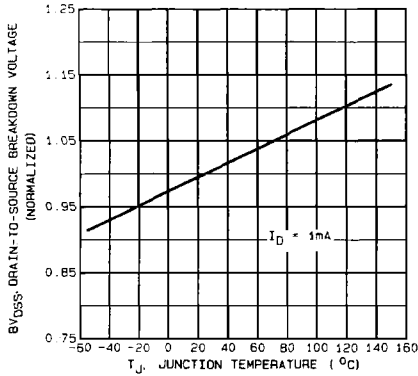


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

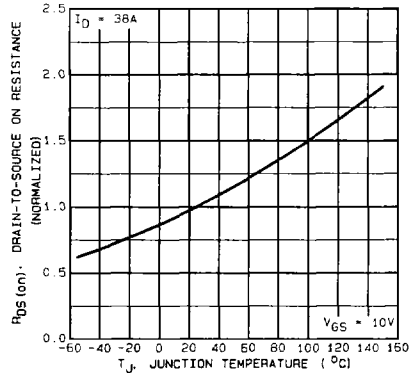


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

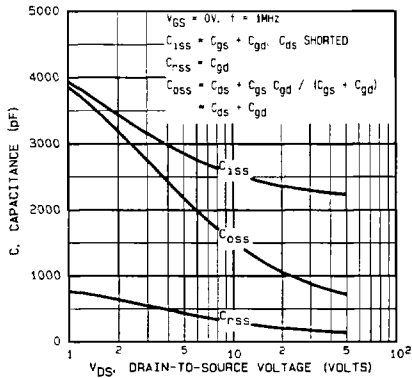


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

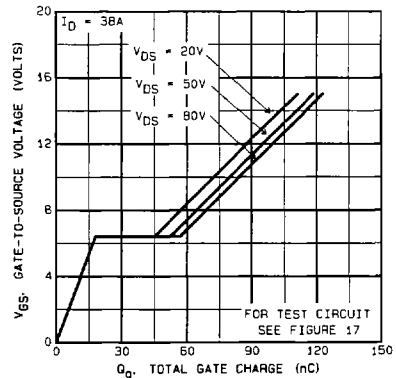


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

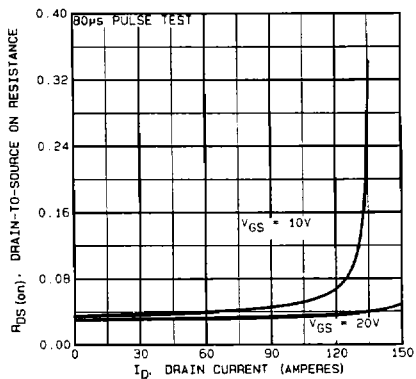


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

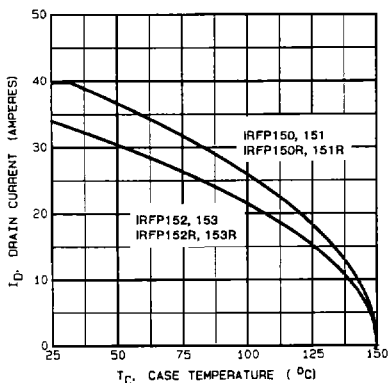


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

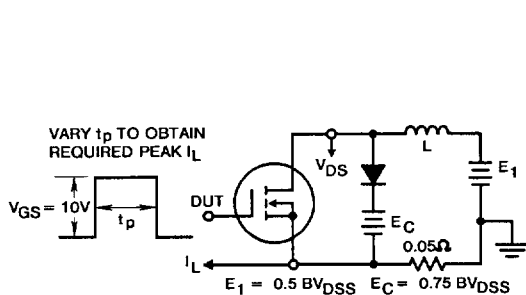


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

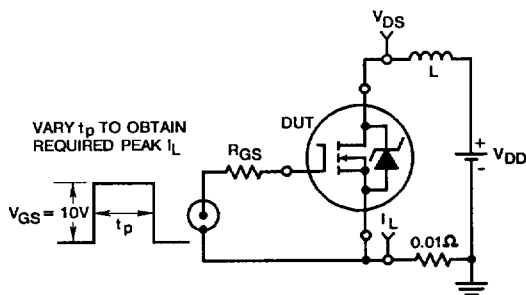


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

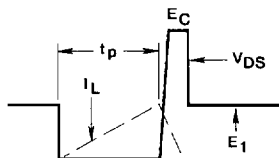


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

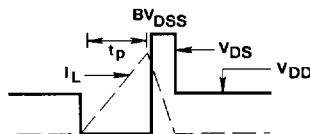


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

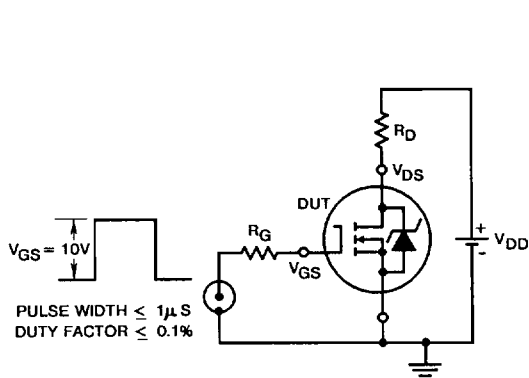


FIGURE 16. SWITCHING TIME TEST CIRCUIT

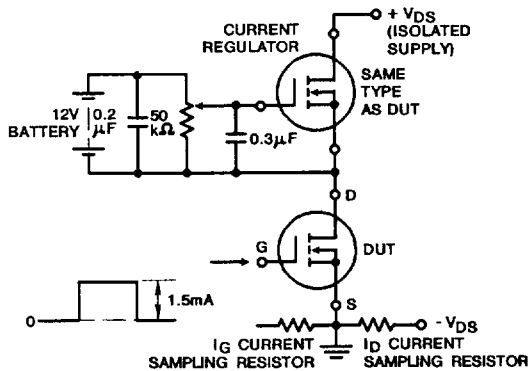


FIGURE 17. GATE CHARGE TEST CIRCUIT