

# DATA SHEET

## **74F51**

Dual 2-wide 2-input, 2-wise 3-input  
AND-OR-invert gate

Product specification

1989 Mar 03

IC15 Data Handbook

# Dual 2-wide 2-input, 2-wide 3-input AND-OR-invert gate

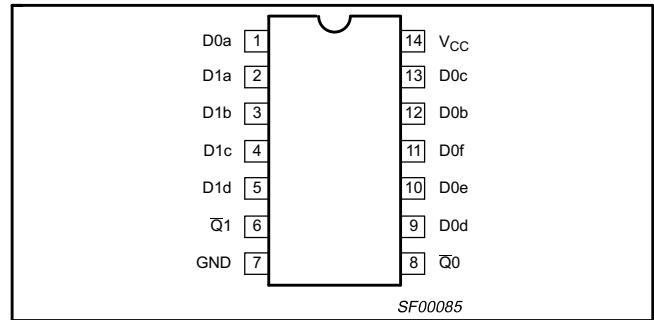
# 74F51

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F51	3.0ns	3.5mA

### ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
14-pin plastic DIP	N74F51N	SOT27-1
14-pin plastic SO	N74F51D	SOT108-1

### PIN CONFIGURATION

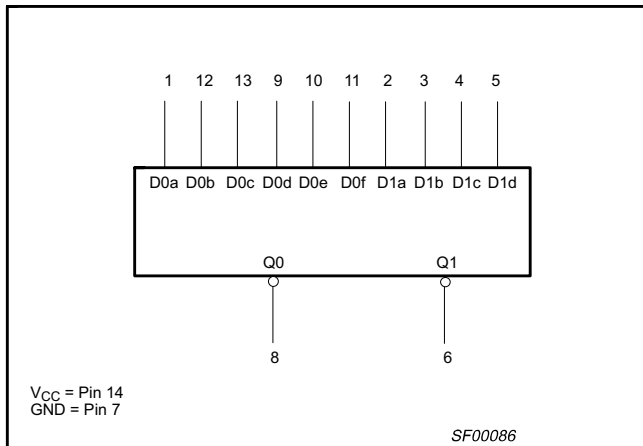


### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

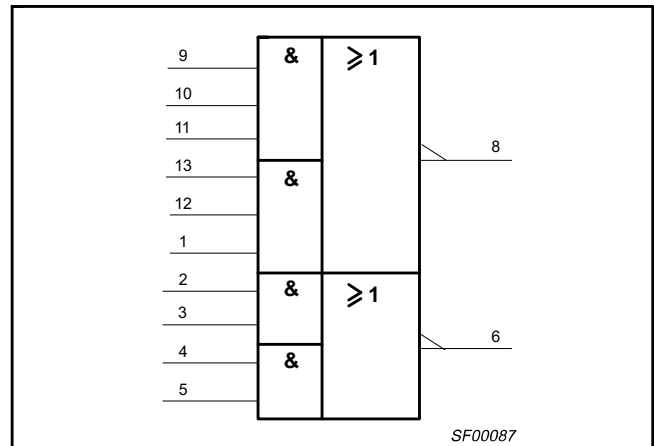
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc, Dnd, Dne, Dnf	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\bar{Q}0, \bar{Q}1$	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

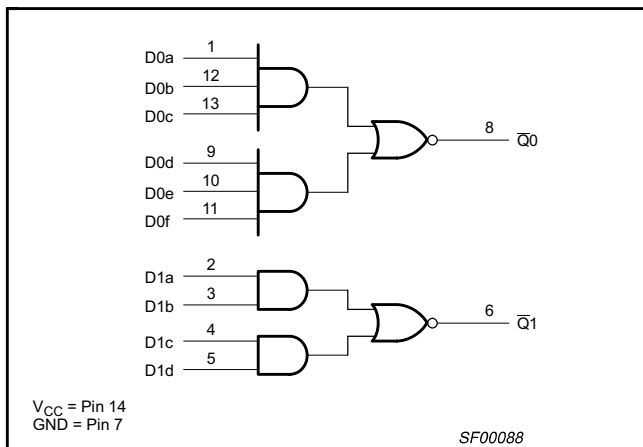
### LOGIC SYMBOL



### IEC/IEEE SYMBOL



### LOGIC DIAGRAM



### FUNCTION TABLE FOR 3-INPUT GATES

INPUTS						OUTPUT
D0a	D0b	D0c	D0d	D0e	D0f	$\bar{Q}0$
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

NOTES:  
 H = High voltage level  
 L = Low voltage level  
 X = Don't care

### FUNCTION TABLE FOR 2-INPUT GATES

INPUTS				OUTPUT
D1a	D1b	D1c	D1d	$\bar{Q}1$
H	H	X	X	L
X	X	H	H	L
All other combinations				H

NOTES:  
 H = High voltage level  
 L = Low voltage level  
 X = Don't care

## Dual 2-wide 2-input, 2-wide 3-input AND-OR-invert gate

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	±10%V <sub>CC</sub>	2.5		V	
		V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V
		V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±5%V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.2	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				-0.6	mA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-60		-150	mA
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX	V <sub>IN</sub> = GND		1.8	3.0	mA
					5.5	7.5	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

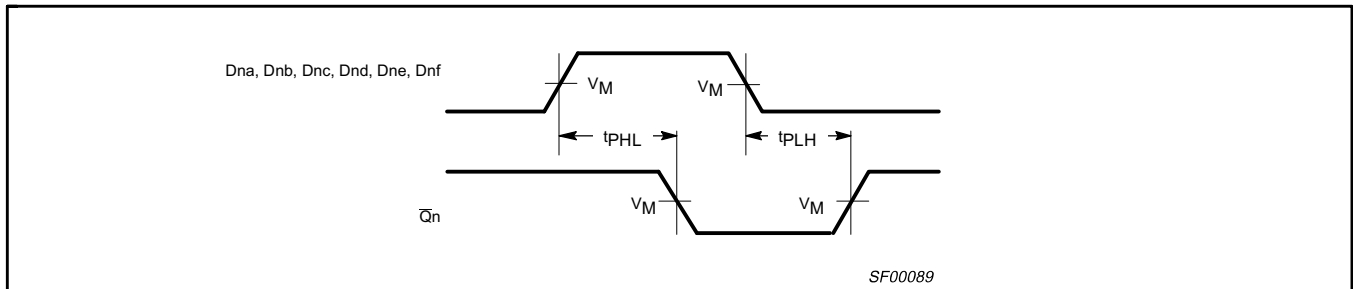
# Dual 2-wide 2-input, 2-wide 3-input AND-OR-invert gate

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5.0V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dna, Dnb, Dnc, Dnd, Dne, Dnf to $\bar{Q}_n$	Waveform 1	2.0 1.0	3.5 2.5	5.5 4.0	1.5 1.0	6.5 4.5	ns

## AC WAVEFORMS



Waveform 1. Propagation Delay for Inverting Outputs

**NOTE:**

For all waveforms, V<sub>M</sub> = 1.5V.

## TEST CIRCUIT AND WAVEFORM

**Test Circuit for Totem-Pole Outputs**

**DEFINITIONS:**

R<sub>L</sub> = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

**Input Pulse Definition**

family	INPUT PULSE REQUIREMENTS					
	amplitude	V <sub>M</sub>	rep. rate	t <sub>w</sub>	t <sub>TLH</sub>	t <sub>THL</sub>
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

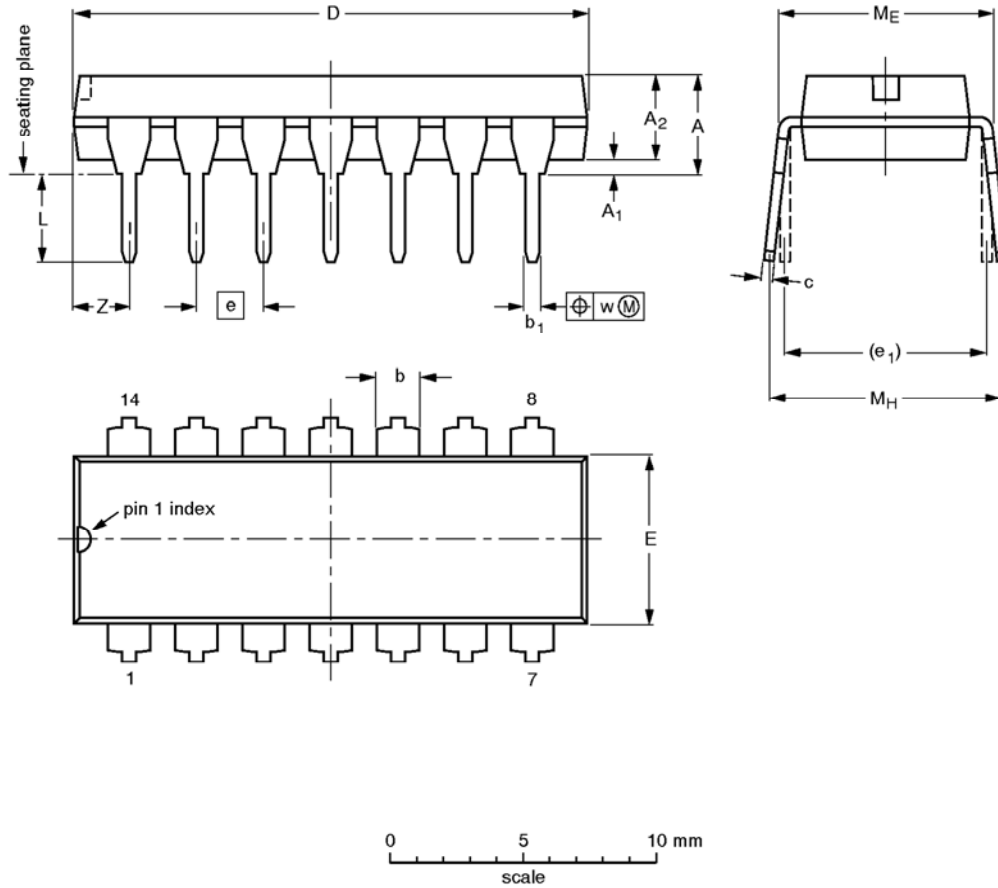
SF00006

# Dual 2-wide 2-input, 2-wise 3-input AND-OR-invert gate

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

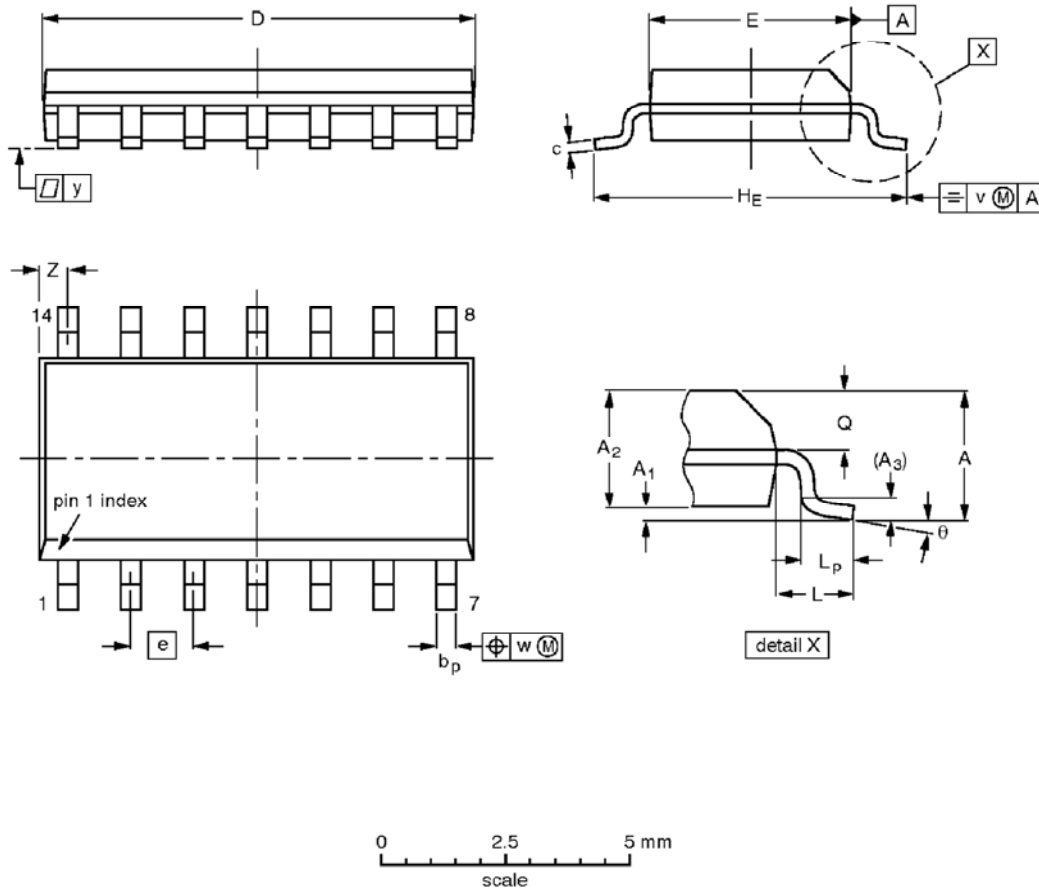
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

# Dual 2-wide 2-input, 2-wise 3-input AND-OR-invert gate

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**SO14:** plastic small outline package; 14 leads; body width 3.9 mm

**SOT108-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT108-1	076E06S	MS-012AB			<del>95-01-29</del> 97-05-22

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**NOTES**

## Dual 2-wide 2-input, 2-wise 3-input AND-OR-invert gate

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**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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