Monolithic CMOS Analog Switches

The DG401, DG403 and DG405 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

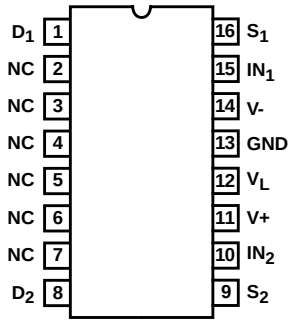
These switches feature low analog ON resistance (<45Ω) and fast switch time (t_{ON} < 150ns). Low charge injection simplifies sample and hold applications.

The improvements in the DG401/403/405 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $30V_{P-P}$ signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

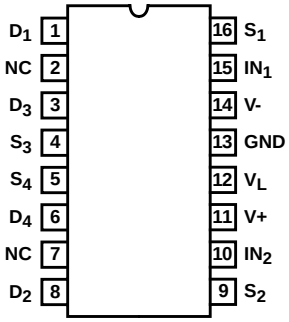
The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The three different devices provide the equivalent of two SPST (DG401), two SPDT (DG403) or two DPST (DG405) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

Pinouts

DG401 (PDIP, SOIC)
TOP VIEW



DG403, DG405 (SOIC)
TOP VIEW



NOTE: (NC) No Connection.

Features

- ON Resistance (Max) 45Ω
- Low Power Consumption (P_D) . . . . . <35µW
- Fast Switching Action
  - t_{ON} (Max) 150ns
  - t_{OFF} (Max) 100ns
- Low Charge Injection
- DG401 Dual SPST; Same Pinout as HI-5041
- DG403 Dual SPDT; DG190, IH5043, IH5151, HI-5051
- DG405 Dual DPST; DG184, HI-5045, IH5145
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
DG401DJ	-40 to 85	16 Ld PDIP	E16.3
DG401DY	-40 to 85	16 Ld SOIC	M16.15
DG403DJ	-40 to 85	16 Ld PDIP	E16.3
DG403DY	-40 to 85	16 Ld SOIC	M16.15
DG405DY	-40 to 85	16 Ld SOIC	M16.15

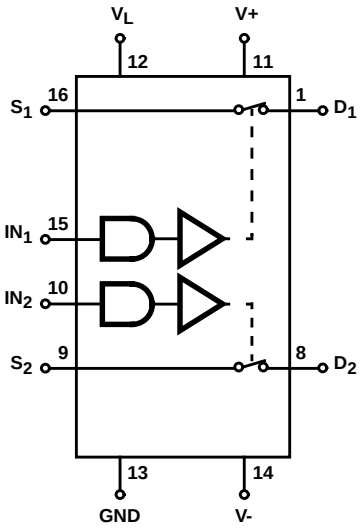
TRUTH TABLE

	DG401	DG403		DG405
LOGIC	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

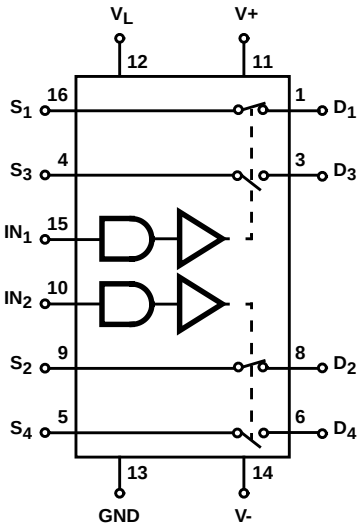
NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V.

Functional Diagrams

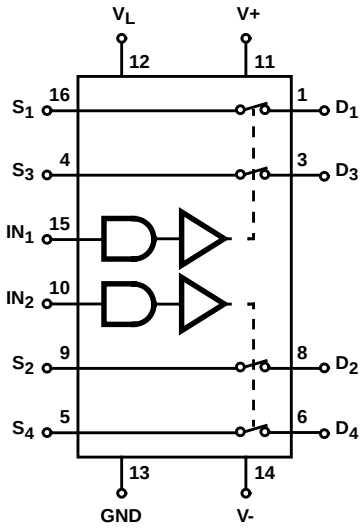
DG401



DG403

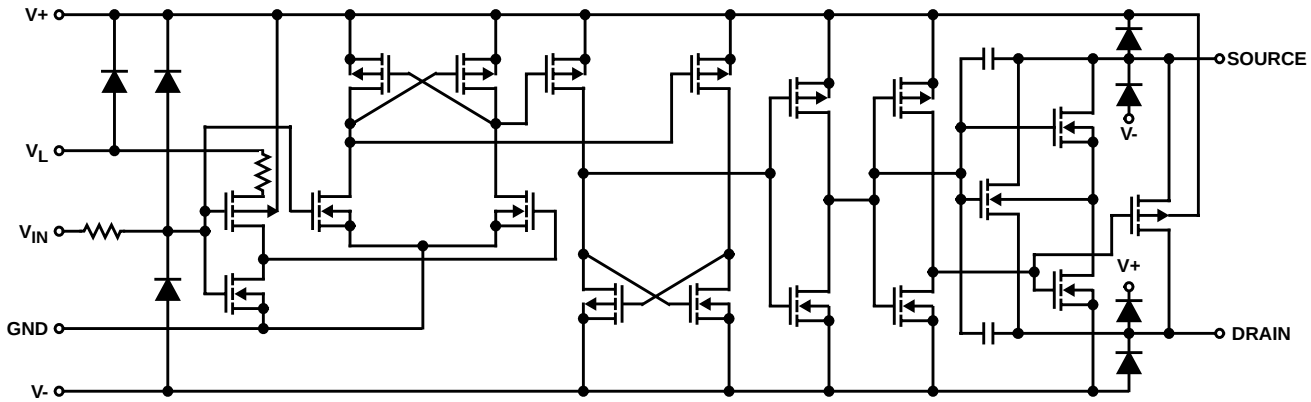


DG405



SWITCHES SHOWN FOR LOGIC “1” INPUT

Schematic Diagram



Absolute Maximum Ratings

V+ to V- 44.0V
GND to V-. 25V
V_L. . . . . (GND - 0.3V) to (V+) +0.3V
Digital Inputs V_S, V_D (Note 1) . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle, Max) . . 100mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	90
SOIC Package	115

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Voltage Range . . . . . ±20V (Max)
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V (Note 3), V_L = 5V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	(NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF	25	-	100	150	ns
Turn-OFF Time, t_{OFF}		25	-	60	100	ns
Break-Before-Make Time Delay (DG403), t_D	R_L = 300Ω, C_L = 35pF	25	5	12	-	ns
Charge Injection, Q (Figure 3)	C_L = 10nF, V_G = 0V, R_G = 0Ω	25	-	60	-	pC
OFF Isolation (Figure 4)	R_L = 100Ω, C_L = 5pF, f = 1MHz	25	-	72	-	dB
Crosstalk (Channel-to-Channel) (Figure 6)		25	-	-90	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_S = V_D = 0V (Figure 7)	25	-	12	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		25	-	12	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$		25	-	39	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Current with V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-1	0.005	1	µA
Input Current with V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-1	0.005	1	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = ∓10mA, V_D = ±10V	25	-	20	45	Ω
		Full	-	-	55	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V+ = 16.5V, V- = -16.5V, I_S = -10mA, V_D = 5, 0, -5V	25	-	3	3	Ω
		Full	-	-	5	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5 V_D = ±15.5V, V_S = ∓15.5V	25	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		25	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Channel ON Leakage Current, $I_{D(ON)}$ + $I_{S(ON)}$	V± = ±16.5V, V_D = V_S = ±15.5V	25	-1	-0.04	1	nA
		Full	-10	-	10	nA

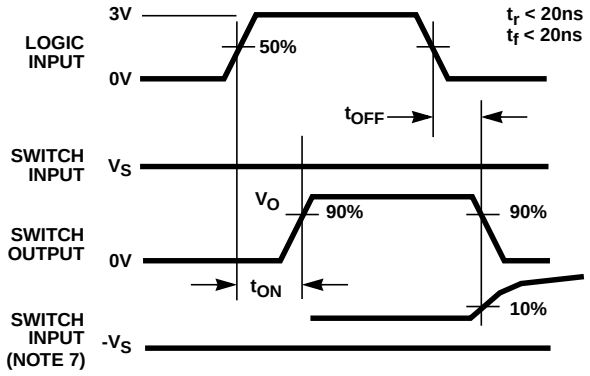
Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V (Note 3), V_L = 5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	(NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	25	-	0.01	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-		25	-1	-0.01	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.01	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.01	-	µA
		Full	-5	-	-	µA

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

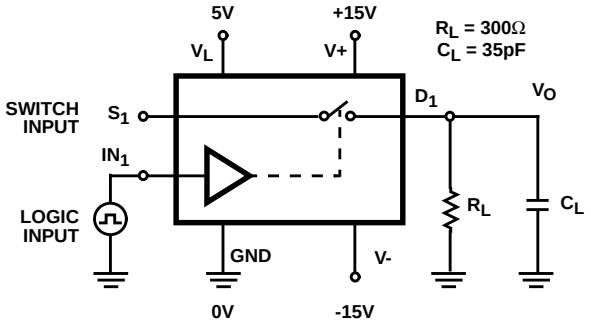
Test Circuits and Waveforms



NOTES:

6. Logic input waveform is inverted for switches that have the opposite logic sense.
7. V_S = 10V for t_{ON}, V_S = -10V for t_{OFF}.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for IN_2 and S_2.
For load conditions, see Specifications. C_L includes fixture and stray capacitance.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

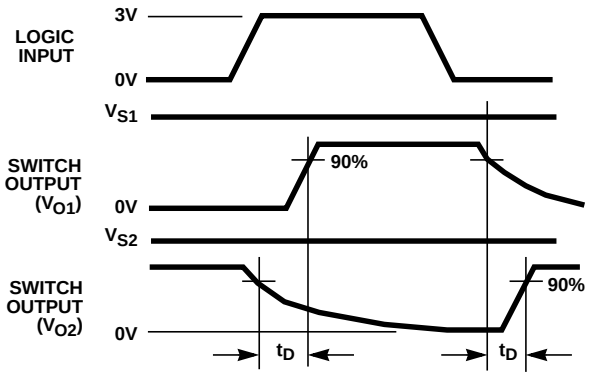
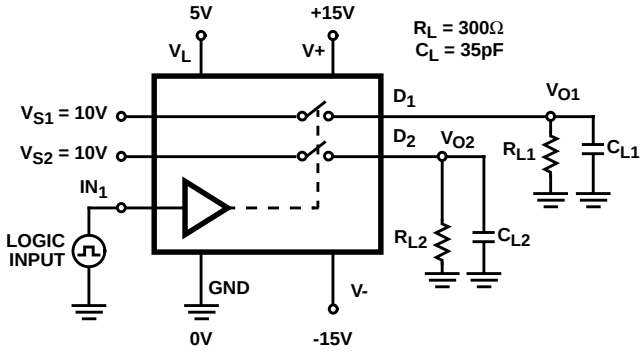


FIGURE 2A. MEASUREMENT POINTS



C_L includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)

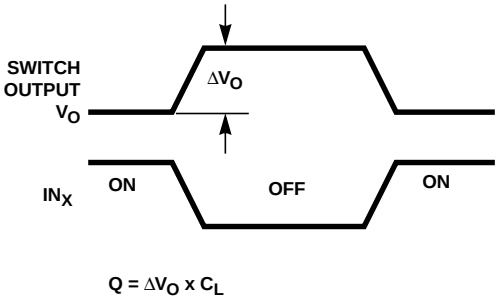


FIGURE 3A. MEASUREMENT POINTS

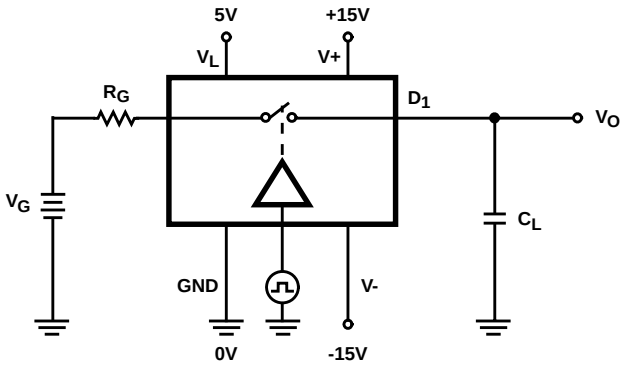


FIGURE 3B. TEST CIRCUIT

FIGURE 3. CHARGE INJECTION

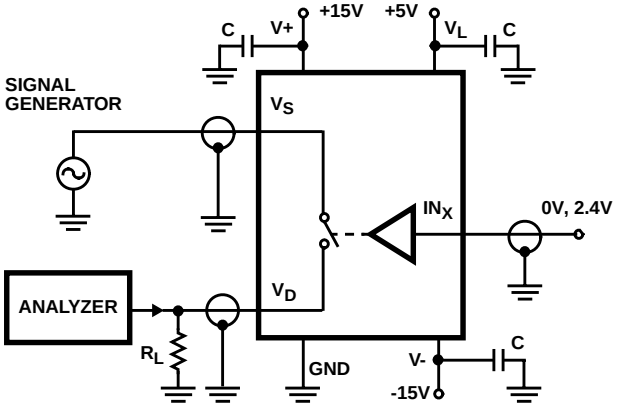


FIGURE 4. OFF ISOLATION TEST CIRCUIT

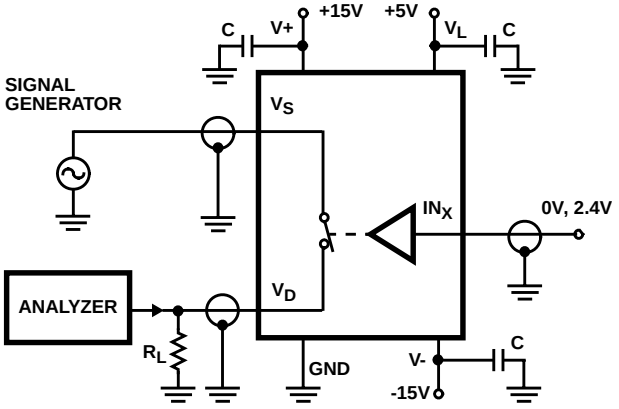


FIGURE 5. INSERTION LOSS TEST CIRCUIT

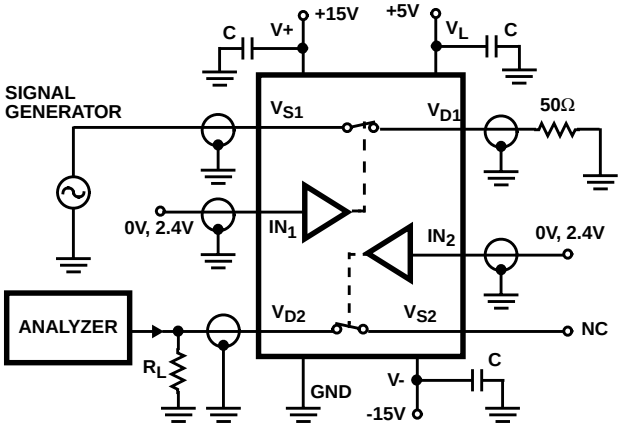


FIGURE 6. CROSSTALK TEST CIRCUIT

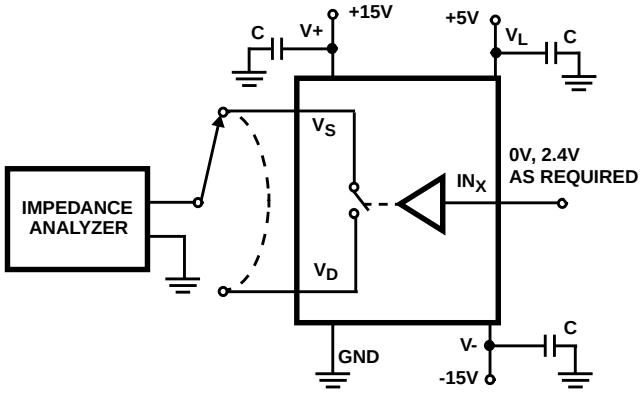


FIGURE 7. CAPACITANCES TEST CIRCUIT

Application Information

Dual Slope Integrators

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{IN} or discharges the capacitor in preparation for the next integration cycle.

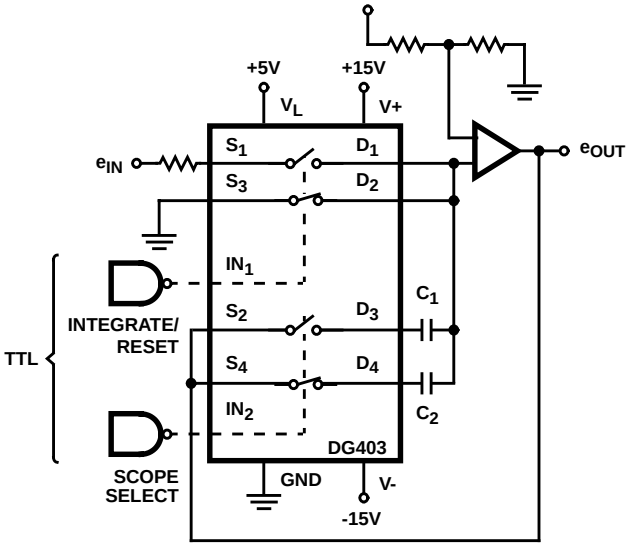


FIGURE 8. DUAL SLOPE INTEGRATOR

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1. The output of A_2 is fed back to A_3 and compared to the analog input e_{IN}. If $e_{IN} > e_{OUT}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{IN} goes below e_{OUT}, A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

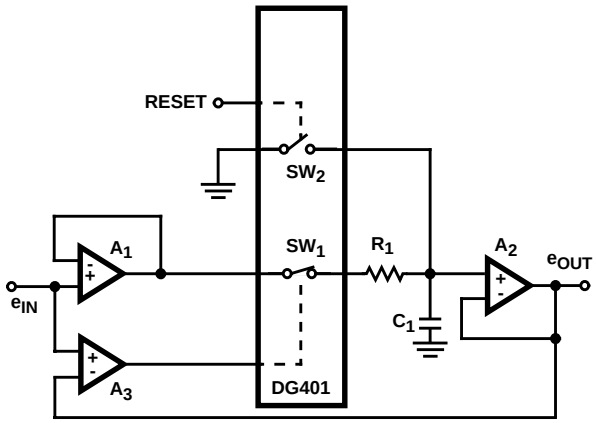


FIGURE 9. POSITIVE PEAK DETECTOR

Typical Performance Curves

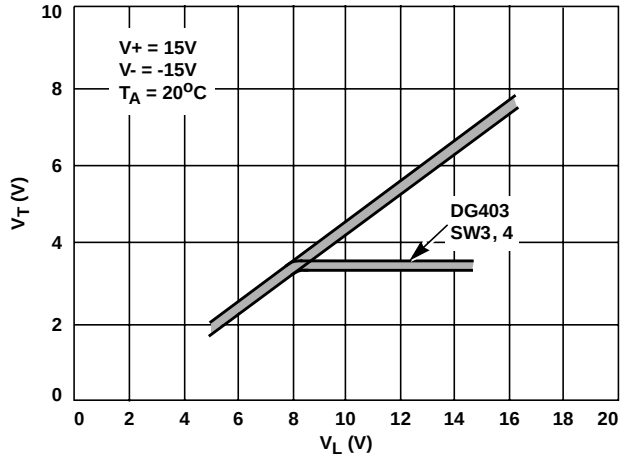


FIGURE 10. INPUT SWITCHING THRESHOLD vs LOGIC SUPPLY VOLTAGE

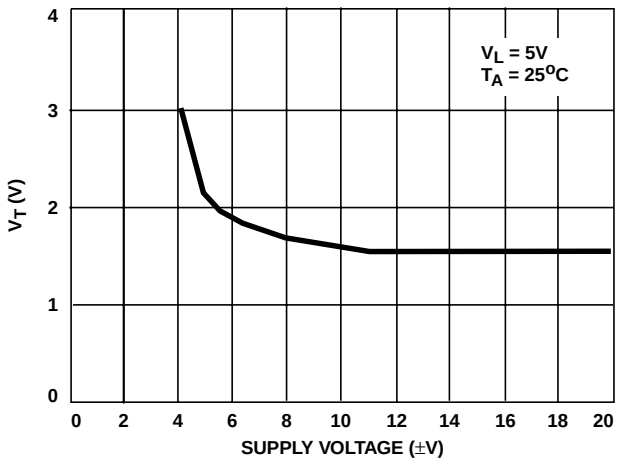


FIGURE 11. INPUT SWITCHING THRESHOLD vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

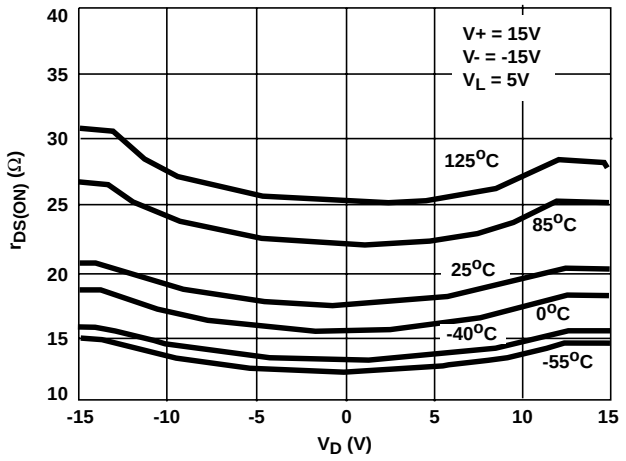


FIGURE 12. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

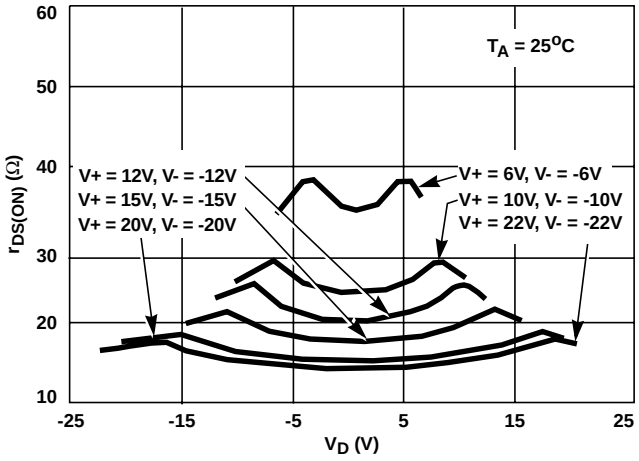


FIGURE 13. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

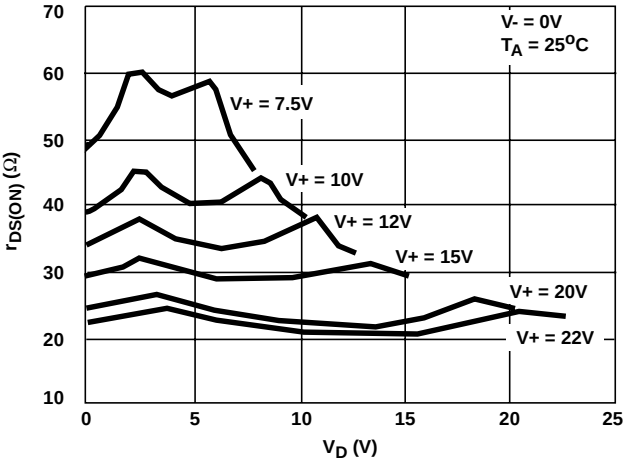


FIGURE 14. $r_{DS(ON)}$ vs V_D AND SINGLE SUPPLY VOLTAGE

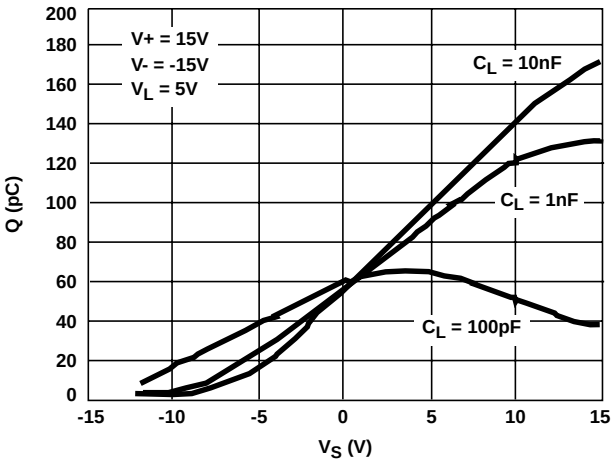


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE

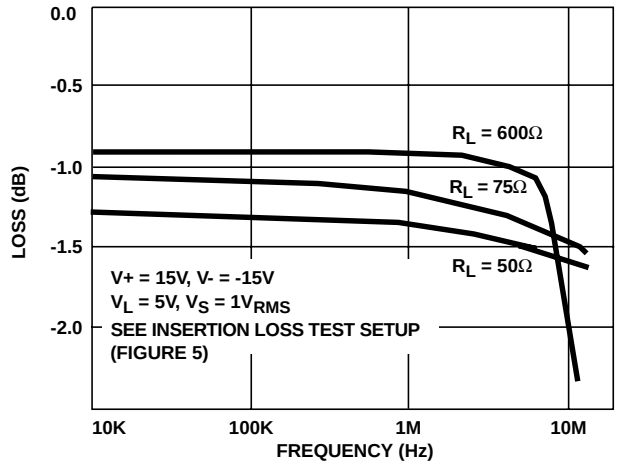


FIGURE 16. INSERTION LOSS vs FREQUENCY

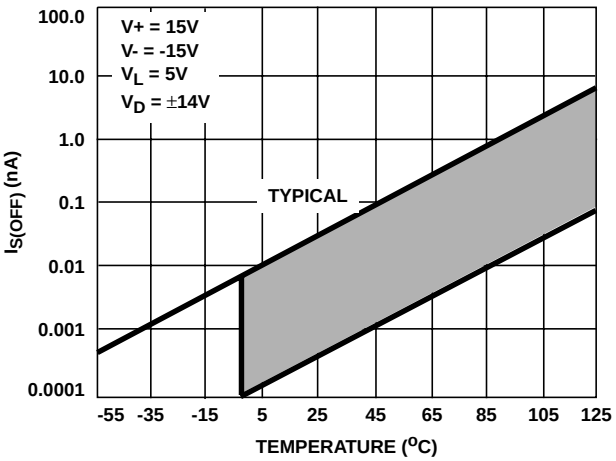


FIGURE 17. $I_{S(OFF)}$ vs TEMPERATURE

Typical Performance Curves (Continued)

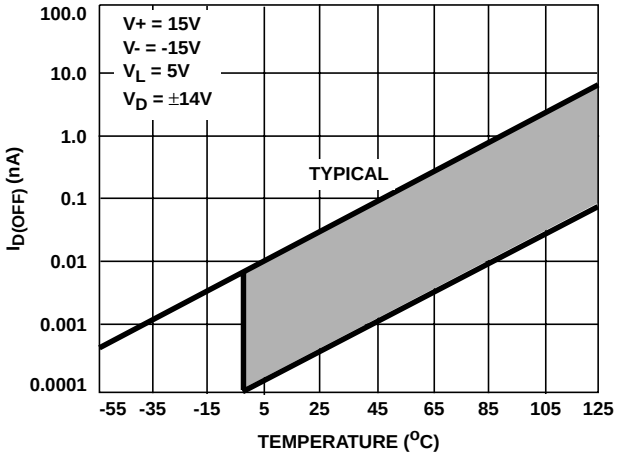


FIGURE 18. $I_{D(OFF)}$ vs TEMPERATURE

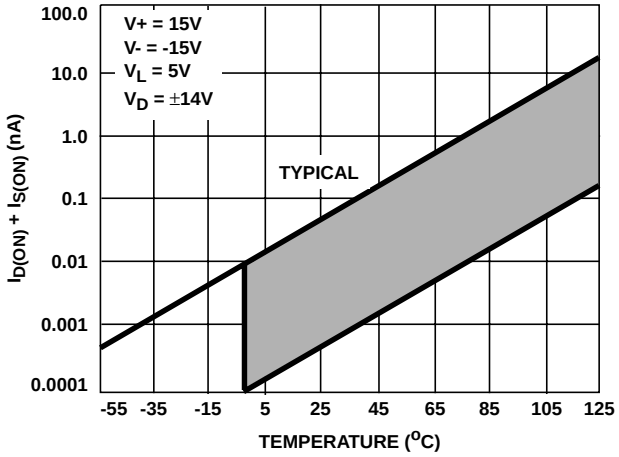


FIGURE 19. $I_{D(ON)} + I_{S(ON)}$ vs TEMPERATURE

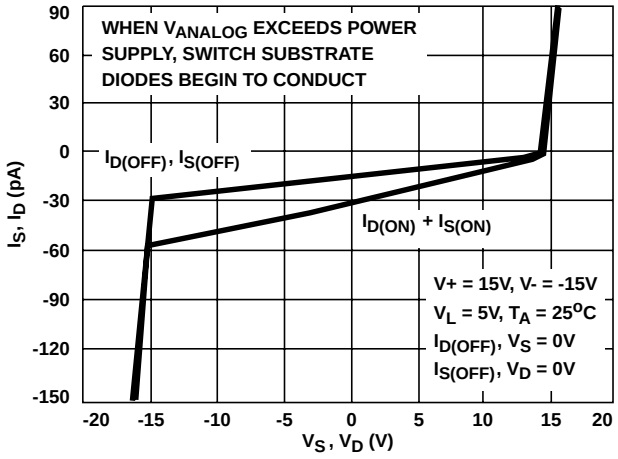


FIGURE 20. LEAKAGE CURRENTS vs ANALOG VOLTAGE

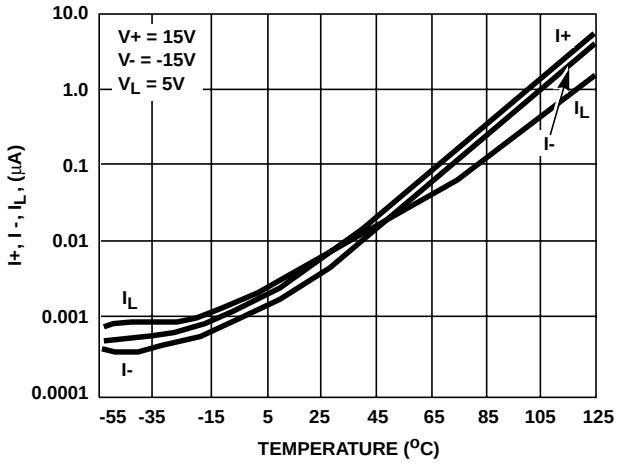


FIGURE 21. SUPPLY CURRENT vs TEMPERATURE

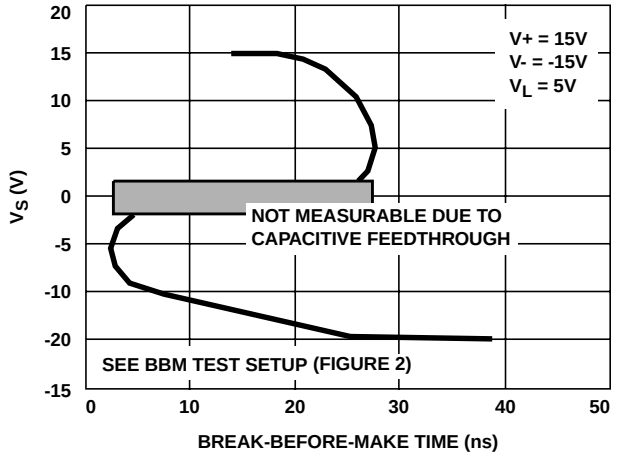


FIGURE 22. BREAK-BEFORE-MAKE vs ANALOG VOLTAGE

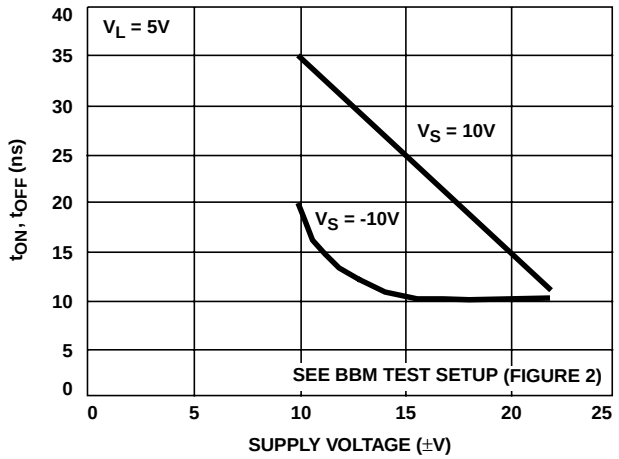


FIGURE 23. BREAK-BEFORE-MAKE vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

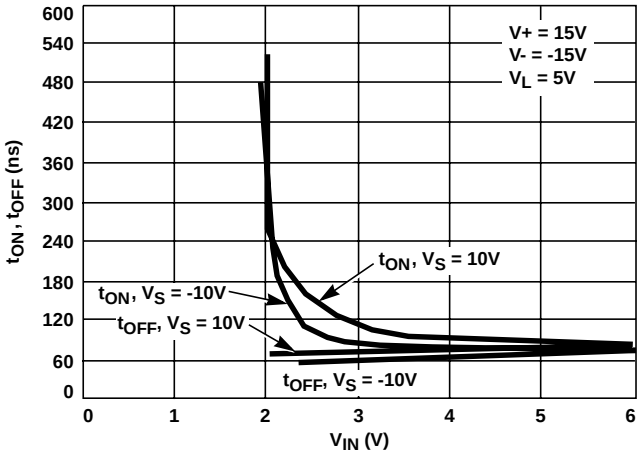


FIGURE 24. SWITCHING TIME vs INPUT LOGIC VOLTAGE (NOTE 8)

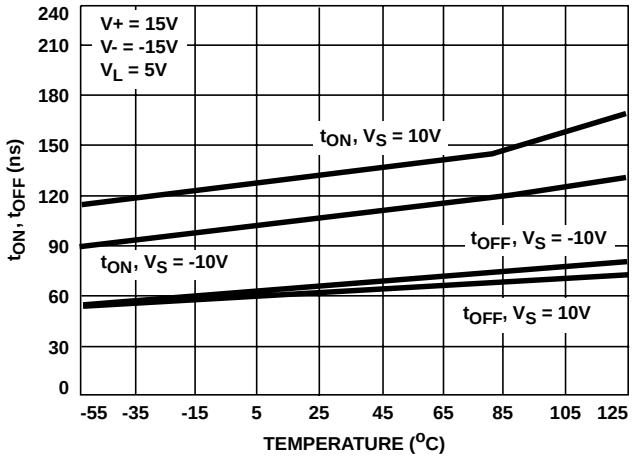


FIGURE 25. SWITCHING TIME vs TEMPERATURE (NOTE 8)

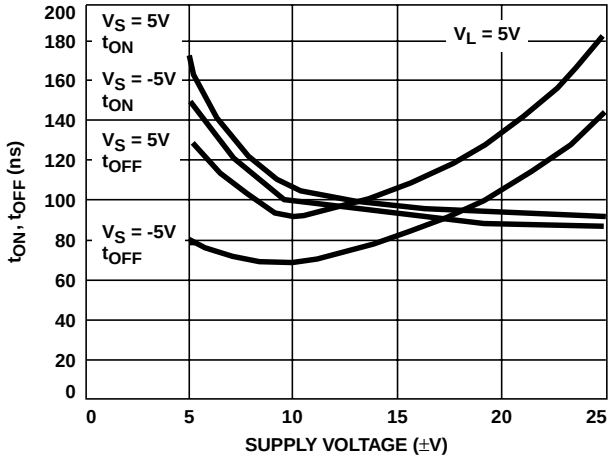


FIGURE 26. SWITCHING TIME vs POWER SUPPLY VOLTAGE (NOTE 8)

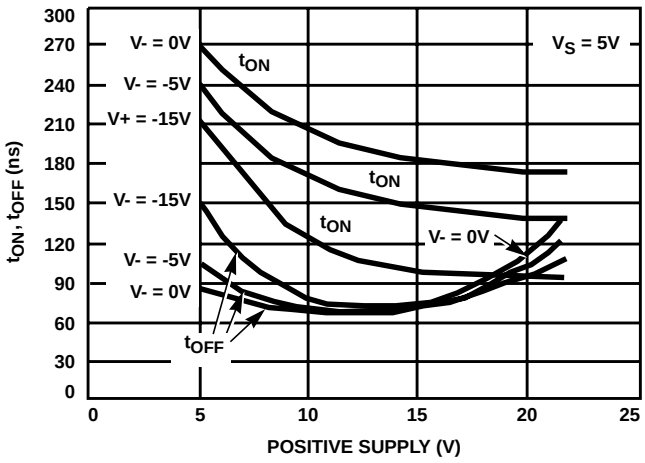


FIGURE 27. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 8)

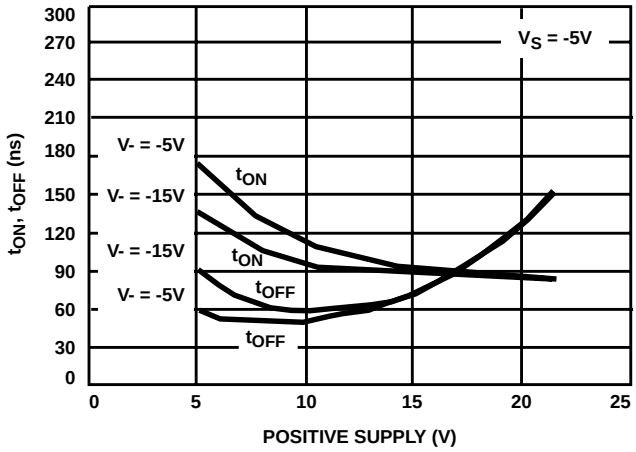


FIGURE 28. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 8)

NOTE:

8. Refer to Figure 1 for test conditions.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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