description (continued)

control block

The control block decodes the M2-M0 instruction inputs, 16B/$\overline{32B}$ configuration select, IP and OP data select/bit reversal options, and other control inputs and transmits the resulting control signals to the rest of the internal logic.

instruction set

The 'AS897A can operate in any of the eight user-programmable shift modes shown in Table 1. Selection of these instructions is controlled by pins M2-M0.

TABLE 1. INSTRUCTION SET

M2	M1	M0	DESCRIPTION
L	L	L	Shift right the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Fill vacated bit positions with logic level on S input. A high on ZN4 causes all bits in the 16-bit mode to be filled with the logic level on S.
L	L	H	Shift left the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Fill vacated bit positions with logic level on S input. A high on ZN4 causes all bits in the 16-bit mode to be filled with the logic level on S.
L	H	L	Circular right shift the number or bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode).
L	H	H	Circular left shift the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode).
H	L	L	Shift right the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Fill vacated bit positions with logic level on S input. Merge result with data from the register/counter. A high on ZN4 causes all bits in the 16-bit mode to be filled with the logic level on S.
H	L	H	Shift left the number of bit positions defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Fill vacated bit positions with logic level on S input. Merge result with data from the register/counter. A high on ZN4 causes all bits in the 16-bit mode to be filled with the logic level on S.
H	H	L	Set the bit position defined by ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode) to the logic level on the S input.
H	H	H	If $\overline{NORM}$ is low, shift data left the number of bit positions defined by the leading-zero detector. Fill vacated bit positions with logic level on S input. Output number of leading zeros in D15-D0 on ZN3-ZN0 (16-bit mode) or ZN4-ZN0 (32-bit mode). Note: If $\overline{NORM}$ is high, this instruction performs like the left shift described above for M2 = L, M1 = L, M0 = H.

mode configuration

The 'AS897A can be configured to operate on 16-bit or 32-bit words. Configuration is controlled by 16B/$\overline{32B}$. When 16B/$\overline{32B}$ is high, the 'AS897A operates in 16-bit mode.

Figure 1 illustrates the connection of four 'AS897As to provide a 32-bit barrel shifter that can perform all Table 1 shift instructions. For 32-bit mode operation, the 16B/$\overline{32B}$ inputs of all 'AS897A devices must be low and should be configured as shown in Figure 1.

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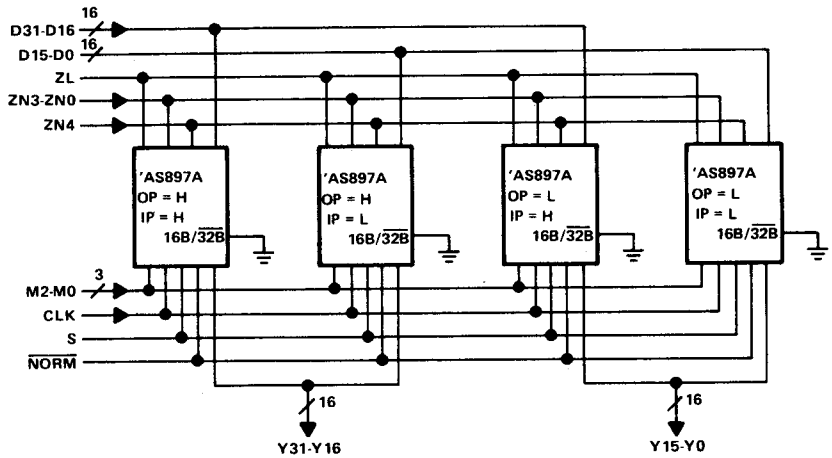

FIGURE 1. 32-BIT BARREL SHIFTER

data input/output

Data can be input to the chip from two ports: D15-D0, which passes data to the zero detector and to the shifter via the data select and bit-reversal multiplexers, and Y15-Y0, which passes data to the register/counter. Y15-Y0 is also used to output the shift result from the chip.

Data input and output positions in the 32-bit mode are defined by IP and OP (see Table 2). When IP is high, the D15-D0 port is the most significant input position; when IP is low, the D15-D0 input port is the least significant. If OP is high, the Y15-Y0 port is the most significant output position; if OP is low, the Y15-Y0 port is the least significant position.

TABLE 2. IP AND OP CONTROLS

SIGNAL	16-BIT OPERATION (16B/$\overline{32B}$ = H)	32-BIT OPERATION (16B/$\overline{32B}$ = L)
IP = L	Bit-reversal option off	D15-D0 is least significant input position
IP = H	Bit-reversal option on	D15-D0 is most significant input position
OP = L	D15-D0 is shifted	Y15-Y0 is least significant output position
OP = H	Register/counter data is shifted	Y15-Y0 is most significant output position

zero detector

The zero detector detects the number of leading zeros at the D15-D0 input port. If HEX/$\overline{BIN}$ is high, the zero detector counts only those binary zeros that are part of a leading hexadecimal zero group. For example, given the binary number 0000 0000 0001 0001, the leading-zero count will be decimal 11 if HEX/$\overline{BIN}$ is low and decimal 8 if HEX/$\overline{BIN}$ is high.

If all zeros are detected at the D port, the ZL output transistor will be turned off. If the ZL output pin is pulled up through the recommended pull-up resistor (see pin description table), the resulting signal will be high. If anything other than a zero is detected on the D15-D0 inputs, the output transistor will be turned on; this will pull the ZL signal low.

During data normalization (M2 = H, M1 = H, M0 = H), the zero-detector outputs the leading zero count to the ZN4-ZN0 I/O ports, provided $\overline{NORM}$ is low. When $\overline{NORM}$ is high, ZN4-ZN0 act only as inputs in this mode. For operations other than normalization, the state of $\overline{NORM}$ is irrelevant.

In the data-normalization mode, a high logic level will be output on the ZN4 pin when the D15-D0 bus contains all lows and $\overline{NORM}$ is low (see Table 3).

TABLE 3. ZN4 I/O PORT

SIGNAL	I/O	16-BIT CONFIGURATION (16B/$\overline{32B}$ = H)	32-BIT CONFIGURATION (16B/$\overline{32B}$ = L)
ZN4	I	In shift-left, shift-right, and shift-and-merge modes, a high fills all bits with the logic level on the S input. Inactive in other modes.	With ZN3-ZN0 indicates number of bits to be shifted in shift operations and position of bit to be replaced in replace-bit mode.
	O	In the normalization mode, when $\overline{NORM}$ = L, indicates when the input to the shifter is zero	In the normalization mode, when $\overline{NORM}$ = L, ZN4-ZN0 indicates number of leading zeros detected in D15-D0 and number of places to be shifted for normalization.

data selector multiplexer

The data selector multiplexer is used only in 16-bit operation (16B/$\overline{32B}$ = H). OP controls the mux and selects the data to be presented to the bit-reversal block. OP high selects the register/counter; OP low selects D15-D0 (see Table 2).

bit reversal

Bit reversal is also available only in the 16-bit mode (16B/$\overline{32B}$ = H) and is controlled by IP (see Table 2). When the bit-reversal option is selected (IP = H), data selected by OP is bit-reversed before it is passed to the shifter: the most significant bit becomes the least significant bit, the second most significant bit becomes the second least significant bit, and so forth. When the bit-reversal option is off (IP = L), the data presented to the shifter is not altered.

register/counter

During most instructions, the register/counter operates as a data latch. Data on the Y15-Y0 bus is latched into the register/counter on the rising edge of the clock. Data can be input to the register/counter from the shifter ($\overline{OEY}$ = L) or from the bidirectional Y port ($\overline{OEY}$ = H).

In the 16-bit circular-shift mode (16B/$\overline{32B}$ = H, M2 = L, M1 = H, M0 = X), the register counter will function as a 16-bit counter on the rising edge of the clock when S is high. Under these same conditions, the register/counter will function as four 4-bit counters when $\overline{TP}$ is low. In the 16-bit circular-shift mode, the register/counter functions as a register when S is low. The counter option is not available for other instructions in the 16-bit mode or for any instructions in the 32-bit mode.

shifter

The shifter performs the operations specified by the M2-M0 inputs (see Table 1). The number of bits to be shifted or the position of the bit to be replaced is specified by ZN3-ZN0 (16-bit operation) or ZN4-ZN0 (32-bit operation).

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merge

During the shift and merge instruction (M2 = H, M1 = L, M0 = X), the merge block ORs the shift result with data from the register/counter.

S or Z fill

During bit replacement (M2 = H, M1 = H, M0 = L) in the 16-bit mode, this block sets the bit specified on the ZN3-ZN0 inputs with the logic level on the S input. This option works identically in the 32-bit mode, except that the bit to be replaced is specified on the Z4-Z0 inputs. During all other instructions except circular shifts, the S input specifies the logic level that will fill the bit position or positions vacated during the shift.

Z fill is used in the 32-bit mode to selectively put the device outputs in a high-impedance state. This feature is necessary to properly select the correct bit locations that will combine to form the shifted output. An example of a 32-bit circular shift four positions to the right, which illustrates the Z-fill technique, is shown in Figure 2.

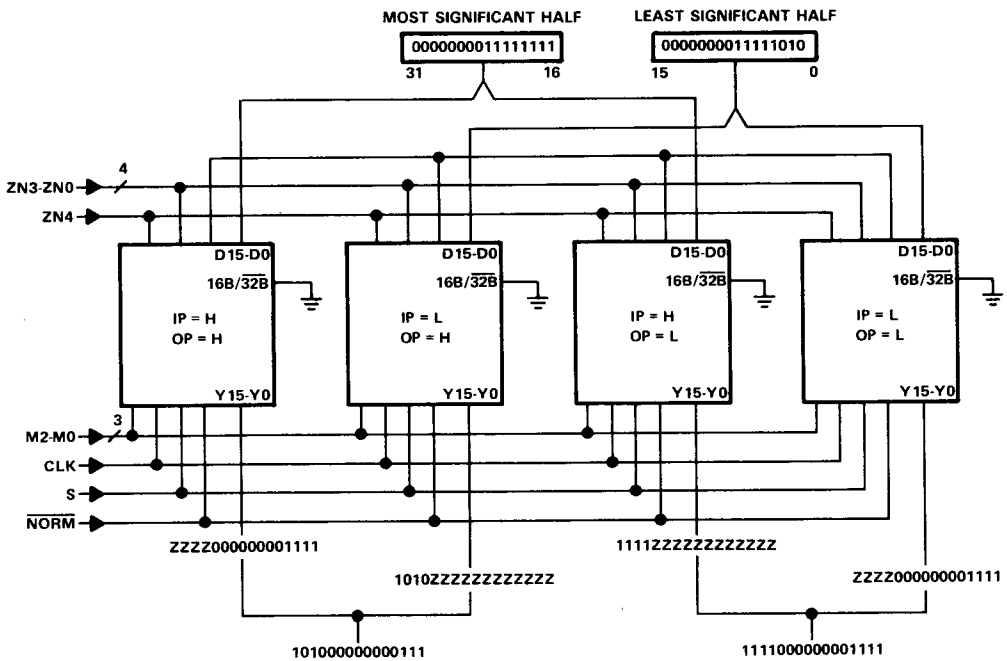

FIGURE 2. 32-BIT Z-FILL TECHNIQUE

SHIFT OPERATION EXAMPLES

Examples of 'AS897A shift instructions are provided in the following paragraphs. Unless otherwise specified, the examples assume a 16-bit configuration.

shift left or right (M2 = L, M1 = L, M0 = X)

When in the shift-right (M0 = L) or shift-left (M0 = H) modes, ZN3-ZN0 define the number of bit positions to be shifted. If, for example, ZN3-ZN0 is equal to a decimal 10, the data selected by OP will be shifted 10 bit positions. The positions vacated during the shift operation are filled with the logic level being applied to the S input. $\overline{\text{NORM}}$ is inactive in all shift modes except normalization and is therefore shown as a don't care. If IP is high, the data selected by OP will be bit-reversed before it is passed to the shifter.

Example

Shift a 16-bit word on the data bus ten positions to the left and fill the least significant bits with highs.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	BIT REVERSAL	DATA SOURCE	BIT FILL	CONFIGURATION
M2-M0	$\overline{\text{NORM}}$	ZN4-ZN0	IP	OP	S	16B/$\overline{32B}$
001	X	01010	0	0	1	1

Assume D15-D0 contains hex AF50:

	D15-D0
Input Data	1010 1111 0101 0000
	Y15-Y0
Result	0100 0011 1111 1111

Example

Shift a 32-bit word on the data bus 20 positions to the right. Fill vacated bit positions with highs.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	BIT REVERSAL	DATA SOURCE	BIT FILL	CONFIGURATION
M2-M0	$\overline{\text{NORM}}$	ZN4-ZN0	IP	OP	S	16B/$\overline{32B}$
000	X	10100	See Figure 1		1	1

Assume D15-D0 contains hex 75BB FCAE:

	D31-D16	D15-D0
Input Data	0111 0101 1011 1011	1111 1100 1010 1110
	Y31-Y16	Y15-Y0
Result	1111 1111 1111 1111	1111 0111 0101 1011

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circular shift left or right (M2 = L, M1 = H, M0 = X)

In this mode, data selected by OP is circular shifted left (M0 = H) or right (M0 = L) the number of bit positions specified by ZN3-ZN0. If, for example, the device is in the circular-shift-right mode (M0 = L) and ZN3-ZN0 contains a decimal five, the data selected by OP will be shifted right five positions.

In all shift modes except 16-bit circular, the S input contains the bit used for end fill or bit replacement. In the 16-bit circular-shift mode, the S input controls whether the register/counter will operate as a 16-bit counter or as a data register. When S is high, the register/counter operates as a 16-bit binary counter; when S is low, the register/counter operates as a 16-bit data latch. Both functions are controlled on the positive edge of the CLK input. Data on Y15-Y0 will be latched into the register/counter on the rising edge of the clock when S is low.

Example

Circular shift a 16-bit word in the register/counter five positions to the right.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	BIT REVERSAL	DATA SOURCE	LATCH OR COUNTER	CONFIGURATION
M2-M0	$\overline{\text{NORM}}$	ZN4-ZN0	IP	OP	S	16B/$\overline{32B}$
010	X	X0101	0	1	0	1

Assume the register/counter contains hex A016:

	Register/Counter
Input Data	1010 0000 0001 0110
	Y15-Y0
Result	1011 0101 0000 0000

shift and merge (M2 = H, M1 = L, M0 = X)

In the shift-and-merge mode, data selected by OP is shifted by OP is shifted left (M0 = H) or right (M0 = L) the number of positions specified by ZN3-ZN0, bit positions vacated by the shift are filled by the logic level on S, and the result is ORed with data in the register/counter.

Example

Shift data on the data bus six positions to the left, and fill vacated positions with zeros. Merge the shifted data with data from the data register.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	BIT REVERSAL	DATA SOURCE	END FILL	CONFIGURATION
M2-M0	$\overline{\text{NORM}}$	ZN4-ZN0	IP	OP	S	16B/$\overline{32B}$
100	X	00110	0	0	0	1

Assume D15-D0 contains hex 6174 and register/counter contains hex 320B:

	D15-D0
Input Data	0110 0001 0111 0100

	Shift Result
Intermediate Result	0101 1101 0000 0000

	Register/Counter
Input Data	0011 0010 0000 1011

	Y15-Y0
Result	0111 1111 0000 1011

bit replacement (M2 = H, M1 = H, M0 = L)

In the bit-replacement mode, data in the bit position specified by ZN3-ZN0 is replaced by the logic level on the S input. If, for example, ZN3-ZN0 contains a decimal seven and S contains a logic high, bit 7 of the data selected by OP will be set high regardless of its original state. In the following example, OP has been set high to select data from the register/counter. Because IP has been set high, the data will be bit-reversed before it enters the shifter.

Example

Bit-reverse the data in the register/counter and set bit 7 of the result to zero.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	POSITION OF BIT TO BE INSERTED	BIT REVERSAL	DATA SOURCE	INSERT BIT	CONFIGURATION
M2-M0	$\overline{NORM}$	ZN4-ZN0	IP	OP	S	16B/$\overline{32B}$
110	X	X0111	1	1	0	1

	Register/Counter
Input Data	0110 0001 0011 0100

	Result after Bit-Reversal
Intermediate Result	0010 1100 1000 0110

	Y15-Y0
Result	0010 1100 0000 0110

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data normalization (M2 = H, M1 = H, M0 = L)

The data-normalization mode shifts data on D15-D0 to the left until a high logic level appears in the most-significant-bit position of output Y15-Y0 if HEX/$\overline{\text{BIN}}$ is low. If HEX/$\overline{\text{BIN}}$ is high, only 4-digit groups containing leading zeros are shifted left. The number of positions shifted to accomplish this is determined by the leading-zero detector. This count will be output on ZN3-ZN0 when the $\overline{\text{NORM}}$ input is low.

Since the leading-zero detector counts leading zeros in the D15-D0 input, the normalization is designed to operate on data from the data bus rather than the register/counter. Therefore OP is set low in the following example. The S input is programmed low so that all bit positions vacated during the shift will be filled with zeros.

Example

Perform a hex normalization on a 16-bit data word from the data bus.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO BE SHIFTED	LEADING-ZERO MODE	BIT REVERSAL	DATA SOURCE	INSERT BIT	CONFIGURATION
M2-M0	$\overline{\text{NORM}}$	ZN4-ZN0	HEX/$\overline{\text{BIN}}$	IP	OP	S	16B/$\overline{32B}$
111	0	Outputs leading zero count	1	0	0	0	1

Assume D15-D0 contains hex 002B:

	D15-D0
Input Data	0000 0000 0010 1011
	ZN3-ZN0
Leading-Zero Count	1000
	Y15-Y0
Result	1010 1011 0000 0000

Example

Perform a binary normalization on a 32-bit word from the data bus.

CONTROL SIGNALS

SHIFT INSTRUCTION	NORMALIZE	NUMBER OF BITS TO SHIFT	LEADING-ZERO MODE	BIT REVERSAL	DATA SOURCE	BIT FILL	CONFIGURATION
M2-M0	$\overline{\text{NORM}}$	ZN4-ZN0	HEX/$\overline{\text{BIN}}$	IP	OP	S	16B/$\overline{32B}$
111	0	Outputs leading zero count	0	See Figure 1		0	0

Assume D31-D0 contains hex 0000 3D61:

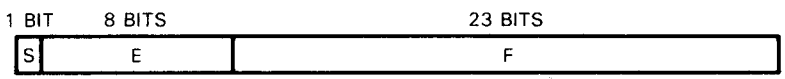
	D31-D16	D15-D0
Input Data	0000 0000 0000 0000	0011 1101 0110 0001

	ZN4-ZN0
Leading-Zero Count	10010

	Y31-Y16	Y15-Y0
Result	1111 0101 1000 0100	0000 0000 0000 0000

IEEE floating-point normalization

Floating-point normalization is used to preserve number resolution after subtraction or some other floating-point algorithm that results in orders of magnitude reduction. Three 'AS897A devices can be configured to convert a 32-bit data word into the IEEE floating-point format shown in Figure 3.



S — sign bit
E — 8-bit exponent
F — 23-bit fraction

FIGURE 3. IEEE FLOATING-POINT FORMAT

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Figure 4 shows the three-device configuration. The limitation of this application is that only 23 bits of the 32 bits are used in the significand, and the sign bit must be set from hardware. As an alternate to the IEEE floating-point format, the same hardware configuration can be used to normalize a 32-bit data word resulting in a 32-bit significand and a five-bit exponent.

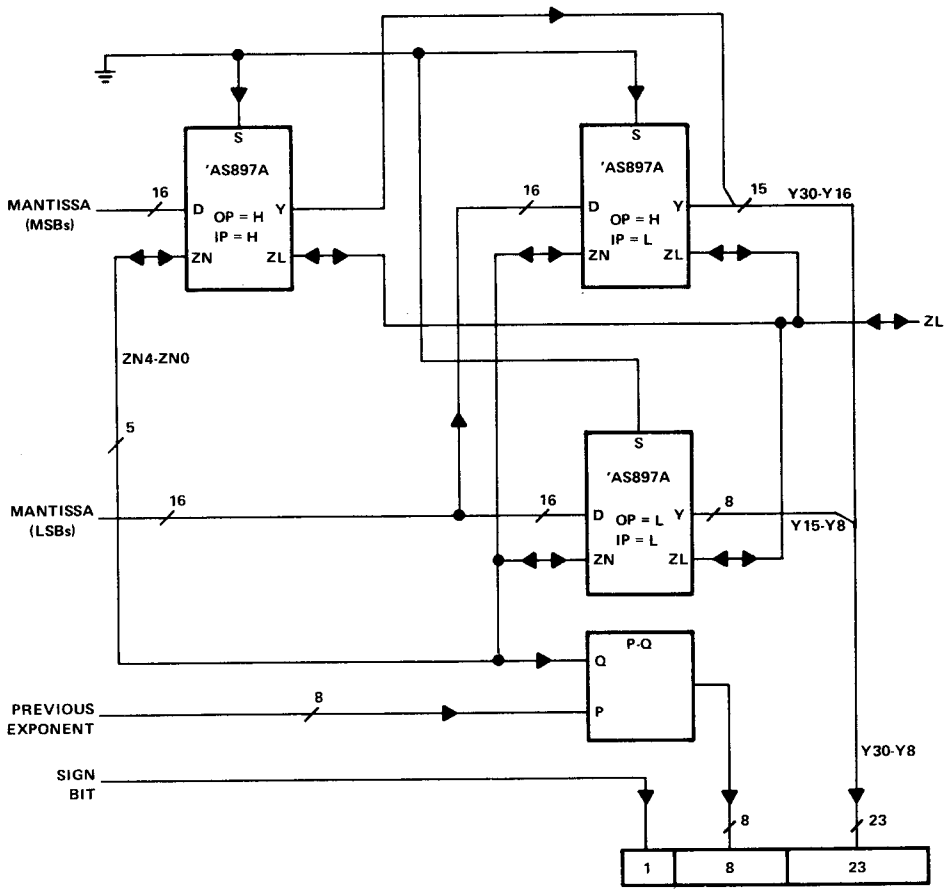

FIGURE 4. THREE-DEVICE CONFIGURATION FOR IEEE FLOATING-POINT FORMAT

Example

Input data in IEEE floating point format

Sign Bit	Previous Exponent	Mantissa
1	0010 1001	000 1001 0001 0001 0001 0001

Input mantissa concatenated with: 0 0000 0000 to D31-D0 of the 'AS897As

D31-D16	D15-D0
0001 0010 0010 0010	0010 0010 0000 0000

Normalize mantissa and output the leading zero count on ZN4-ZN0.

D31-D16	D15-D0	ZN4-ZN0
1001 0001 0001 0001	0001 0000 0000 0000	00011

Pack result in IEEE floating point format
Note: Exponent = old exponent − ZN4-ZN0

Sign Bit	Exponent	Mantissa
1	0010 0110	001 0001 0001 0001 0001 0000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 3 V
Input voltage: I/O ports . . . . . 5.5 V
All other inputs . . . . . 7 V
Operating case temperature range: SN54AS897A . . . . . −55°C to 125°C
Operating free-air temperature range: SN74AS897A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

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recommended operating conditions

			SN54AS897A			SN74AS897A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC1}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{CC2}	Supply voltage		1.9	2	2.1	1.9	2	2.1	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	ZL			5.5			5.5	V
I_{OH}	High-level output current	ZN4-ZN0			−0.4			−0.4	mA
		Y15-Y0			−1			−2.6	
I_{OL}	Low-level output current	ZN4-ZN0			4			8	mA
		ZL, Y15-Y0			12			24	
t_w	Pulse duration	CLK low	10			10			ns
		CLK high	10			10			
t_{su}	Setup time before CLK↑	Y15-Y0	10			10			ns
		S↑	15			14			
		M0, M1, M2↑	15			14			
		16B/$\overline{32B}$‡	20			18			
t_h	Hold time after CLK↑	Y15-Y0‡	2			2			ns
		S↑	0			0			
		M0, M1, M2↑	0			0			
		16B/$\overline{32B}$‡	8			8			
T_A	Operating free-air temperature		−55			0		70	°C
T_C	Operating case temperature				125				°C

† These parameters only apply in the circular mode and with 16B/$\overline{32B}$ high.
‡ These parameters only apply in the circular mode.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS897A			SN74AS897A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = 18 mA			−1.5			−1.5	V
I_{OH}	ZL	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	Y15-Y0	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.2					V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	ZN4-ZN0	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	ZL, Y15-Y0	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	I/O ports‡	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	I/O ports‡	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	All inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC1}		V_{CC} = 5.5 V,	See Note 1			100			90	mA
I_{CC2}		V_{CC} = 2.1 V,	See Note 1			180			170	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: Supply currents I_{CC1} and I_{CC2} are measured with M0, M1, M2, IP, OP, S, ZN3-ZN0, D15-D0, and $\overline{OEY}$ low; 16B/$\overline{32B}$, $\overline{NORM}$, and CLK high; and Y15-Y0, ZL, and ZN4 open.

switching characteristics over recommended operating temperature range

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
			SN54AS897A		SN74AS897A		
			MIN	MAX	MIN	MAX	
t_{pd}	D15-D0	Y15-Y0		37		33	ns
	S	Y15-Y0		20		17	
	ZN3-ZN0	Y15-Y0		24		22	
	IP	Y15-Y0		33		29	
	OP	Y15-Y0		33		29	
	M0, M1, M2	Y15-Y0		24		21	
	CLK†	Y15-Y0		47		42	
	D15-D0	ZL		28		27	
	D15-D0‡	ZN4-ZN0		28		26	
t_{en}	M0, M1, M2§	ZN4-ZN0		25		20	ns
	16B/$\overline{32B}$	Y15-Y0		29		26	
	$\overline{NORM}$‡	ZN3-ZN0		26		21	
	$\overline{OEY}$	Y15-Y0		22		19	
	ZN4, ZL	Y15-Y0		32		29	
t_{dis}	M0, M1, M2§	ZN4-ZN0		22		20	ns
	16B/$\overline{32B}$	Y15-Y0		31		27	
	$\overline{NORM}$‡	ZN3-ZN0		14		12	
	$\overline{OEY}$	Y15-Y0		10		9	
	ZN4, ZL	Y15-Y0		30		26	

† This parameter applies only to the circular mode with S high and OP high.
‡ These parameters apply only to the normalization mode.
§ These parameters apply only to the 32-bit mode (16B/$\overline{32B}$ = L).

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