19-2962; Rev 1; 10/03

EVALUATION KIT AVAILABLE

5-Output Power-Management IC For Low-Cost PDAs

General Description

The MAX1559 is a complete power-management chip for low-cost personal digital assistants (PDAs) and portable devices operating from a 1-cell lithium-ion (Li+) or 3-cell NiMH battery. It includes all the regulators, outputs, and voltage monitors necessary for small PDAs while requiring a bare minimum of external components. Featured are four linear regulators, a DC-DC boost converter for LCD bias, a microprocessor reset output, and low-battery shutdown in a miniature QFN package. For a compatible Li+ charger for both USB and AC adapter inputs, refer to the MAX1551.

The four linear regulators feature PMOS pass elements for efficient low-dropout operation. A MAIN LDO supplies 3.3V at 500mA. A signal-detect (SD) card-slot output supplies 3.3V at 400mA. The COR1 LDO outputs 1V at 250mA, and the COR2 LDO supplies 1.8V at 30mA. The SD output and COR2 LDO have pin-controlled shutdown. For other output-voltage combinations, contact Maxim.

The DC-DC boost converter features an on-board MOSFET and True Shutdown™ when off. This means that during shutdown, input power is disconnected from the inductor so that the boost output falls to 0V rather than remaining one diode drop below the input voltage.

A µP reset output clears when the MAIN LDO achieves regulation to ensure an orderly start. Thermal shutdown protects the die from overheating.

The MAX1559 operates from a 3.1V to 5.5V supply and consumes 50mA of no-load supply current. It is packaged in a 1.3W, 16-pin thin QFN with a power pad on the underside of the package. The MAX1559 is specified for operation from -40°C to +85°C.

Applications

PDAs

Organizers

Cellular and Cordless Phones

MP3 Players

Hand-Held Devices

True Shutdown is a trademark of Maxim Integrated Products, Inc.

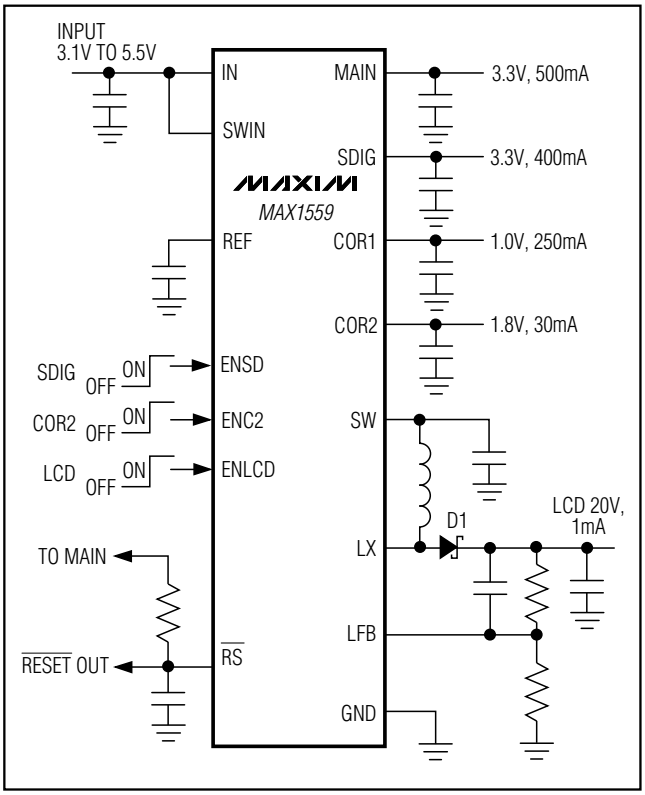
Features

- **Minimal External Components**
- **3.3V, 500mA MAIN LDO**
- **3.3V, 400mA SD Card Output**
- **1V, 250mA Core LDO**
- **1.8V, 30mA Second Core LDO**
- **High-Efficiency LCD Boost**
- **LCD 0V True Shutdown when Off**
- **50µA Quiescent Current**
- **3.1V to 5.5V Input Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1559ETE	-40°C to +85°C	16 Thin QFN

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

5-Output Power-Management IC For Low-Cost PDAs

ABSOLUTE MAXIMUM RATINGS

IN, SWIN, ENSD, ENC2, ENLCD, $\overline{RS}$, SDIG to GND .....-0.3V to +6V
LX to GND .....-0.3V to +30V
MAIN, COR1, COR2, REF, LFB to GND .....-0.3V to (V_{IN} + 0.3V)
SWIN to IN .....-0.3V to +0.3V
Current into LX or SWIN .....300mA_{RMS}
Current Out of SW .....300mA_{RMS}
Output Short-Circuit Duration.....Continuous

Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 16.9mW/°C above +70°C) ...1.349W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{SWIN} = V_{ENSD} = V_{ENC2} = V_{ENLCD} = 4.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
IN, SWIN Voltage Range	Operating	3.1		5.5	V
IN Complete Shutdown Threshold	V_{IN} falling	2.95	3	3.05	V
IN Restart Threshold	V_{IN} rising	3.51	3.6	3.69	V
IN, SWIN Operating Current—All On	V_{LFB} = 1.3V		100	125	µA
IN Operating Current—All On Except LCD	ENLCD = GND		90	110	µA
IN Operating Current—MAIN and COR1 On	ENLCD = ENC2 = ENSD = GND, LDO loads = 0µA		50	65	µA
IN, SWIN Operating Current—Shut Down	V_{SWIN} = V_{IN} = 2.9V		2	10	µA
REF Output Voltage	I_{REF} = 0µA to 5µA	1.235	1.25	1.265	V
LDOs					
MAIN Output Voltage	I_{LOAD} = 100µA to 300mA, V_{IN} = 3.6V to 5.5V	3.2175	3.3	3.3825	V
$\overline{RS}$ Deassert Threshold for MAIN Rising		3.093	3.173	3.252	V
$\overline{RS}$ Assert Threshold MAIN Falling		3.0100	3.094	3.1755	V
MAIN Current Limit		630	900	1200	mA
MAIN Dropout Voltage (0.7Ω typ)	I_{LOAD} = 1mA		1		mV
	I_{LOAD} = 300mA		210	310	
	I_{LOAD} = 500mA		350	525	
SDIG Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	3.2175	3.3	3.3825	V
SDIG Current Limit		420	630	825	mA
SDIG Dropout Voltage (0.85Ω typ) (Note 1)	I_{LOAD} = 1mA		0.80		mV
	I_{LOAD} = 200mA		170	300	
	I_{LOAD} = 400mA		340	600	
SDIG Reverse Leakage Current	V_{SDIG} = 5V, ENSD = V_{IN} = GND		7	15	µA
COR1 Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	0.960	1	1.025	V
COR1 Current Limit		250	450	750	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{SWIN} = V_{ENSD} = V_{ENC2} = V_{ENLCD} = 4.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
COR2 Output Voltage	I_{LOAD} = 100µA to 20mA, V_{IN} = 3.6V to 5.5V	1.755	1.8	1.845	V
COR2 Current Limit		30	50	100	mA
LCD					
LX Voltage Range				28	V
LX Current Limit	L1 = 10µH	210	250	285	mA
LX On-Resistance			1.7		Ω
LX Leakage Current	V_{LX} = 28V			2	µA
Maximum LX On-Time		8	11	14	µs
Minimum LX Off-Time	V_{LFB} > 1.1V	0.8	1	1.2	µs
	V_{LFB} < 0.8V (soft-start)	3.9	5	6.0	
LFB Feedback Threshold		1.23	1.25	1.27	V
LFB Input Bias Current	V_{LFB} = 1.3V		5	100	nA
SW Off Leakage Current	SW = GND, V_{SWIN} = 5.5V, ENLCD = GND		0.01	1	µA
SW PMOS On-Resistance			1	1.75	Ω
SW PMOS Peak Current Limit			700		mA
SW PMOS Ave Current Limit			300		mA
Soft-Start Time	C_{SW} = 1µF		0.13		ms
LOGIC IN AND OUT					
EN_ Input Low Level	V_{IN} = 3.1V to 5.5V			0.4	V
EN_ Input High Level	V_{IN} = 3.1V to 5.5V	1.4			V
EN_ Input Leakage Current			0.01	1	µA
$\overline{RS}$, Output Low Level	Sinking 1mA, V_{IN} = 2.5V		0.25	0.4	V
$\overline{RS}$, Output High Leakage	V_{OUT} = 5.5V			1	µA
THERMAL PROTECTION					
Thermal-Shutdown Temperature	Rising temperature		+160		°C

5-Output Power-Management IC For Low-Cost PDAs

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{SWIN} = V_{ENSD} = V_{ENC2} = V_{ENLCD} = 4.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
GENERAL				
IN, SWIN Voltage Range	Operating	3.1	5.5	V
IN Complete Shutdown Threshold	V_{IN} falling	2.95	3.05	V
IN Restart Threshold	V_{IN} rising	3.51	3.69	V
IN, SWIN Operating Current—All On	V_{LFB} = 1.3V		125	µA
IN Operating Current—All On Except LCD	ENLCD = GND		110	µA
IN Operating Current—MAIN and COR1 On	ENLCD = ENC2 = ENSD = GND, LDO loads = 0µA		65	µA
IN, SWIN Operating Current—Shut Down	V_{SWIN} = V_{IN} = 2.9V		10	µA
LDOs				
MAIN Output Voltage	I_{LOAD} = 100µA to 300mA, V_{IN} = 3.6V to 5.5V	3.2175	3.3825	V
$\overline{RS}$ Deassert Threshold for MAIN Rising		3.093	3.252	V
$\overline{RS}$ Assert Threshold MAIN Falling		3.0100	3.1755	V
MAIN Current Limit		630	1200	mA
MAIN Dropout Voltage (0.7Ω typ) (Note 1)	I_{LOAD} = 300mA		310	mV
	I_{LOAD} = 500mA		525	
SDIG Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	3.2175	3.3825	V
SDIG Current Limit		420	825	mA
SDIG Dropout Voltage (0.75Ω typ)	I_{LOAD} = 1mA		800	mV
	I_{LOAD} = 200mA		300	
	I_{LOAD} = 400mA		600	
SDIG Reverse Leakage Current	V_{SDIG} = 5V, ENSD = V_{IN} = GND		15	µA
COR1 Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	0.96	1.025	V
COR1 Current Limit		250	750	mA
COR2 Output Voltage	I_{LOAD} = 100µA to 20mA, V_{IN} = 3.6V to 5.5V	1.755	1.845	V
COR2 Current Limit		30	100	mA
LCD				
LX Voltage Range			28	V
LX Current Limit	L1 = 10µH	200	285	mA
LX Leakage Current	V_{LX} = 28V		2	µA
Maximum LX On-Time		8	14	µs
Minimum LX Off-Time	V_{LFB} > 1.1V	0.8	1.2	µs
	V_{LFB} < 0.8V (soft-start)	3.9	6.0	
LFB Feedback Threshold		1.220	1.270	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{SWIN} = V_{ENSD} = V_{ENC2} = V_{ENLCD} = 4.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

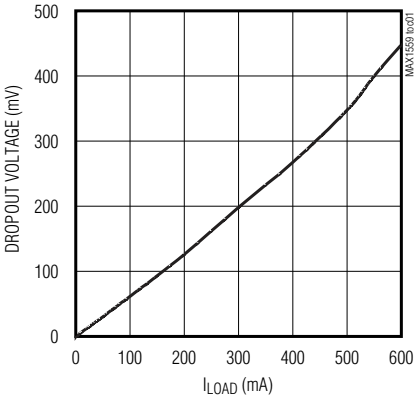
PARAMETER	CONDITIONS	MIN	MAX	UNITS
LFB Input Bias Current	V_{LFB} = 1.3V		100	nA
SW Off-Leakage Current	SW = GND, V_{SWIN} = 5.5V, ENLCD = GND		1	µA
LOGIC IN AND OUT				
EN_ Input Low Level	V_{IN} = 3.1V to 5.5V		0.4	V
EN_ Input High Level	V_{IN} = 3.1V to 5.5V	1.4		V
EN_ Input Leakage Current			1	µA
$\overline{RS}$, Output Low Level	Sinking 1mA, V_{IN} = 2.5V		0.4	V
$\overline{RS}$, Output High Leakage	V_{OUT} = 5.5V		1	µA

Note 1: Specification is guaranteed by design, not production tested.
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

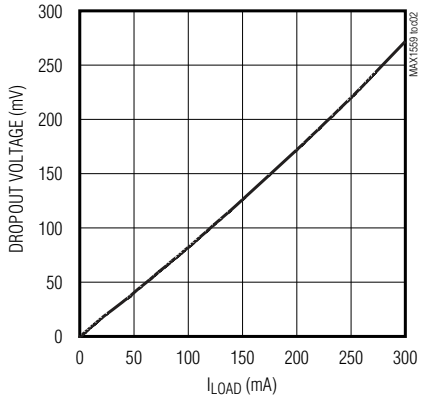
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

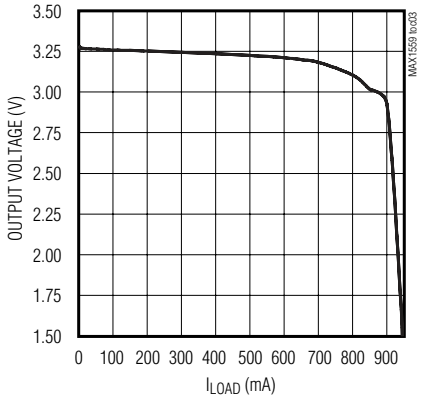
MAIN DROPOUT VOLTAGE vs. LOAD CURRENT



SDIG DROPOUT VOLTAGE vs. LOAD CURRENT



MAIN OUTPUT VOLTAGE vs. LOAD CURRENT

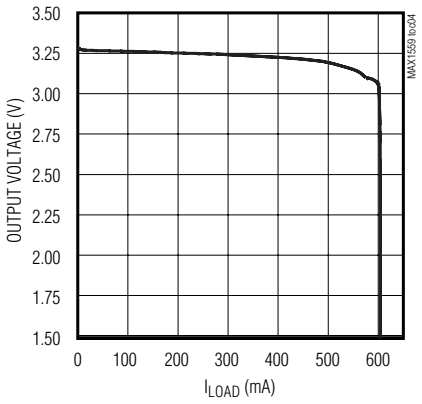


5-Output Power-Management IC For Low-Cost PDAs

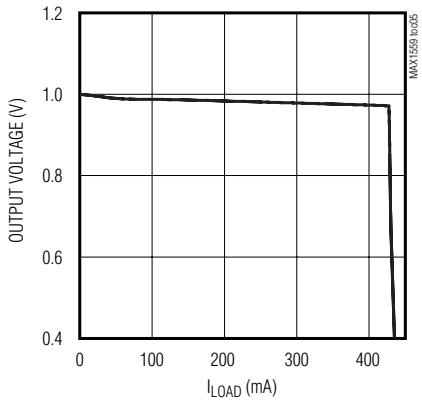
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

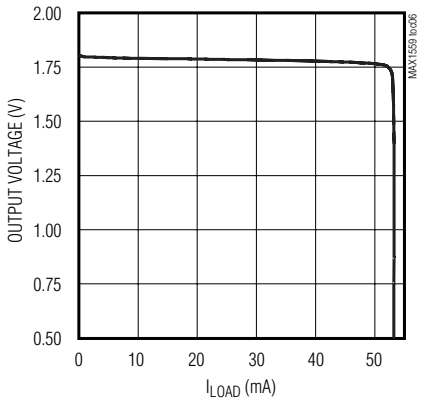
SDIG OUTPUT VOLTAGE vs. LOAD CURRENT



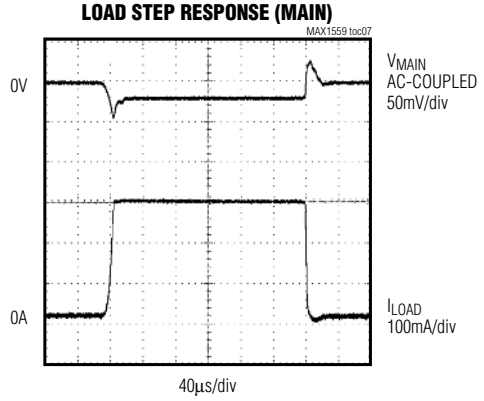
COR1 OUTPUT VOLTAGE vs. LOAD CURRENT



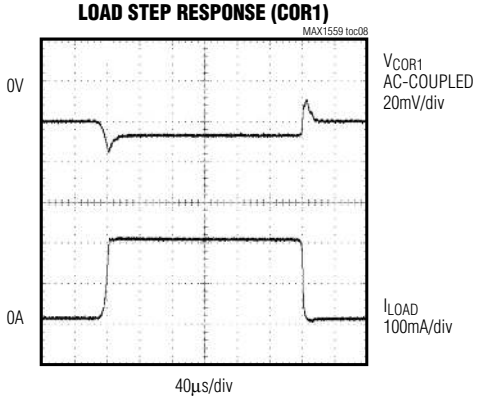
COR2 OUTPUT VOLTAGE vs. LOAD CURRENT



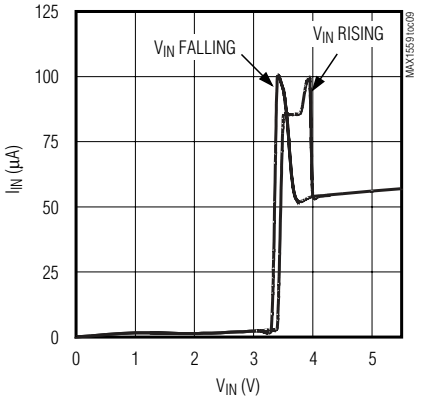
LOAD STEP RESPONSE (MAIN)



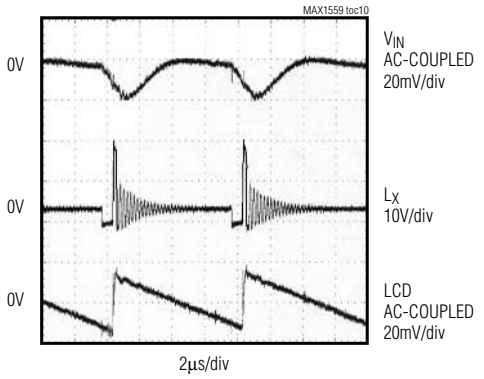
LOAD STEP RESPONSE (COR1)



INPUT CURRENT vs. INPUT VOLTAGE



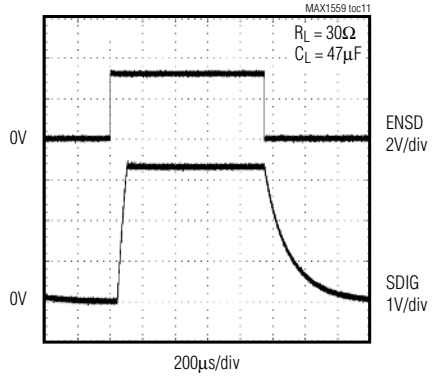
LCD SWITCH WAVEFORM



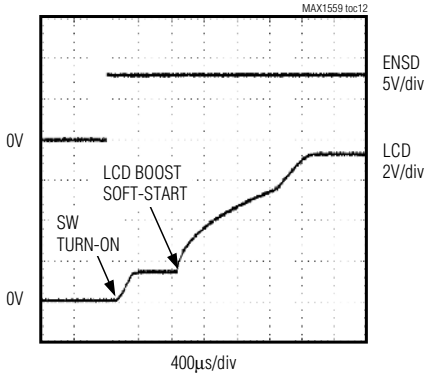
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

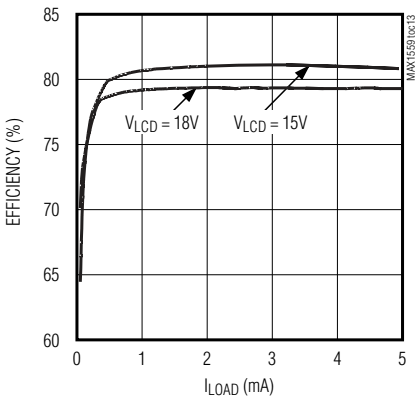
ENABLE RESPONSE TO ENSD



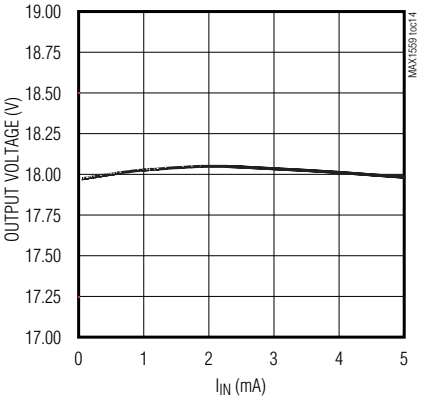
ENABLE RESPONSE TO LCD



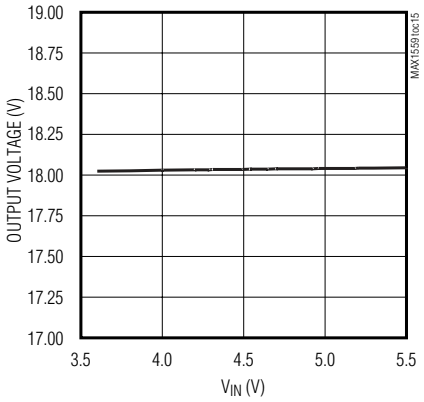
LCD EFFICIENCY vs. LOAD CURRENT



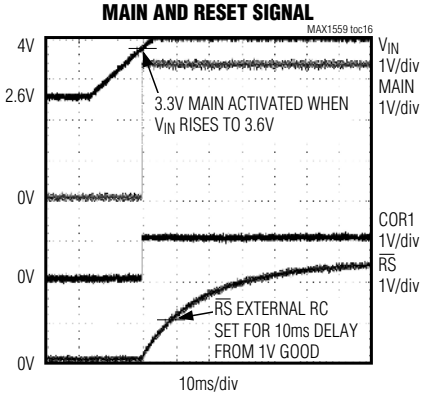
LCD OUTPUT VOLTAGE vs. LOAD CURRENT



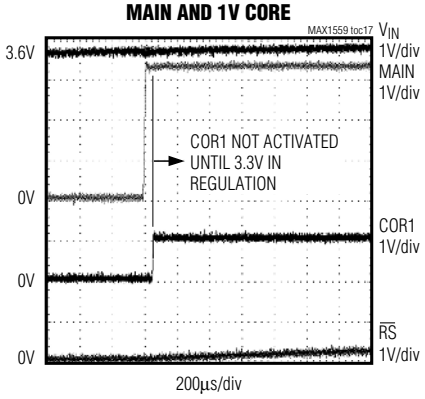
LCD OUTPUT VOLTAGE vs. INPUT VOLTAGE



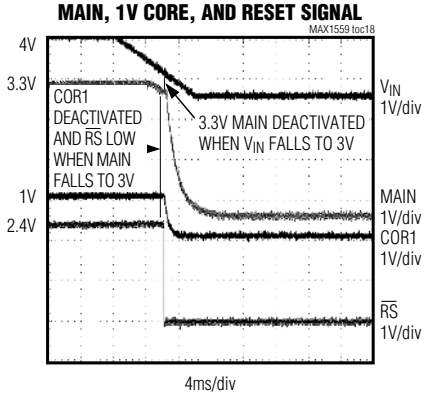
POWER-ON TIMING FOR 3.3V MAIN AND RESET SIGNAL



POWER-ON TIMING FOR 3.3V MAIN AND 1V CORE



POWER-OFF TIMING FOR 3.3V MAIN, 1V CORE, AND RESET SIGNAL



5-Output Power-Management IC For Low-Cost PDAs

Pin Description

PIN		FUNCTION
1	COR1	1V, 250mA LDO Output for CPU Core. COR1 turns off when V_{IN} < 3V or MAIN < 3.1V.
2	IN	Input Voltage to the Device. Bypass to GND with a 1µF capacitor.
3	SDIG	3.3V, 400mA LDO Output for Secure Digital Card Slot. SDIG has reverse current protection so SDIG can be biased when no power is present at IN. SDIG output turns off when V_{IN} < 3V or when ENSD goes low.
4	ENSD	SDIG Enable Input. Drive ENSD low to turn off SDIG and high to turn on. SDIG cannot be activated when V_{IN} < 3V.
5	REF	1.25V Reference. Bypass with 0.1µF to GND.
6	$\overline{RS}$	Reset Output. $\overline{RS}$ is an active-low, open-drain output that goes low when V_{MAIN} falls below 3.1V. $\overline{RS}$ deasserts when V_{MAIN} goes above 3.2V. Connect a 1MΩ pullup resistor from $\overline{RS}$ to MAIN.
7	N.C.	Not Connected
8	GND	Ground
9	LX	LCD Boost Switch. Connect to a boost inductor and Schottky diode. See Figure 1.
10	SW	LCD True Shutdown Switch Output. SW is the power source for the boost inductor. SW turns on when ENLCD is high. For best efficiency, bypass SW with 4.7µF to GND.
11	SWIN	LCD True Shutdown Switch Input. The SWIN-to-SW switch turns off when ENLCD goes low or when V_{IN} < 3V. Connect SWIN to IN.
12	LFB	LCD Feedback Input. Connect LFB to a resistor-divider network between the LCD output and GND. The feedback threshold is 1.25V.
13	ENLCD	Enable Input for LCD (Boost Regulator). Drive ENLCD high to activate the LCD boost. Drive ENLCD low to shut down the LCD output. The LCD cannot be activated when V_{IN} < 3V.
14	ENC2	Enable Input for Secondary Core LDO (COR2). Drive ENC2 high to turn on COR2 and low to turn off. COR2 cannot be activated when V_{IN} < 3V.
15	COR2	1.8V, 30mA LDO Output for Secondary Core. COR2 turns off when V_{IN} < 3V or when ENC2 goes low.
16	MAIN	3.3V, 500mA LDO Output for Main Supply. MAIN output turns off when V_{IN} < 3V.

Detailed Description

Linear Regulators

The MAX1559 contains all power blocks and voltage monitors for a small PDA. Power for logic and other subsystems are provided by four LDOs:

- MAIN—Provides 3.3V at a guaranteed 500mA with a typical current limit of 900mA.
- SDIG—Provides 3.3V at a guaranteed 400mA for secure digital cards with a typical current limit of 630mA.
- COR1—1V for CPU core guarantees 250mA and a typical current limit of 450mA.
- COR2—1.8V for CODEC core guarantees 30mA and a typical current limit of 50mA.

Note that it may not be possible to draw the rated current of MAIN and SDIG at all operating input voltages due to the dropout limitations of those regulators. The typical dropout resistance of the MAIN regulator is 0.7Ω (350mV drop at 500mA), and the typical dropout resistance of the SDIG regulator is 0.85Ω (340mV drop at 400mA).

MAIN and COR1 regulators are always on as long as the IC is not in low-voltage shutdown (V_{IN} < 3V). COR2 and SDIG can be turned on and off independently by logic signals at ENC2 and ENSD, respectively, but cannot be activated if V_{IN} < 3V.

When SDIG is turned off, reverse current is blocked so the SDIG output can be biased with an external source when no power is present at IN. Leakage current is typically 3µA with 3.3V at SDIG.

LCD DC-DC Boost

In addition to the LDOs, the MAX1559 also includes a low-current, high-voltage DC-DC boost converter for LCD bias. This circuit can output at up to 28V and can be adjusted with either an analog or PWM control signal using external components.

SW provides an input-power disconnect for the LCD when ENLCD is low (off). The input-power disconnect function is ideal for applications that require the output voltage to fall to 0V in shutdown (True Shutdown). If True Shutdown is not required, the SW switch can be bypassed by connecting the boost inductor directly to IN and removing the bypass cap on SW (C9 in Figure 1).

System Sleep

All regulated outputs turn off when V_{IN} falls below 3V. The MAX1559 resumes normal operation when V_{IN} rises above 3.6V.

Reset Output

Reset ($\overline{RS}$) asserts when V_{MAIN} falls below 3.094V. $\overline{RS}$ is an open-drain, active-low output. Connect a 1MΩ resistor from $\overline{RS}$ to MAIN. To implement a reset deassertion delay, add a capacitor from $\overline{RS}$ to GND. An approximate 10ms delay can be generated with 1MΩ and 22nF. This results in a 22ms time constant, but assumes the input threshold of the CPU reset input is approximately 1V and is reached approximately 10ms after $\overline{RS}$ goes high impedance. Timing for $\overline{RS}$, 3.3V MAIN, and 1V COR1 is shown in Figure 3.

Applications Information

LDO Output Capacitors (MAIN, SDIG, COR1, and COR2)

Capacitors are required at each output of the MAX1559 for stable operation over the full load and temperature range. See Figure 1 for recommended capacitor values for each output. To reduce noise and improve load transients, large output capacitors at up to 10µF can be used. Surface-mount ceramic capacitors have very low ESR and are commonly available in values up to 10µF. X7R and X5R dielectrics are recommended. Note that some ceramic dielectrics, such as Z5U and Y5V, exhibit large capacitance and ESR variation with temperature and require larger than the recommended values to maintain stability over temperature.

LCD Boost Output

Selecting an Inductor

The LCD boost is designed to operate with a wide range of inductor values (4.7µH to 22µH). Smaller inductance values typically offer smaller size for a given series resistance or saturation current. Smaller values make LX switch more frequently for a given load and can reduce efficiency at low load currents. Larger values reduce switching losses due to less frequent switching for a given load, but higher resistance can then reduce efficiency. A 10µH inductor provides a good balance and works well for most applications. The inductor's saturation current rating should be greater than the peak switching current (250mA); however, it is generally acceptable to bias some inductors into saturation by as much as 20%, although this slightly reduces efficiency.

Selecting a Diode

Schottky diodes rated at 250mA or more, such as the Motorola MBRS0530 or Nihon EP05Q03L are recommended. The diode reverse-breakdown voltage rating must be greater than the LCD output voltage.

Selecting Capacitors

For most applications, use a small 1µF LCD output capacitor. This typically provides a peak-to-peak output ripple of 30mV. In addition, bypass IN with 1µF and SW with 4.7µF ceramic capacitors.

An LCD feed-forward capacitor, connected from the output to FB, improves stability over a wide range of battery voltages. A 10pF capacitor is sufficient for most applications; however, this value is also affected by PC board layout.

Setting the LCD Voltage

Adjust the output voltage by connecting a voltage-divider from the output (V_{OUT}) to FB (Figure 1). Select R2 between 10kΩ and 200kΩ. Calculate R1 with the following equation:

$$R_1 = R_2 [(V_{OUT} / V_{FB}) - 1]$$

where V_{FB} = 1.25V and V_{OUT} can range from V_{IN} to 28V. The input bias current of FB is typically only 5nA, which allows large-value resistors to be used. For less

5-Output Power-Management IC For Low-Cost PDAs

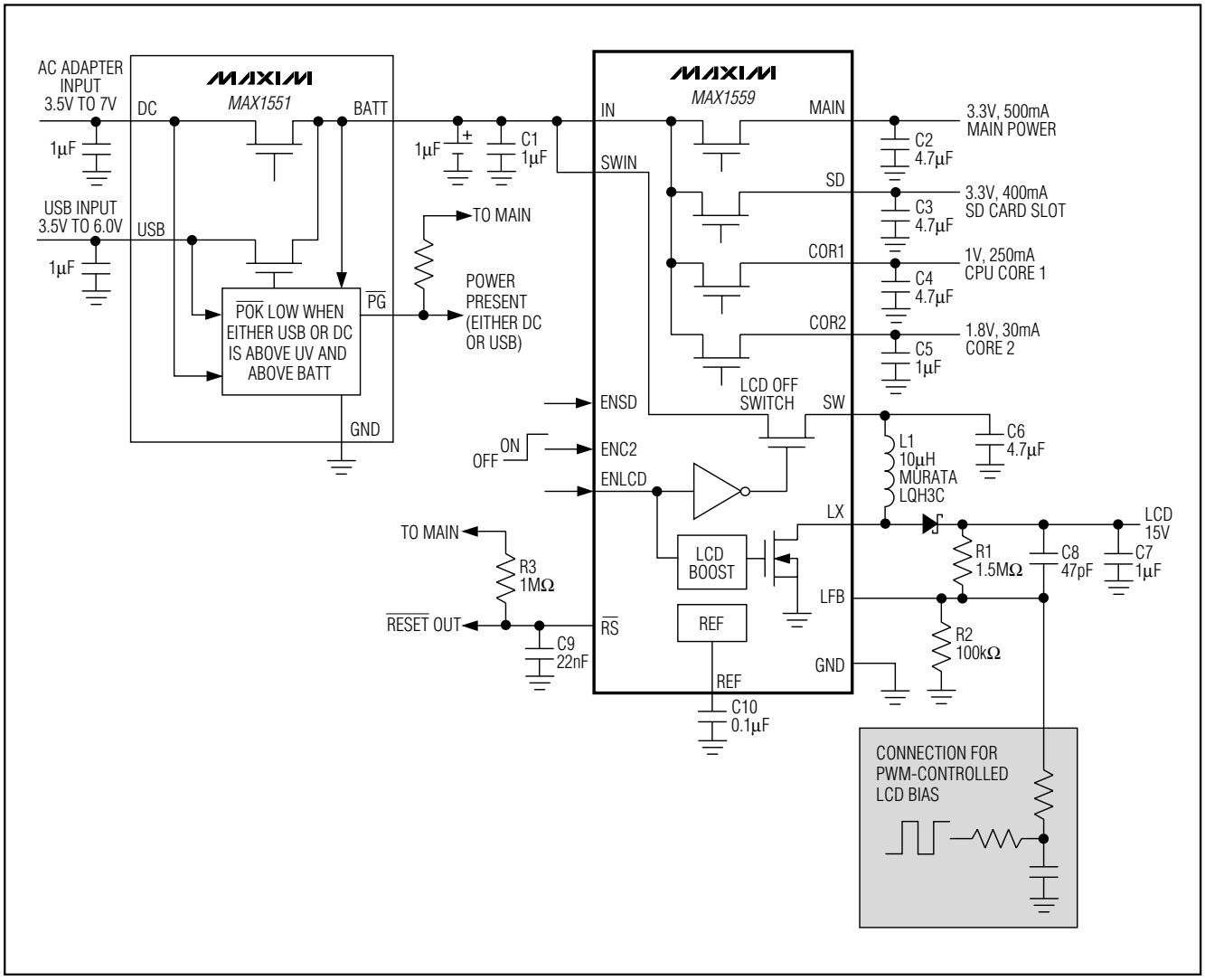


Figure 1. Typical Operating Circuit with Charger and External PWM LCD Control

than 1% error, the current through R2 should be greater than 100 times the feedback input bias current (I_{FB}).

LCD Adjustment

The LCD boost output can be digitally adjusted by either a DAC or PWM signal.

DAC Adjustment

Adding a DAC and a resistor, R_D, to the divider-circuit (Figure 4) provides DAC adjustment of V_{OUT}. Ensure that $V_{OUT(MAX)}$ does not exceed the LCD panel rating. The output voltage (V_{OUT}) as a function of the DAC voltage (V_{DOUT}) can be calculated using the following formula:

$$V_{OUT} = V_{REF}\left(1+\left(\frac{R_1}{R_2}\right)\right)+\frac{(V_{REF}-V_{DOUT})R_1}{R_D}$$

Using a PWM Signal

Many microprocessors have the ability to create PWM outputs. These are digital outputs, based on either 16-bit or 8-bit counters, with a programmable duty cycle. In many applications, they are suitable for adjusting the output of the MAX1559 as seen in Figure 1.

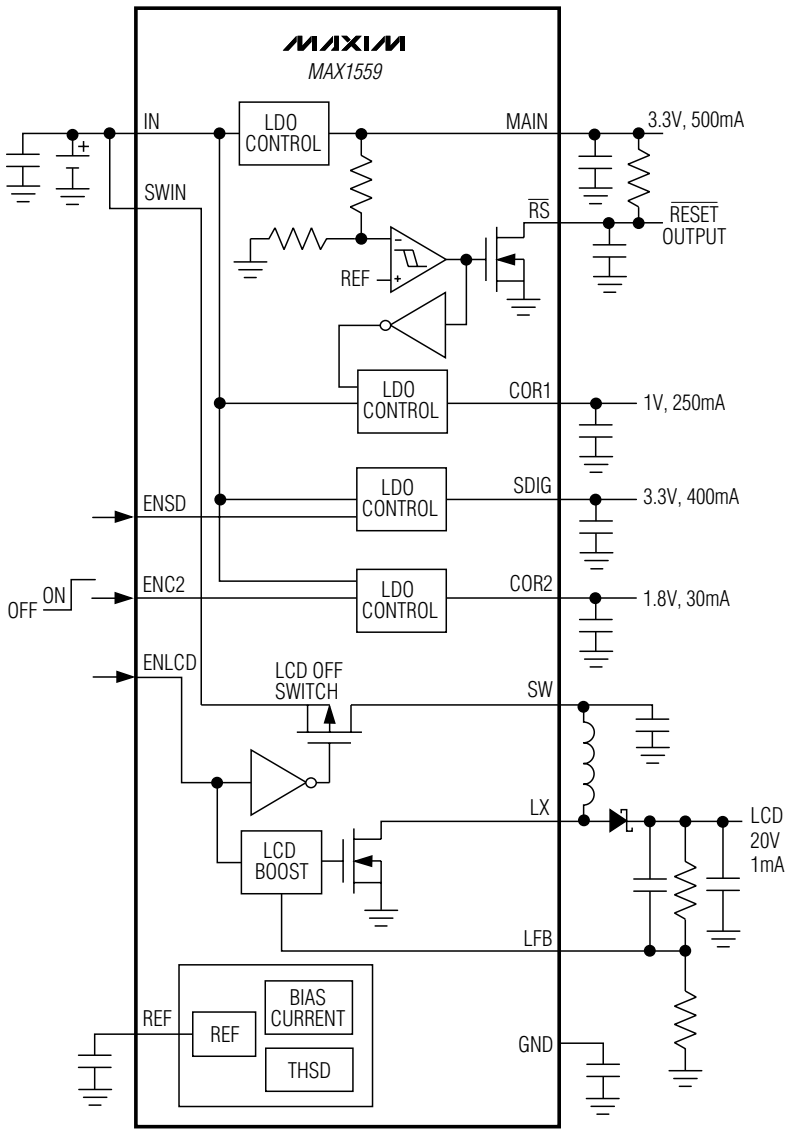


Figure 2. Functional Diagram

The circuit consists of the PWM source, capacitor C10, and resistors R_D and R_W. To analyze the transfer function of the PWM circuit, it is easiest to first simplify it to its Thevenin equivalent. The Thevenin voltage can be calculated using the following formula:

$$V_{THEV} = (D \times V_{OH}) + (1 - D) \times V_{OL}$$

where D is the duty cycle of the PWM signal, V_{OH} is the PWM output high level (often 3.3V), and V_{OL} is the PWM output low level (usually 0V). For CMOS logic, this equation simplifies to:

$$V_{THEV} = D \times V_{DD}$$

5-Output Power-Management IC For Low-Cost PDAs

where V_{DD} is the I/O voltage of the PWM output. The Thevenin impedance is the sum of resistors R_W and R_D:

$$R_{THEV} = R_D + R_W$$

The output voltage (V_{OUT}) as a function of the PWM average voltage (V_{THEV}) is:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) + \frac{(V_{REF} - V_{THEV}) \times R_1}{R_{THEV}}$$

When using the PWM adjustment method, R_D isolates the capacitor from the feedback loop of the MAX1559. The cutoff frequency of the lowpass filter is defined as:

$$f_C = \frac{1}{2 \times \pi \times R_{THEV}}$$

The cutoff frequency should be at least 2 decades below the PWM frequency to minimize the induced AC ripple at the output.

An important consideration is the turn-on transient created by the initial charge on the filter capacitor C10. This capacitor forms a time constant with R_{THEV}, which causes the output to initialize at a higher than intended voltage. This overshoot can be minimized by scaling R_D as high as possible compared to R1 and R2. Alternately, the µP can briefly keep the LCD disabled until the PWM voltage has had time to stabilize.

PC Board Layout and Grounding

Careful PC board layout is important for minimizing ground bounce and noise. Keep the MAX1559's ground pin and the ground leads of the input and output capacitors less than 0.2in (5mm) apart. In addition, keep all connections to FB and LX as short as possible. In particular, external feedback resistors should be as close to FB as possible. To minimize output voltage ripple and to maximize output power and efficiency, use a ground plane and solder GND directly to the ground plane. Refer to the MAX1559 evaluation kit for a layout example.

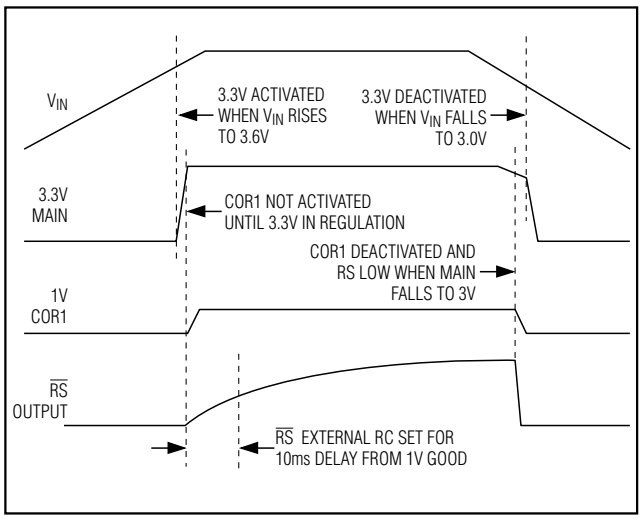


Figure 3. $\overline{RS}$ and Power-On, Power-Off Timing for 3.3V and 1V Core

Thermal Considerations

In most applications, the circuit is located on a multilayer board and full use of the four or more layers is recommended. For heat dissipation, connect the exposed backside pad of the QFN package to a large analog ground plane, preferably on a surface of the board that receives good airflow. Typical applications use multiple ground planes to minimize thermal resistance. Avoid large AC currents through the analog ground plane.

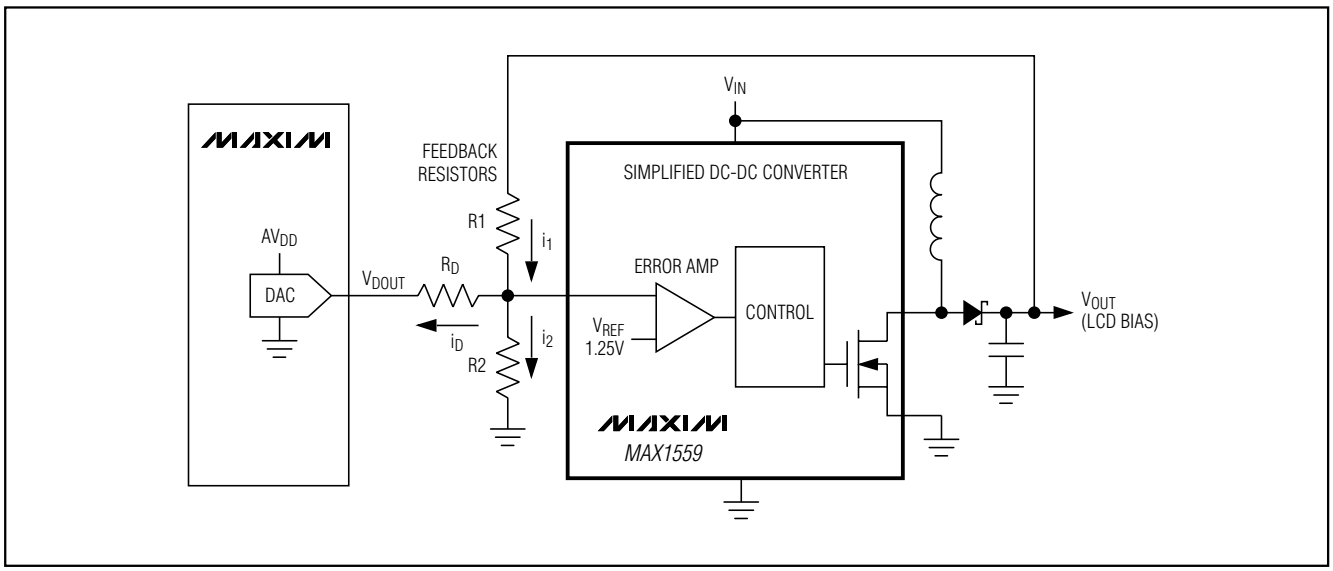
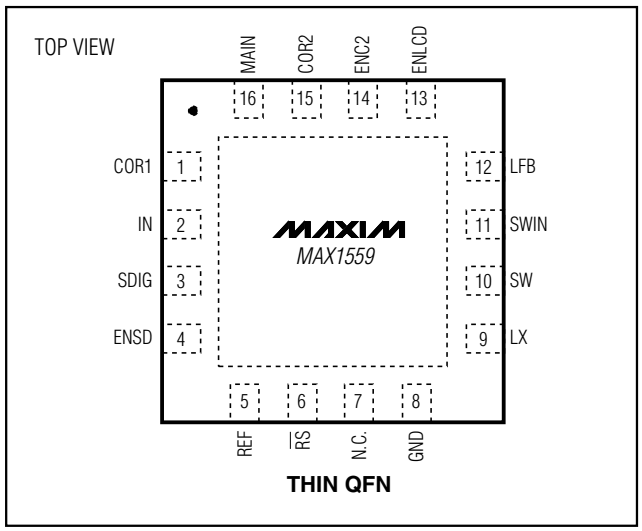


Figure 4. Adjusting the Output Voltage with a DAC

Pin Configuration



Chip Information

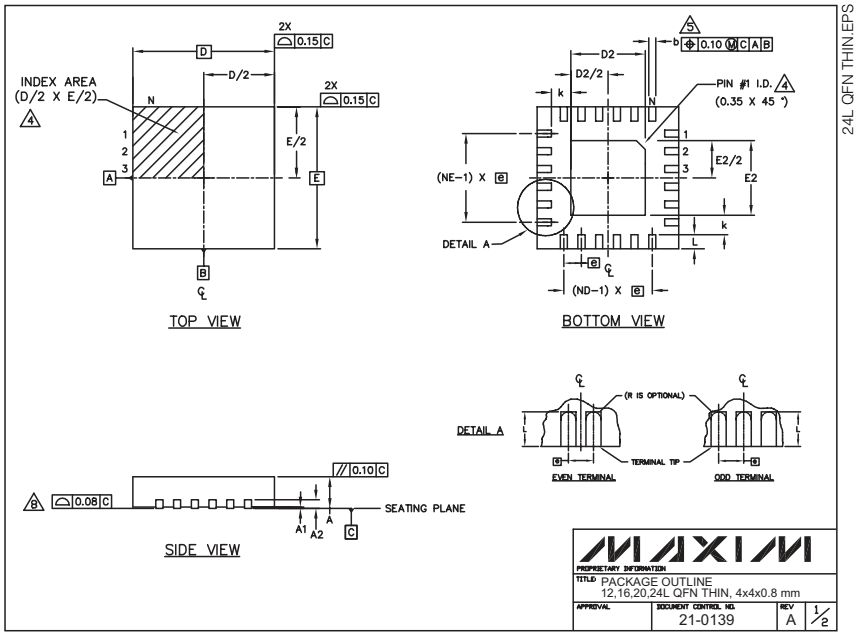
PROCESS: BiCMOS

TRANSISTOR COUNT: 1872

5-Output Power-Management IC For Low-Cost PDAs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV A
2/2

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