# 0.7V to $V_{CC}$-1V, 4A 1ch Ultra Low Dropout Linear Regulator

## BD3509MUV

### General Description

The BD3509MUV ultra low-dropout linear chipset regulator operates from a very low input supply. The product offers ideal performance at low input voltage and low output voltage applications. A built-in N-channel MOSFET is incorporated to minimize the input-to-output differential voltage across the ON-Resistance ($R_{ON}$ =50mΩ(Max)) level. This lower dropout voltage ensures high output current ($I_{OUTMAX}$=4.0A) with reduced conversion loss, and thereby eliminates the need for a switching regulator, its power transistor, choke coil, and rectifier diode. BD3509MUV is designed with significant package profile downsizing and reducing cost. External resistors allow a wide range of output voltage configurations between 0.65V and 2.7V. NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to any required power supply sequence.

### Features

- High-precision internal reference voltage circuit (0.65V±1%)
- Built-in VCC under voltage lock out circuit ($V_{CC}$=3.80V)
- NRCS (soft start) function for reduction of in-rush current
- Internal N-channel MOSFET driver offers low ON-Resistance
- Built-in current limiter circuit (4.0A min)
- Built-in thermal shutdown (TSD) circuit
- Tracking function
- Built-in Power Good function

### Key Specifications

| | |
|---|---|
| ■ IN Input Voltage Range: | 0.7V to $V_{CC}$-1V |
| ■ VCC Input Voltage Range: | 4.3V to 5.5V |
| ■ VDD Input Voltage Range: | 2.7V to 5.5V |
| ■ Output Voltage Range: | 0.65V to 2.7V |
| ■ Output Current: | 4.0A (Max) |
| ■ ON-Resistance: | 28mΩ(Typ) |
| ■ Standby Current: | 0µA (Typ) |
| ■ Operating Temperature Range: | -10°C to +100°C |

### Package

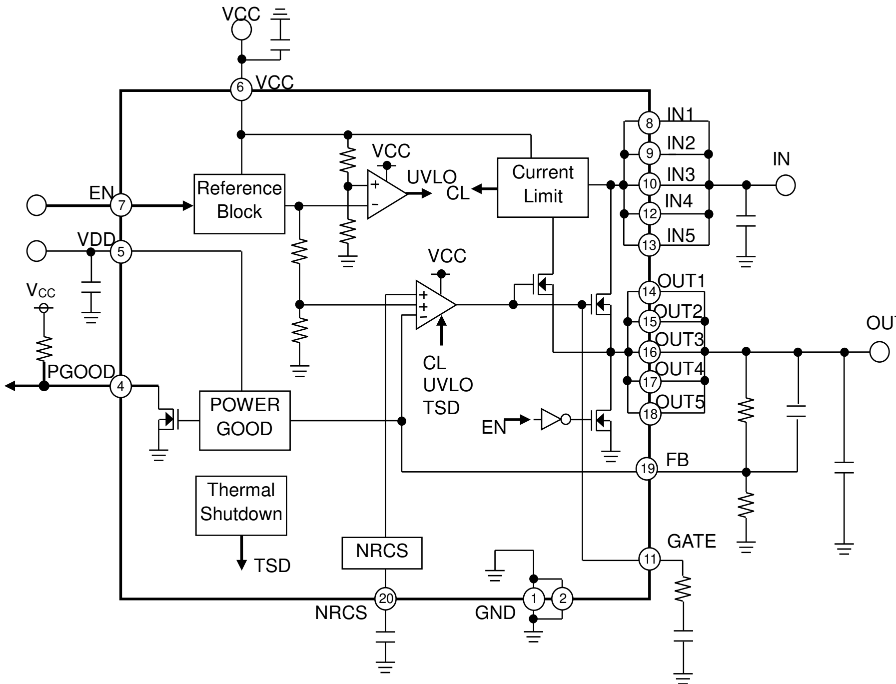
W(Typ) x D(Typ) x H(Max)

**VQFN020V4040**
4.00mm x 4.00mm x 1.00mm

### Applications

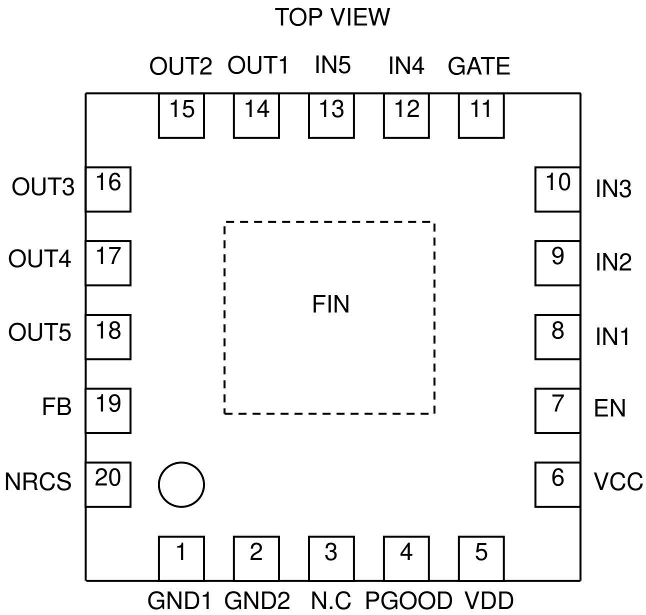
Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

### Typical Application Circuit and Block Diagram




○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

## Pin Configuration




## Pin Descriptions

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | GND1 | Ground pin 1 |
| 2 | GND2 | Ground pin 2 |
| 3 | N.C. | No connection (empty) pin (Note) |
| 4 | PGOOD | Power good pin |
| 5 | VDD | Power supply pin for Power good circuit |
| 6 | VCC | Power supply pin |
| 7 | EN | Enable input pin |
| 8 | IN1 | Input pin 1 |
| 9 | IN2 | Input pin 2 |
| 10 | IN3 | Input pin 3 |
| 11 | GATE | Gate pin |
| 12 | IN4 | Input pin 4 |
| 13 | IN5 | Input pin 5 |
| 14 | OUT1 | Output voltage pin 1 |
| 15 | OUT2 | Output voltage pin 2 |
| 16 | OUT3 | Output voltage pin 3 |
| 17 | OUT4 | Output voltage pin 4 |
| 18 | OUT5 | Output voltage pin 5 |
| 19 | FB | Reference voltage feedback pin |
| 20 | NRCS | In-rush current protection (NRCS) capacitor connection pin |
| reverse | FIN | Connected to heatsink and GND |

(Note) Please short N.C to the GND.

## Description of Blocks

1. AMP
   This is an error amplifier that functions by comparing the reference voltage (0.65V) with FB voltage to drive the output N-channel FET. The frequency characteristics are optimized such that polymer output capacitors can be used ad rapid transit response can be achieved. The AMP output voltage ranges from GND to VCC. When EN is OFF, or when UVLO is active, the output goes LOW and the output N-channel FET switches OFF.

2. EN
   EN is a logic input pin which controls the regulator ON or OFF. When the regulator is OFF, the circuit current is maintained at 0µA, minimizing current consumption during standby. When the FET is switched ON, the discharge of NRCS and OUT is enabled, draining the excess charge and preventing the load IC from malfunctioning. Since no electrical connection is required (such as between the VCC pin and the ESD prevention diode), module operation is independent of the input sequence.

3. UVLO
   To prevent malfunction that can occur when there is a brief decrease in VCC supply voltage, the UVLO circuit switches the output OFF. Like EN, UVLO discharges the NRCS and OUT. Once the UVLO threshold voltage (typ 3.80V) is exceeded, UVLO turns the output ON.

4. Current Limit
   When the output is ON and the output current exceeds the set current limit threshold (0.6A or more), the output voltage is attenuated to protect the IC on the load side. When current decreases, the output voltage is restored to the allowable value.

5. NRCS
   The soft-start function can be accomplished by connecting an external capacitor across the NRCS pin and the target ground. Output ramp-up can be set to any period up to the time the NRCS pin reaches $V_{FB}$ (0.65V). During startup, the NRCS pin serves as a 20µA (typ) constant current source and charges the external capacitor.

6. TSD (Thermal Shut Down)
   The Thermal Shutdown (TSD) circuit automatically switches output OFF when the chip temperature becomes too high, protecting the IC against thermal runaway and heat damage. Since the TSD circuit shuts down the IC during extreme heat conditions, in order to avoid potential problems with the TSD, during thermal design, it is crucial that Tj(max) parameter is not exceeded.

## Description of Blocks - continued

7. IN
   The IN line acts as the major current supply line, and is connected to the output N-Channel FET drain. Since there is no electrical connection with the VCC terminal, as in the case when an ESD diode is connected, so its operation does not depend on the input sequence. However, because of the body diode of the output N-Channel FET, there is electrical connection (diode connection) between IN and OUT. Consequently, when the output is turned ON and OFF by IN, reverse current flows, in which case care must be taken.

8. PGOOD
   This is the monitor pin for output voltage (OUT). A pull-up resistor (100kΩ) is connected to this pin. PGOOD pin indicates if OUT voltage is High or Low (threshold voltage is 0.585V typ FB Voltage).

## Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Input Voltage 1 | $V_{CC}$ | 6.0 (Note 1) | V |
| Input Voltage 2 | $V_{IN}$ | 6.0 (Note 1) | V |
| Input Voltage 3 | $V_{DD}$ | 6.0 (Note 1) | V |
| Enable Input Voltage | $V_{EN}$ | 6.0 | V |
| Power Good Input Voltage | $V_{PGOOD}$ | 6.0 | V |
| Power Dissipation 1 | Pd1 | 0.34 (Note 2) | W |
| Power Dissipation 2 | Pd2 | 0.70 (Note 3) | W |
| Power Dissipation 3 | Pd3 | 2.21 (Note 4) | W |
| Power Dissipation 4 | Pd4 | 3.56 (Note 5) | W |
| Operating Temperature Range | Topr | -10 to +100 | °C |
| Storage Temperature Range | Tstg | -55 to +125 | °C |
| Maximum Junction Temperature | Tjmax | +150 | °C |

(Note 1) Should not exceed Pd.
(Note 2) Derating in done 2.7mV/°C for operating above Ta ≥ 25°C no heat sink
(Note 3) Derating in done 5.6mV/°C for operating above Ta ≥ 25°C
PCB size:74.2mm x 74.2mm x 1.6mm when mounted on a 1-layer glass epoxy board(copper foil area : 10.29mm$^2$)
(Note 4) Derating in done 17.7mV/°C for operating above Ta ≥ 25°C
PCB size:74.2mm x 74.2mm x 1.6mm when mounted on a 4-layer glass epoxy board(copper foil area : front and reverse 10.29mm$^2$ , 2nd and 3rd 5505mm$^2$)
(Note 5) Derating in done 28.5mV/°C for operating above Ta ≥ 25°C
PCB size:74.2mm x 74.2mm x 1.6mm when mounted on a 4-layer glass epoxy board(copper foil area : each 5505mm$^2$)

**Caution:** An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

## Recommended Operating Conditions (Ta=25°C)

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Input Voltage 1 | $V_{CC}$ | 4.3 | 5.5 | V |
| Input Voltage 2 | $V_{IN}$ | 0.7 | $V_{CC}$-1 (Note 6) | V |
| Input Voltage 3 | $V_{DD}$ | 2.7 | 5.5 | V |
| Output Voltage setting Range | $V_{OUT}$ | $V_{FB}$ | 2.7 | V |
| Enable Input Voltage | $V_{EN}$ | -0.3 | +5.5 | V |
| NRCS capacity | $C_{NRCS}$ | 0.001 | 1 | μF |

(Note 6) VCC and IN do not have to be implemented in the order listed.

### Electrical Characteristics

(Unless otherwise specified, Ta=25°C $V_{CC}$=5V $V_{EN}$=3V $V_{IN}$=1.5V $V_{DD}$=3.3V $R_1$=3.9kΩ $R_2$=3.6kΩ)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Circuit Current | $I_{CC}$ | - | 1.2 | 2.0 | mA | |
| VCC Shutdown Mode Current | $I_{ST}$ | - | 0 | 10 | µA | $V_{EN}$=0V |
| Maximum Output Current | $I_{OUT}$ | 4.0 | - | - | A | |
| Output Voltage Temperature Coefficient | Tcvo | - | 0.01 | - | %/°C | |
| Feedback Voltage 1 | $V_{FB1}$ | 0.643 | 0.650 | 0.657 | V | |
| Feedback Voltage 2 | $V_{FB2}$ | 0.637 | 0.650 | 0.663 | V | $I_{OUT}$=0A to 4A<br>Tj=-10°C to 100°C (Note 7) |
| Line Regulation 1 | Reg.l1 | - | 0.1 | 0.5 | %/V | $V_{CC}$=4.3V to 5.5V |
| Line Regulation 2 | Reg.l2 | - | 0.1 | 0.5 | %/V | $V_{IN}$=1.2V to 3.3V |
| Load Regulation | Reg.L | - | 0.5 | 10 | mV | $I_{OUT}$=0A to 4A |
| Minimum Input-Output Voltage Differential | dVo | - | 28 | 50 | mV | $I_{OUT}$=1A,$V_{IN}$=1.25V<br>Tj=-10°C to 100°C (Note 7) |
| Standby Discharge Current | $I_{DEN}$ | 1 | - | - | mA | $V_{EN}$=0V, $V_{OUT}$=1V |
| [ENABLE] | | | | | | |
| Enable Pin Input Voltage High | $V_{ENHI}$ | 2 | - | - | V | |
| Enable Pin Input Voltage Low | $V_{ENLOW}$ | -0.2 | - | +0.8 | V | |
| Enable Input Bias Current | $I_{EN}$ | - | 7 | 10 | µA | $V_{EN}$=3V |
| [FEEDBACK] | | | | | | |
| Feedback Pin Bias Current | $I_{FB}$ | -100 | 0 | +100 | nA | |
| [NRCS] | | | | | | |
| NRCS Charge Current | $I_{NRCS}$ | 14 | 20 | 26 | µA | $V_{NRCS}$=0.5V |
| NRCS Standby Voltage | $V_{STB}$ | - | 0 | 50 | mV | $V_{EN}$=0V |
| [UVLO] | | | | | | |
| VCC Under Voltage Lock Out Threshold Voltage | $V_{CCUVLO}$ | 3.5 | 3.8 | 4.1 | V | VCC: Sweep-up |
| VCC Under Voltage Lock Out Hysteresis Voltage | $V_{CCHYS}$ | 100 | 160 | 220 | mV | VCC: Sweep-down |
| [AMP] | | | | | | |
| Gate Source Current | $I_{GSO}$ | 6 | 10 | 14 | mA | $V_{FB}$=0, $V_{GATE}$=2.5V |
| Gate Sink Current | $I_{GSI}$ | 11 | 18 | 25 | mA | $V_{FB}$=$V_{CC}$, $V_{GATE}$=2.5V |
| [PGOOD Block] | | | | | | |
| Threshold Voltage | $V_{THPG}$ | 0.565 | 0.585 | 0.605 | V | FB voltage |
| Ron | $R_{PG}$ | - | 0.1 | 0.3 | kΩ | |

(Note 7) Not 100% tested

**Typical Waveforms**

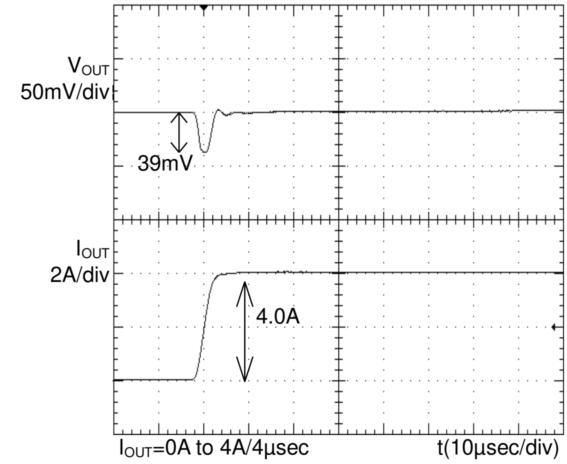



Figure 1. Transient Response
(0A to 4A)
$C_{OUT}$=22µF,$C_{FB}$=0.01µF

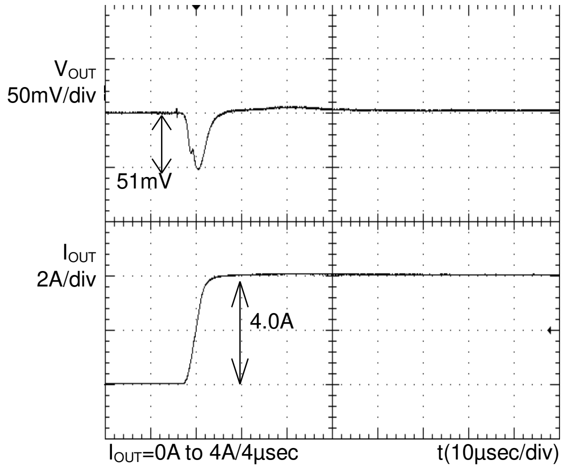



Figure 2. Transient Response
(0A to 4A)
$C_{OUT}$=100µF

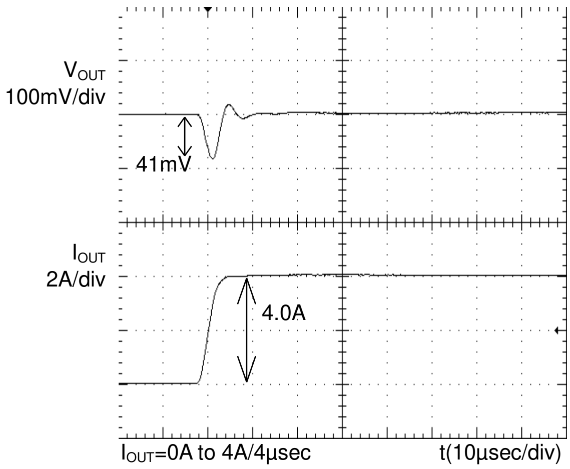



Figure 3. Transient Response
(0A to 4A)
$C_{OUT}$=47µF,$C_{FB}$=0.01µF

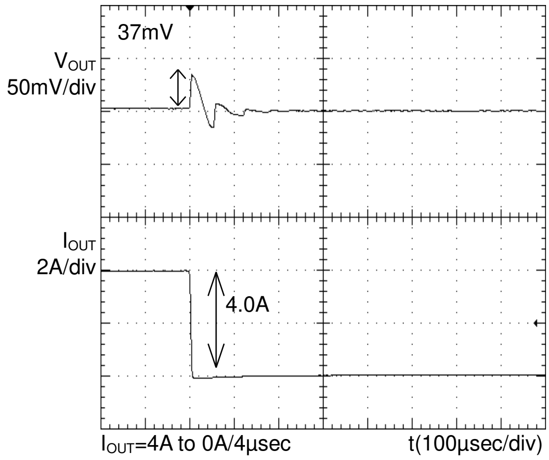



Figure 4. Transient Response
(4A to 0A)
$C_{OUT}$=22µF, $C_{FB}$=0.01µF

### Typical Waveforms – continued

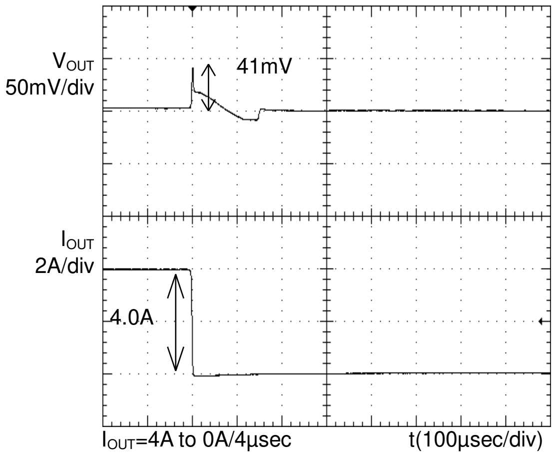



Figure 5. Transient Response
(4A to 0A)
$C_{OUT}$=100µF

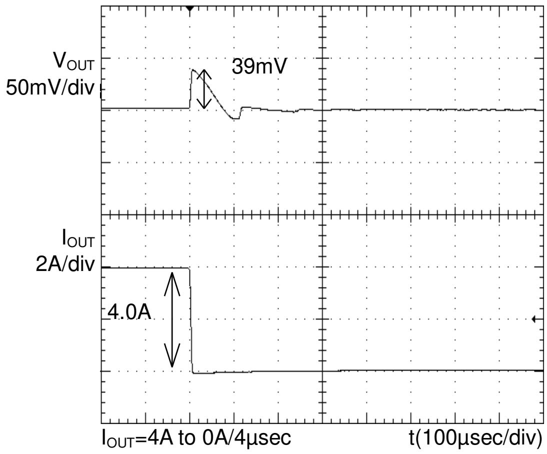



Figure 6. Transient Response
(4A to 0A)
$C_{OUT}$=47µF, $C_{FB}$=0.01µF

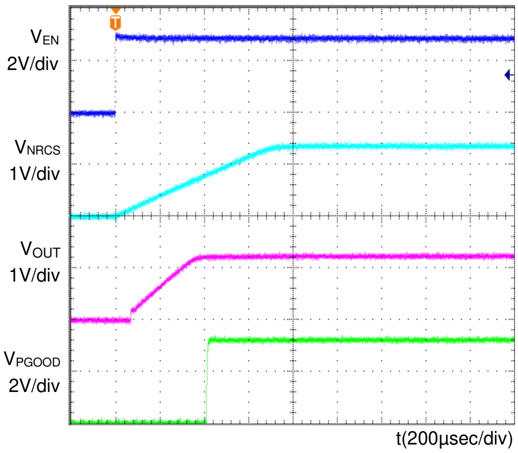



Figure 7. Waveform at Output Start

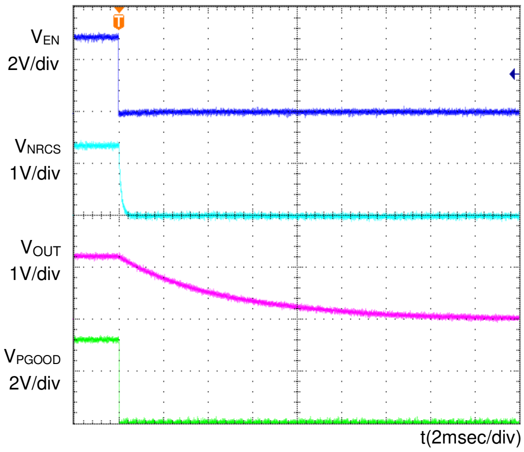
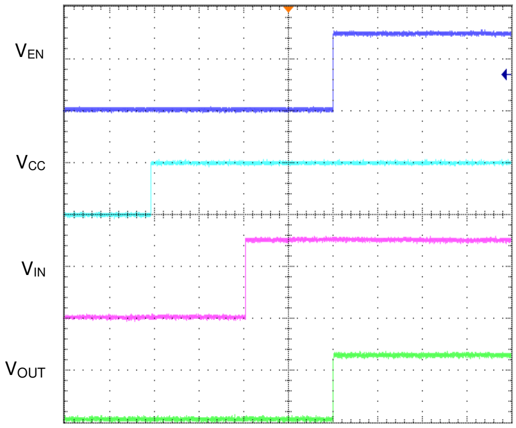


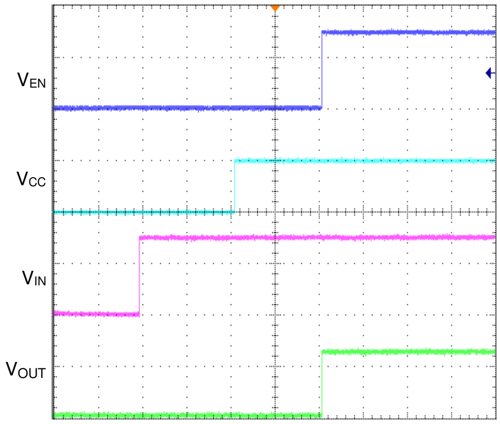

Figure 8. Waveform at Output OFF

## Typical Waveforms – continued



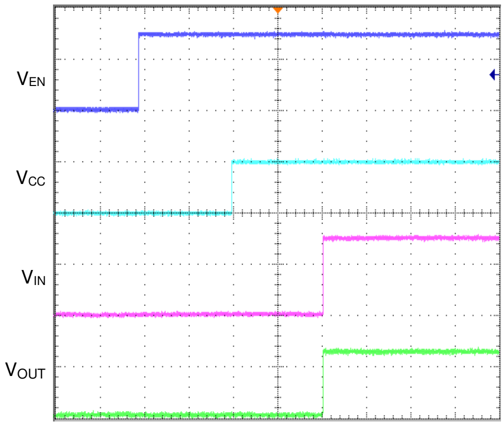

$V_{CC}$ to $V_{IN}$ to $V_{EN}$

Figure 9. Input Sequence



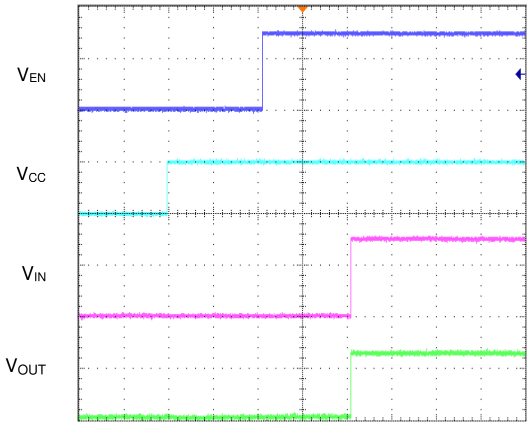

$V_{IN}$ to $V_{CC}$ to $V_{EN}$

Figure 10. Input Sequence




$V_{EN}$ to $V_{CC}$ to $V_{IN}$

Figure 11. Input Sequence




$V_{CC}$ to $V_{EN}$ to $V_{IN}$

Figure 12. Input Sequence

**Typical Waveforms – continued**

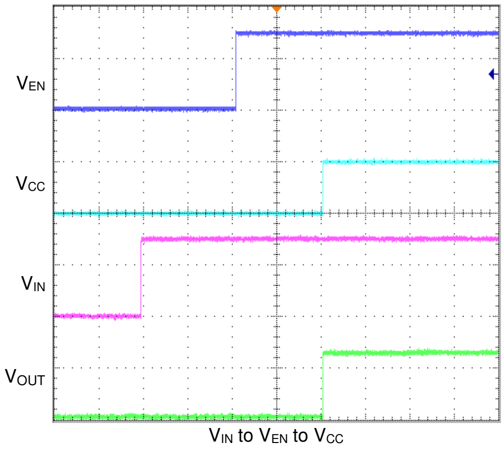



Figure 13. Input Sequence

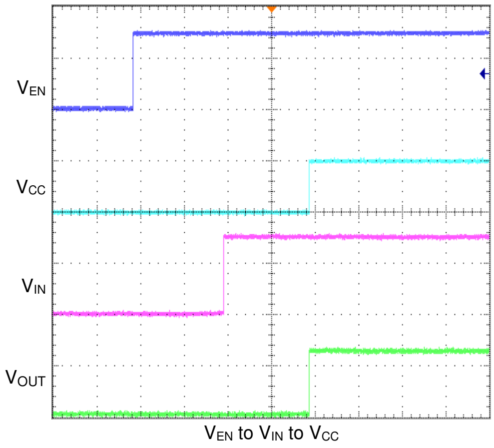



Figure 14. Input Sequence

## Typical Performance Curves

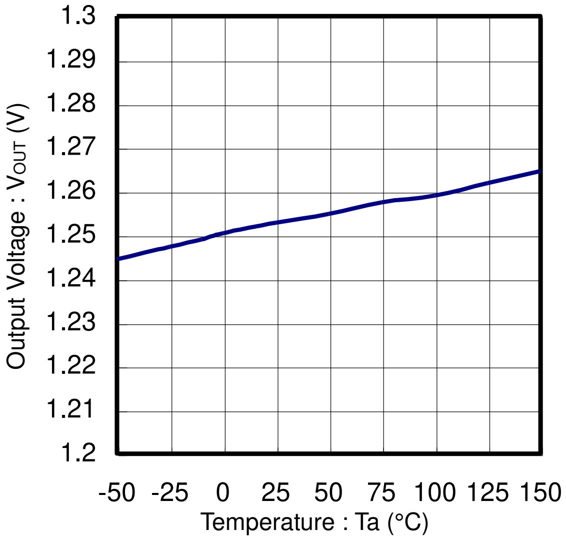



Figure 15. Output Voltage vs Temperature ($I_{OUT}$=0mA)

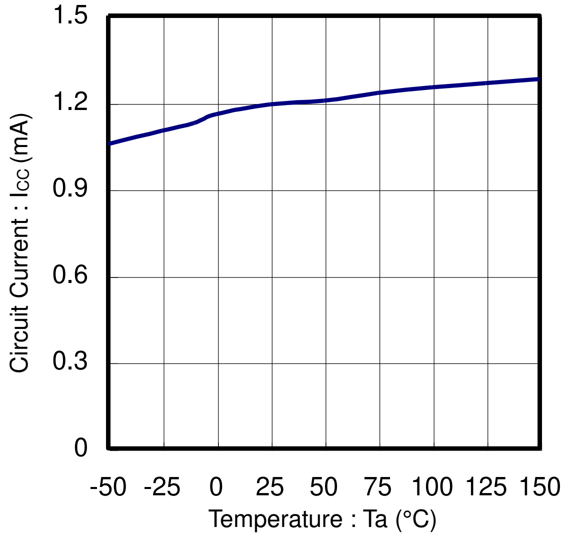



Figure 16. Circuit Current vs Temperature

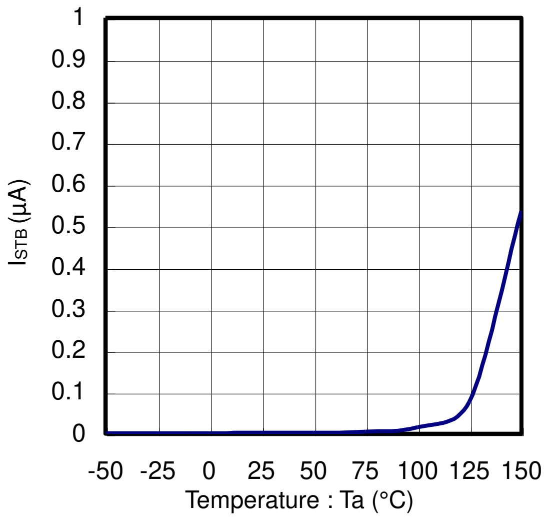



Figure 17. $I_{STB}$ vs Temperature

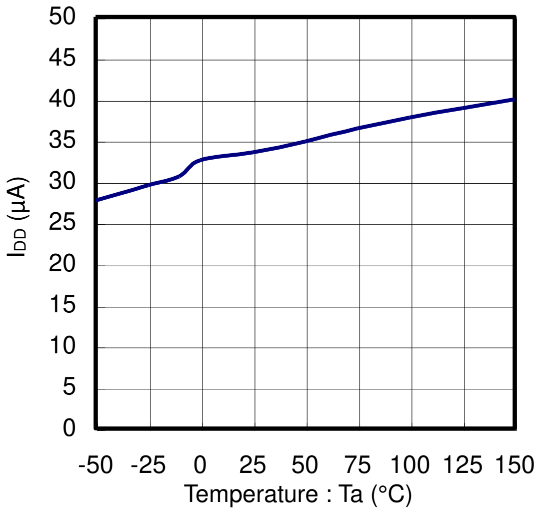



Figure 18. $I_{DD}$ vs Temperature

**Typical Performance Curves – continued**

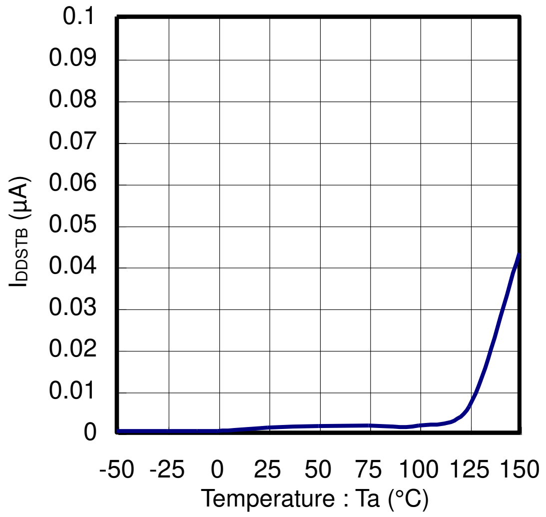



Figure 19. $I_{DDSTB}$ vs Temperature

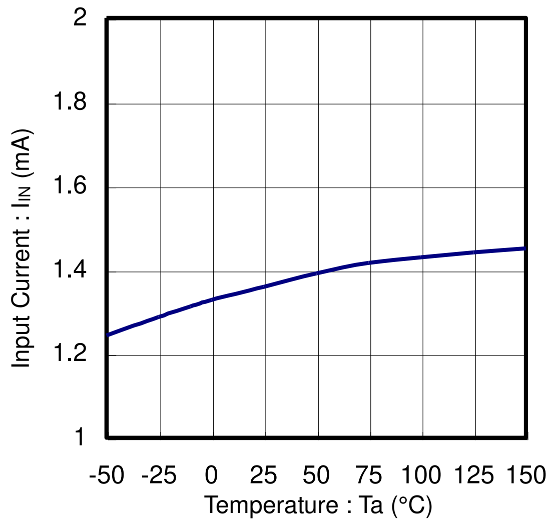



Figure 20. Input Current vs Temperature

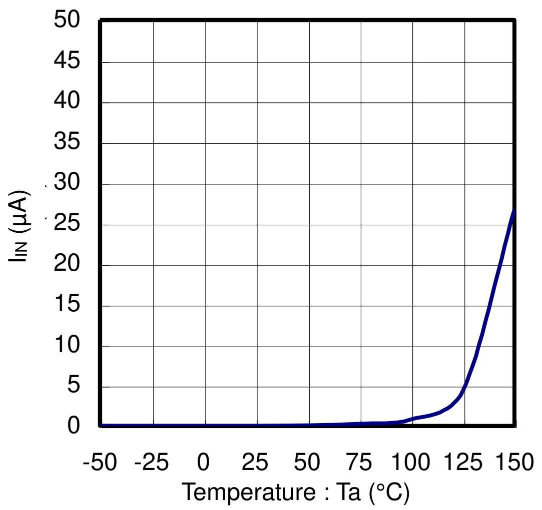



Figure 21. $I_{INSTB}$ vs Temperature

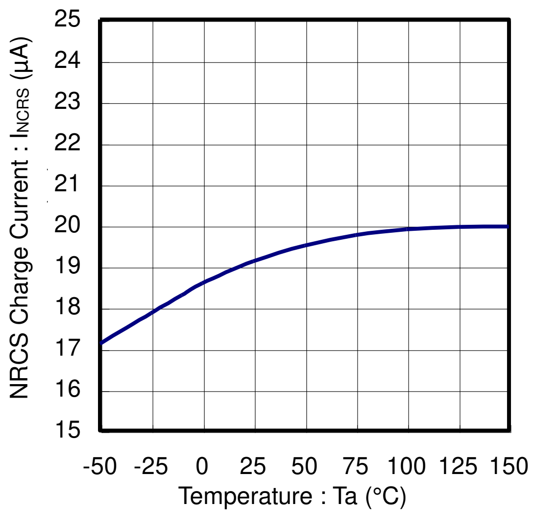



Figure 22. NRCS Charge Current vs Temperature

**Typical Performance Curves – continued**

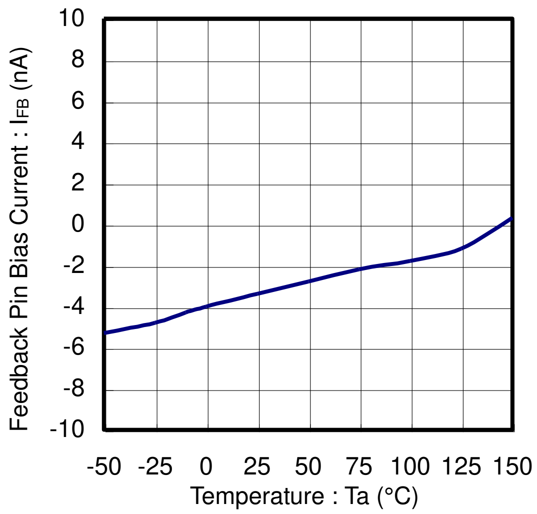



Figure 23. Feedback Pin Bias Current vs Temperature

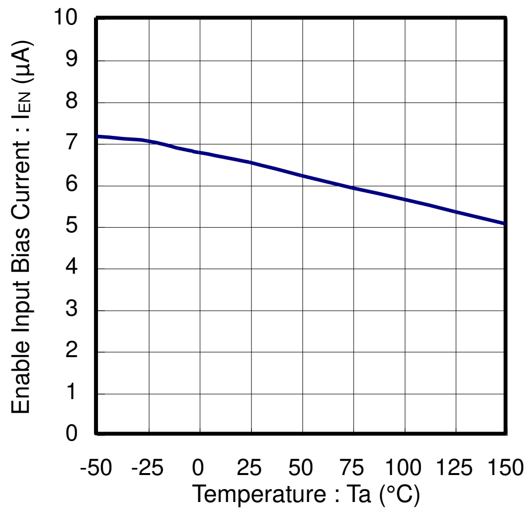



Figure 24. Enable Input Bias Current vs Temperature

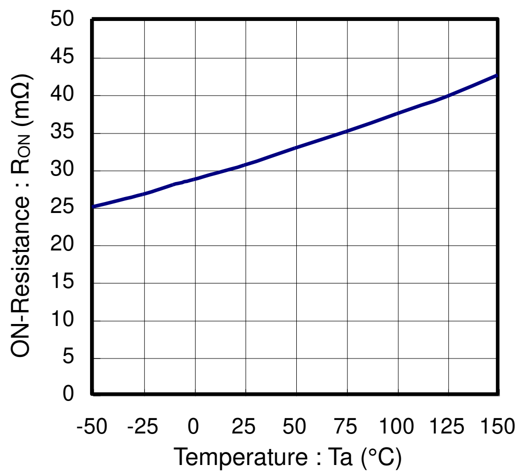



Figure 25. ON-Resistance vs Temperature
($V_{CC}$=5V/$V_{OUT}$=1.2V)

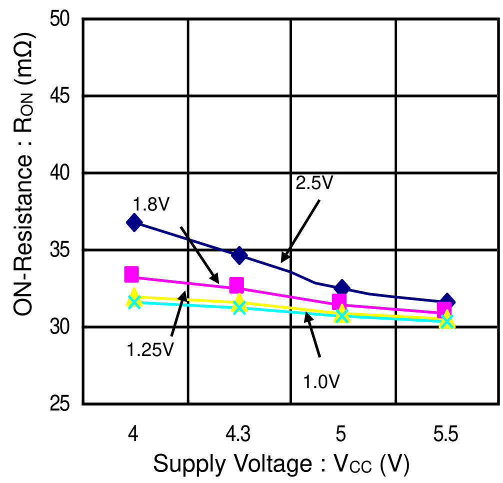
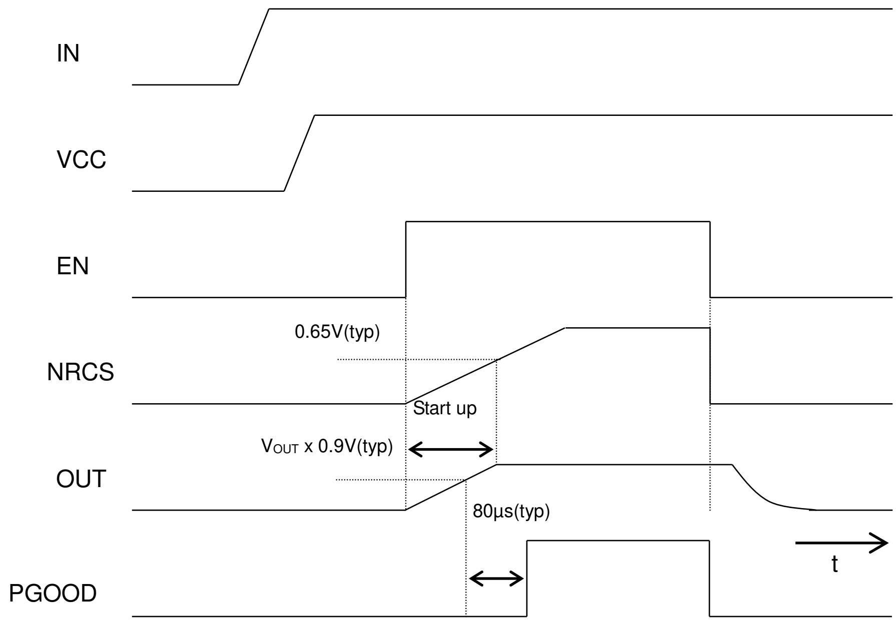


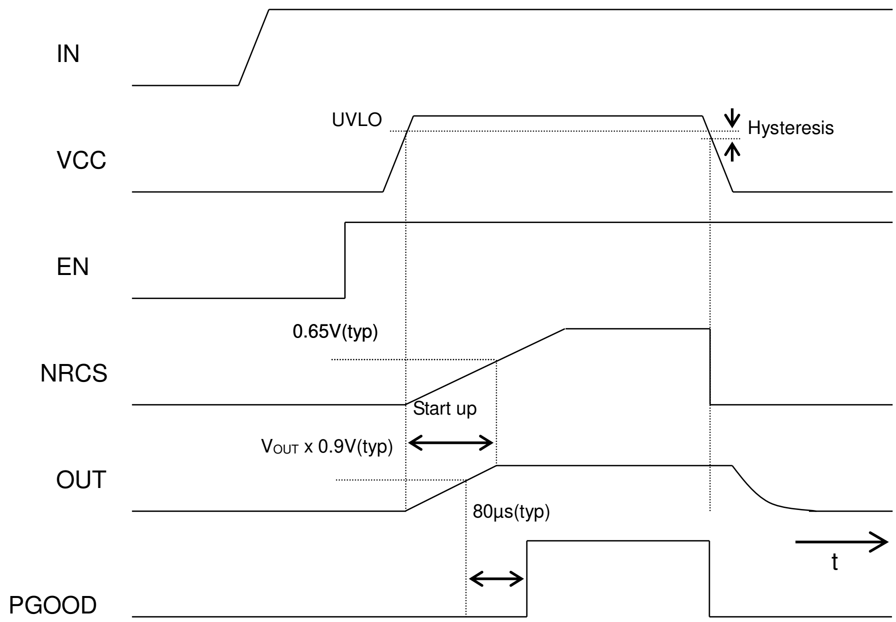

Figure 26. ON-Resistance vs Supply Voltage

### Timing Chart

EN ON/OFF



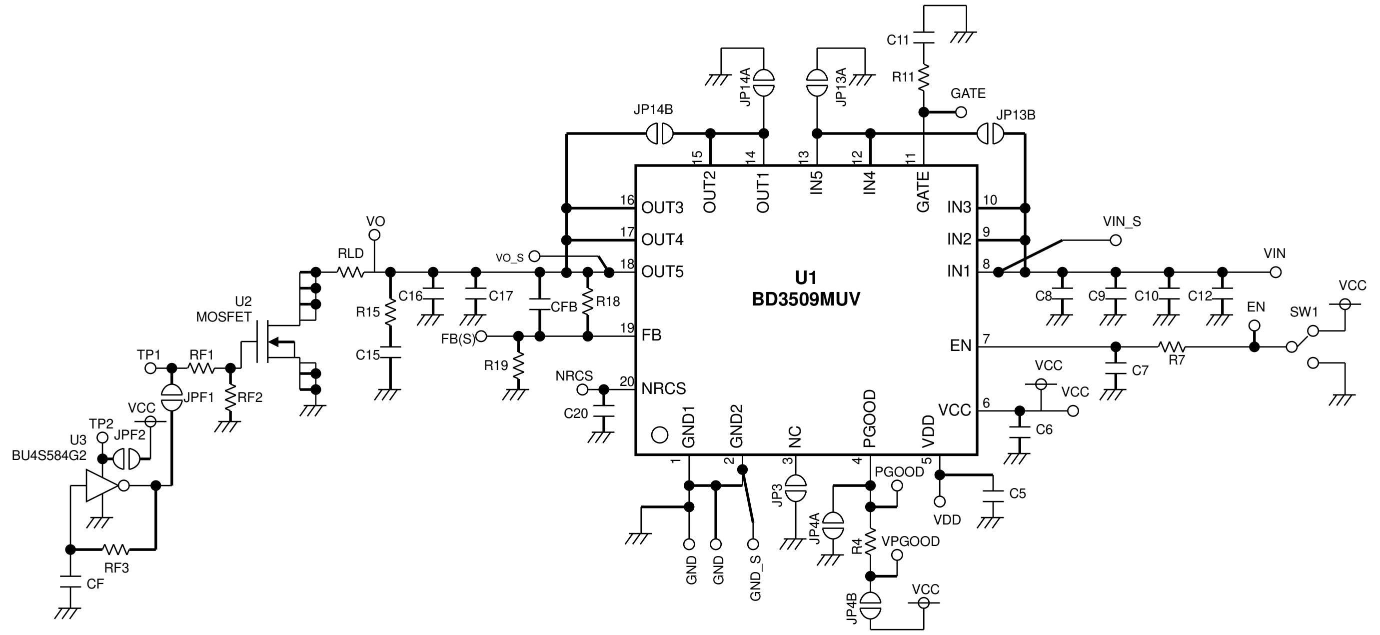

VCC ON/OFF



## Application Information

### 1. Evaluation Board

#### ■ Evaluation Board Schematic



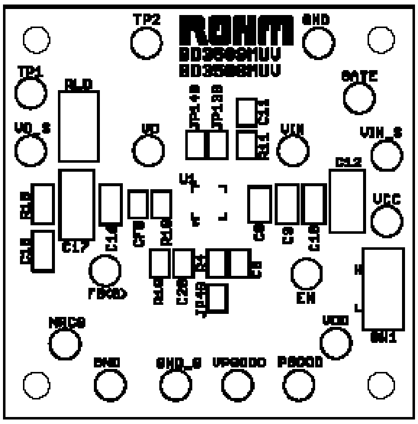

#### ■ Evaluation Board Standard Component List

| Component | Rating | Manufacturer | Product Name |
|---|---|---|---|
| U1 | - | ROHM | BD3509MUV |
| C5 | 0.1µF | MURATA | GRM155F11E104ZD |
| C6 | 1µF | MURATA | GRM188B11A105KD |
| C8 | 10µF | MURATA | GRM21BB10J106KD |
| C16 | 22µF | KYOCERA | CM315W5R226K06AT |
| C20 | 0.01µF | MURATA | GRM188B11H103KD |

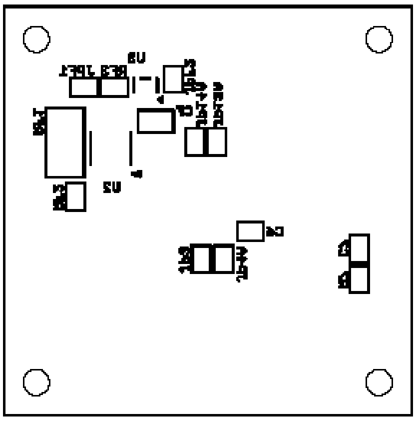
| Component | Rating | Manufacturer | Product Name |
|---|---|---|---|
| R4 | 100kΩ | ROHM | MCR03EZPF1003 |
| R7 | 0Ω | - | Jumper |
| R18 | 5.1kΩ | ROHM | MCR03EZPF5101 |
| R19 | 3.9kΩ | ROHM | MCR03EZPF3901 |
| CFB | 0.01µF | MURATA | GRM188B11H103KD |
| JP13B,JP14B | 0Ω | - | Jumper |

## ■ Evaluation Board Layout

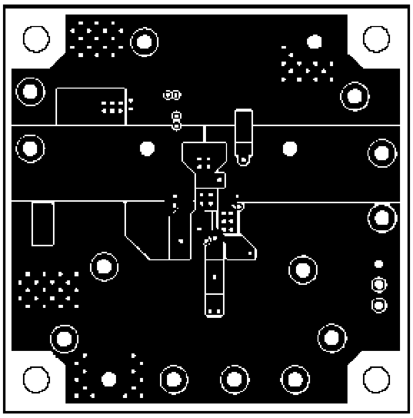
Silk Screen (Top)



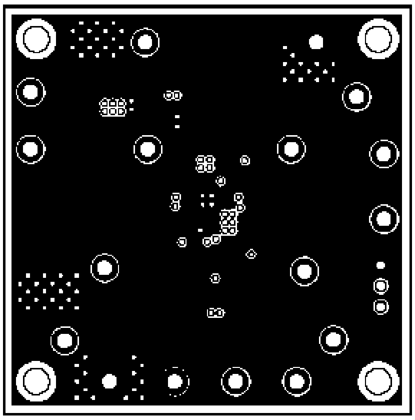
Silk Screen (Bottom)



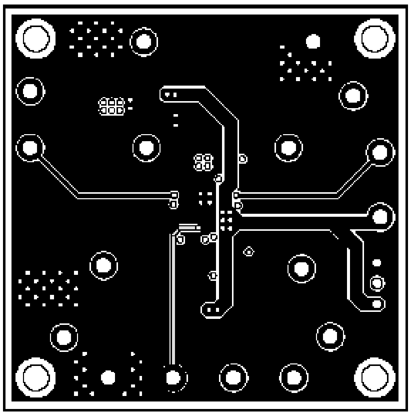
TOP Layer



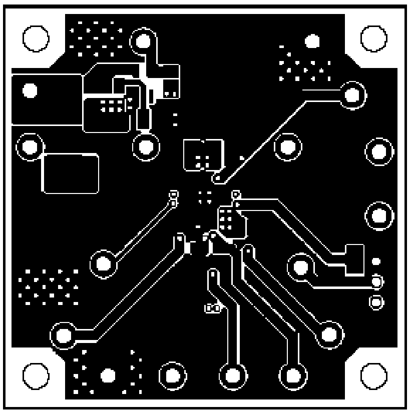
Middle Layer_1



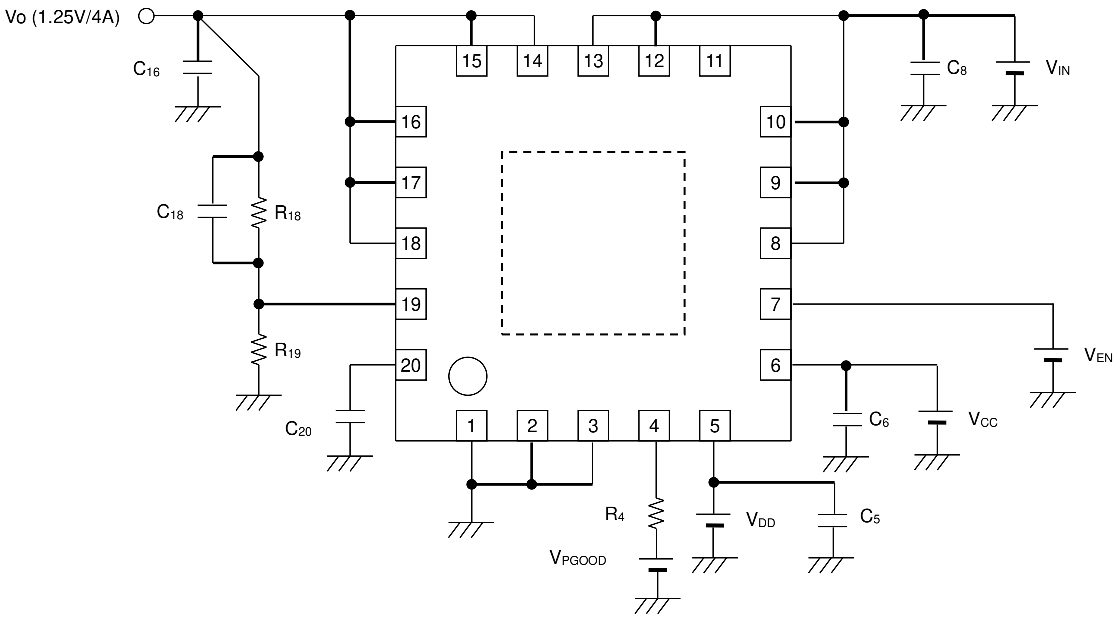
Middle Layer_2



Bottom Layer



## 2. Recommended Circuit Example



| Component | Recommended Value | Programming Notes and Precautions |
|---|---|---|
| $R_{18}$/$R_{19}$ | 3.6kΩ / 3.9kΩ | IC output voltage can be set by feedback voltage($V_{FB}$) and value of output voltage setting resistance($R_{18}$ $R_{19}$). Output voltage can be computed by $V_{FB}$ x ($R_{18}$+$R_{19}$)/$R_{19}$ but it is recommended to use at the resistance value(total:about 10kΩ) which is not susceptible to feedback pin bias current. |
| $R_4$ | 100kΩ | This is the pull-up resistance for open drain pin.<br>It is recommended to set the value about 100kΩ. |
| $C_{16}$ | 22µF | To ensure output voltage stability, OUT1～OUT5 should be connected to each other. In additions, GND pins should also be connected to each other. Output capacitors play a role in loop gain phase compensation and mitigation of output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series resistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22µF ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. Confirm the operation along a variety of temperature and load conditions. |
| $C_6$ | 1µF | The input capacitor reduces the output impedence of the voltage supply connected to the VCC. When the output impedence of this power supply increases, the input voltage ($V_{CC}$) may become unstable. This may result to output oscillation or lower ripple rejection. A low ESR 1µF capacitor with minimal susceptibility to temperature is preferable, but stability depends on the power supply characteristics and the substrate wiring pattern. Confirm the operation across a variety of temperature and load conditions. |
| $C_8$ | 10µF | Input capacitors reduce the output impedance of the voltage supply source connected to the IN input pins. If the impedance of this power supply were to increase, $V_{IN}$ input voltage could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 10µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. Confirm the operation across a variety of temperature and load conditions. |
| $C_5$ | 0.1µF | Input capacitors reduce the output impedance of the voltage supply source connected to the VDD input pins. If the impedance of this power supply were to increase, VDD input voltage could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 0.1µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. Confirm its operation across a variety of temperature and load conditions. |
| $C_{20}$ | 0.01µF | During power supply start-up, the Non-rush Current on Startup (NRCS) function prevents rush current flow from IN to OUT through the load, preventing impact on the output capacitors. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportional to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time. |
| $C_{18}$ | 0.01µF | This component is employed when the $C_{16}$ capacitor causes, or may cause, oscillation.<br>This provides more precise internal phase correction. |

**3. Heat Loss**

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

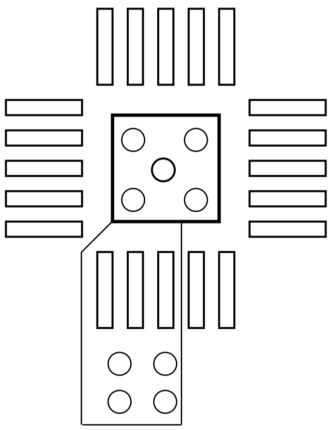
(1) Ambient temperature Ta can be no higher than 100°C.
(2) Chip junction temperature (Tj) can be no higher than 150°C.

Chip junction temperature can be determined as follows:

① Calculation based on ambient temperature (Ta)
<Reference values>
$Tj = Ta + \theta j - a \times W$

θj-a: VQFN020V4040 367.6°C/W IC only
178.6°C/W 1-layer board(copper foil area : 10.29mm$^2$)
56.6°C/W 4-layer board(copper foil area : front and reverse 10.29mm$^2$ , 2nd and 3rd 5505mm$^2$)
35.1°C/W 4-layer board(copper foil area : each 5505mm$^2$)
Substrate size: 74.2 x 74.2 x 1.6mm$^3$ (substrate with thermal via)

It is recommended to layout the heat radiation VIAs at the GND pattern (at the back of the IC) when there is the GND pattern in the inner layer (in using multiplayer substrate). However, because this package is very small (size: 4.0mm x 4.0mm) there is no available space to layout the VIA at the bottom of IC. Spreading the pattern and increasing the number of VIA like the figure below) can achieve superior heat radiation characteristic. (See figure below. the VIA quantity and size number are designed suitable for the actual situation.)



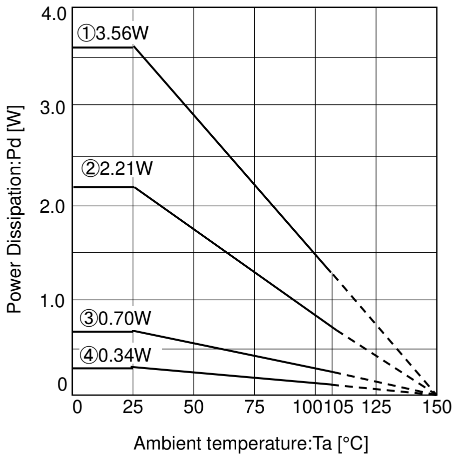
Most of the heat loss that occurs in BD3509MUV is from the output N-Channel FET. Power loss is determined by the total $V_{IN}$ -$V_{OUT}$ voltage and output current. In the design, be sure to confirm the system input, output voltage and the output current conditions in relation to the heat dissipation characteristics of the IN and OUT. Bear in mind that heat dissipation may vary substantially, depending on the substrate employed because due to the power package incorporated in BD3509MUV, consider conditions such as substrate size into thermal design.

Power consumption (W) = $\{$ Input voltage ($V_{IN}$)- output voltage ($V_{OUT}$)$\}$ x $I_{OUT}$ (Ave)

Example) $V_{IN}$=1.5V, $V_{OUT}$=1.25V, $I_{OUT}$(Ave) = 4A

$$Power\ consumption(W) = \{1.5(V) - 1.25(V)\} \times 4.0(A)$$
$$= 1.0(W)$$

## Power Dissipation



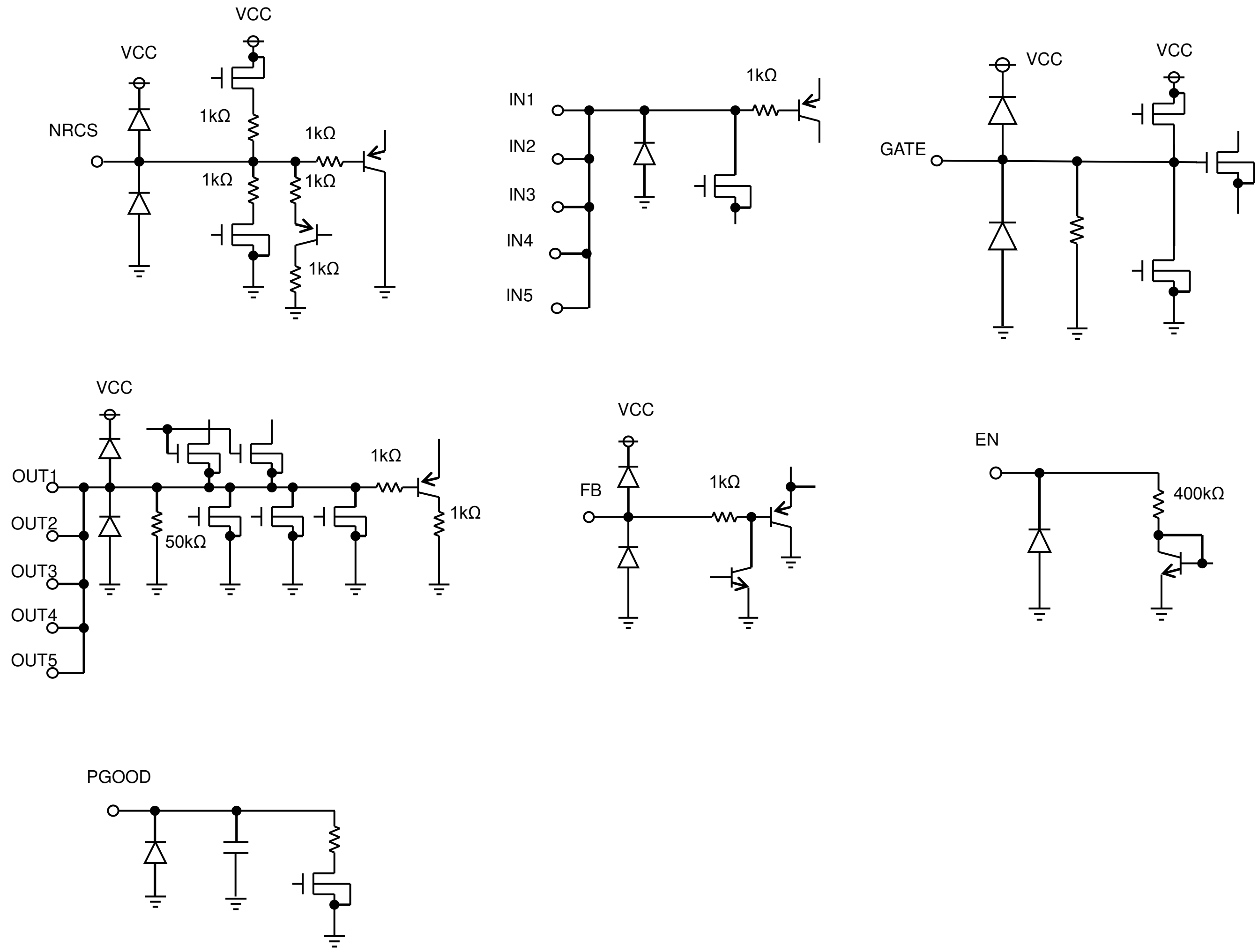

① 4 layers (Copper foil area : 5505mm²)
copper foil in each layers.
θj-a=35.1°C/W

② 4 layers (Copper foil area front and reverse : 10.29mm²、
2nd and 3rd : 5505mm²)
θj-a=56.6°C/W

③ 1 layer (Copper foil area : 10.29m²)
θj-a=178.6°C/W

④ IC only.
θj-a=367.6°C/W

## I/O Equivalent Circuits



## Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes – continued

**12. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

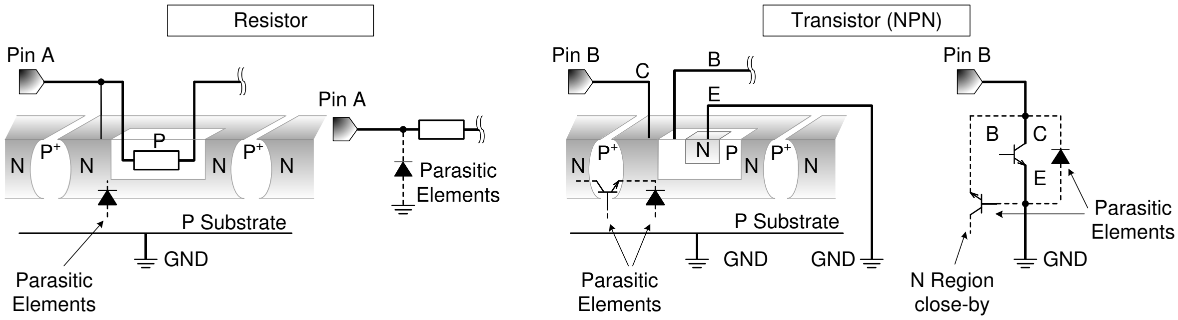



Figure 27. Example of monolithic IC structure

**13. Area of Safe Operation (ASO)**

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

**14. Thermal Shutdown Circuit(TSD)**

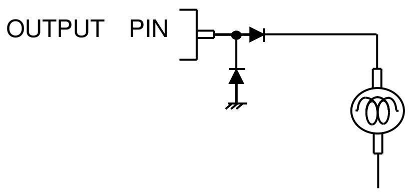
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

| | TSD on Temperature [°C] (typ) | Hysteresis Temperature [°C] (typ) |
|---|---|---|
| BD3509MUV | 175 | 15 |

**15. Output Pin**

In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

(Example)



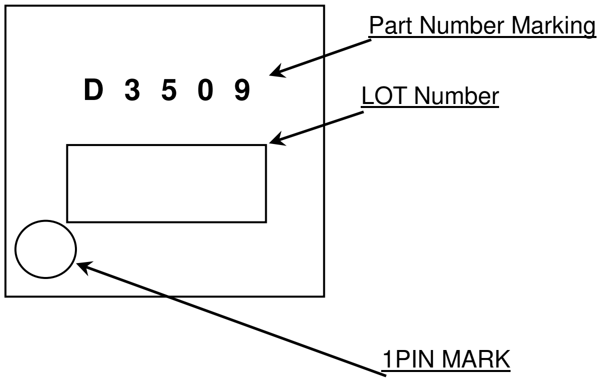
## Ordering Information

| B | D | 3 | 5 | 0 | 9 | M | U | V | - | E2 |
|---|---|---|---|---|---|---|---|---|---|---|

- Part Number
- Package
  MUV : VQFN020V4040
- Packaging and forming specification
  E2: Embossed tape and reel

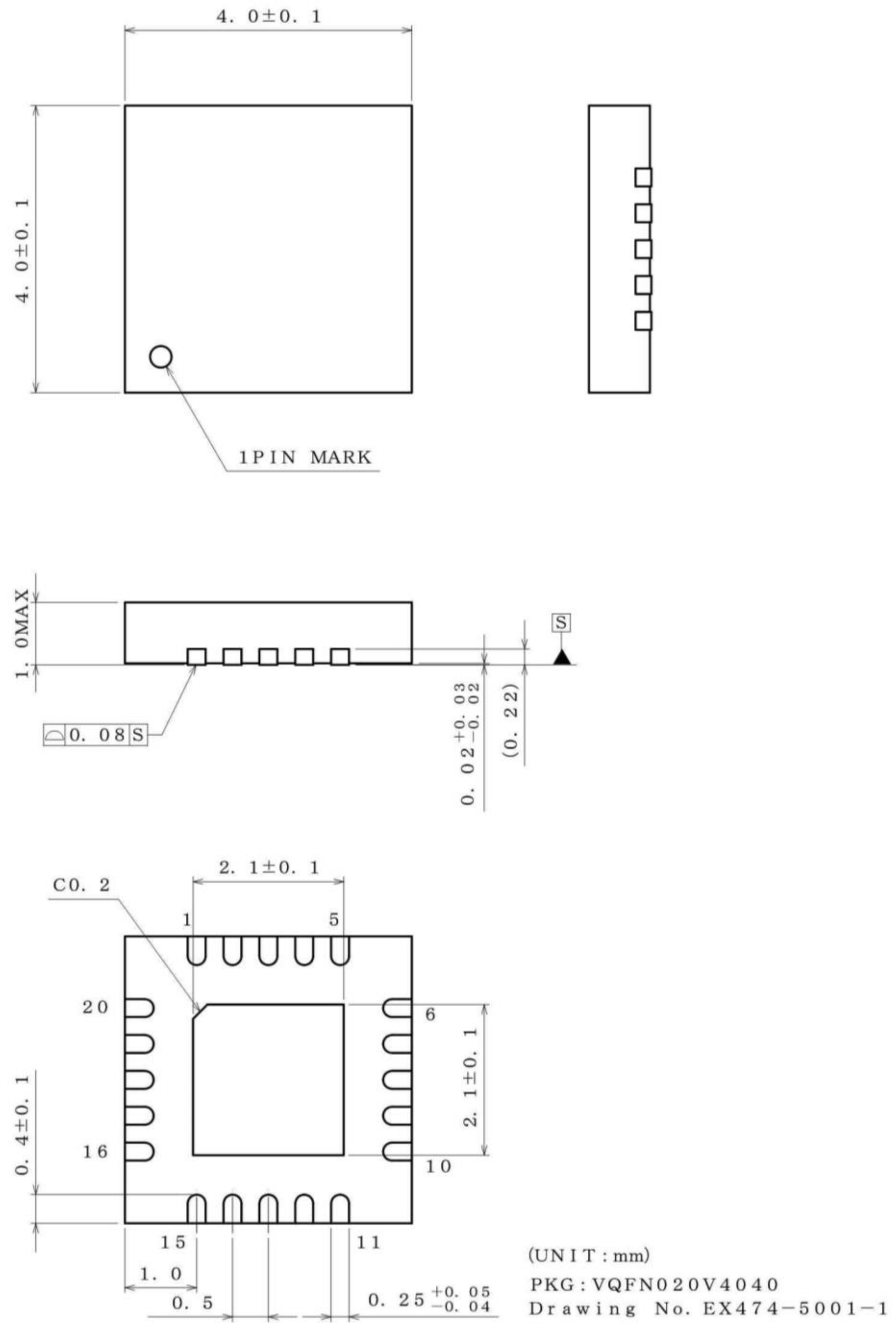
## Marking Diagram

VQFN020V4040 (TOP VIEW)



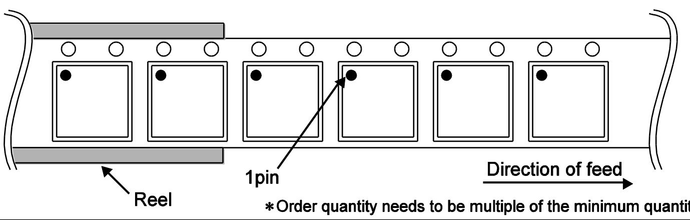
**Physical Dimension, Tape and Reel Information**

| Package Name | VQFN020V4040 |
|---|---|




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.

## Revision History

| Date | Revision | Changes |
|---|---|---|
| 02.Nov.2015 | 001 | New Release |

# Notice

## Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment [Note 1], transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

<table>
<tr><th>JAPAN</th><th>USA</th><th>EU</th><th>CHINA</th></tr>
<tr><td>CLASSⅢ</td><td rowspan="2">CLASSⅢ</td><td>CLASSⅡb</td><td rowspan="2">CLASSⅢ</td></tr>
<tr><td>CLASSⅣ</td><td>CLASSⅢ</td></tr>
</table>

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   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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QR code printed on ROHM Products label is for ROHM's internal use only.

## Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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