ISL54100A, ISL54101A, ISL54102A

TMDS Regenerators with Multiplexers

FN6725
Rev 0.00
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The ISL54100A, ISL54101A, ISL54102A are high-performance TMDS (Transition Minimized Differential Signaling) timing regenerators and multiplexers. The receiver contains a programmable equalizer and a clock data recovery (CDR) function for each of the 3 TMDS pairs in an HDMI or DVI signal. The TMDS data outputs of the ISL5410xA are regenerated and perfectly aligned to the regenerated TMDS clock signal, creating an extremely clean, low-jitter DVI/HDMI signal that can be easily decoded by any TMDS receiver.

The ISL5410xA's design and package footprint supports many compound configurations. Two ISL54100As can create a DualLink 4:1 mux, a 4:2 crosspoint, or an 8:1 mux. Additional ISL54100As can create larger combinations of these building blocks. The ISL54102A with its 2:1 multiplexing function serves applications with fewer inputs, while the ISL54101A can be used as a cable extender, to clean up a noisy/jittery TMDS source, or to provide a very stable TMDS signal to a marginal DVI or HDMI receiver.

Certified HDMI 1.3a compliant by the HDMI ATC for the following features: 12 bit Deep Color (1080i/720p guaranteed, 1080p typical), x.v.Color™, and all HDMI1.3 audio formats and options.

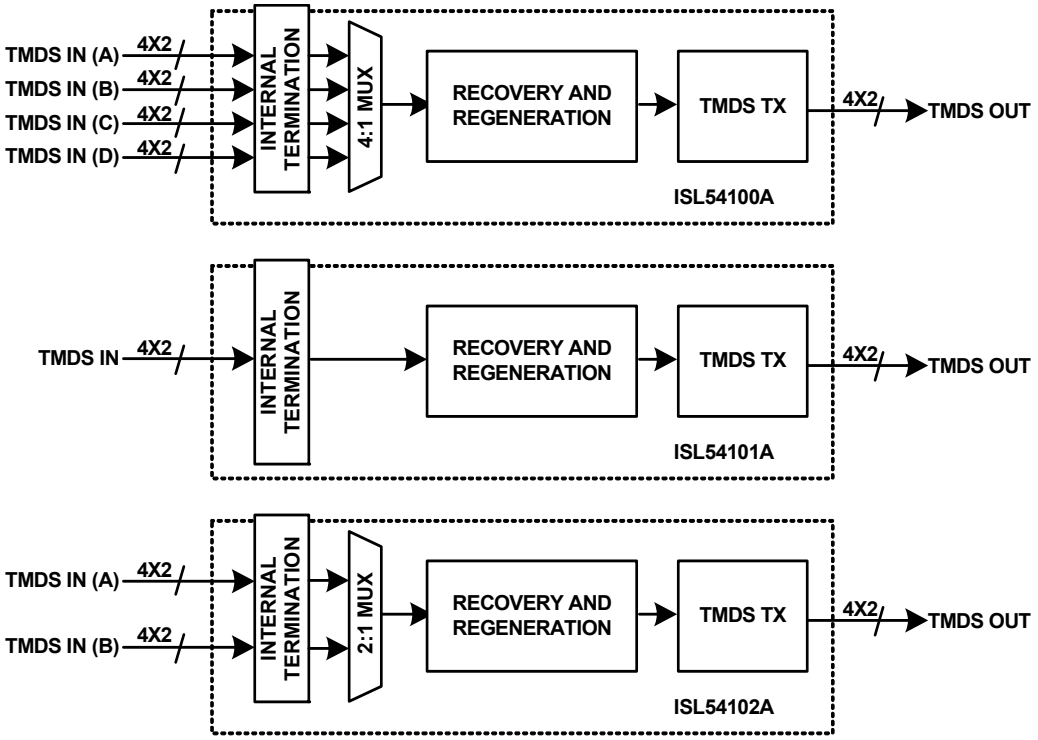
Features

- ISL54100A: 4:1 TMDS regenerator and multiplexer
- ISL54101A: 1:1 TMDS regenerator
- ISL54102A: 2:1 TMDS regenerator and multiplexer
- Clock Data Recovery and Retiming function enables use as TMDS range extender
- Programmable pre-emphasis on output driver
- Channel activity detect based on input TMDS clock activity
- Symmetrical pinout enables high-performance DualLink, 4:2 crosspoint and 8:1 multiplexing options
- Programmable internal 50Ω, 100Ω, or high-Z termination
- External pins for channel select, activity detection
- Stand-alone or I^2C software-controlled operation
- Hardware, software, or automatic channel selection
- Pb-free (RoHS compliant)

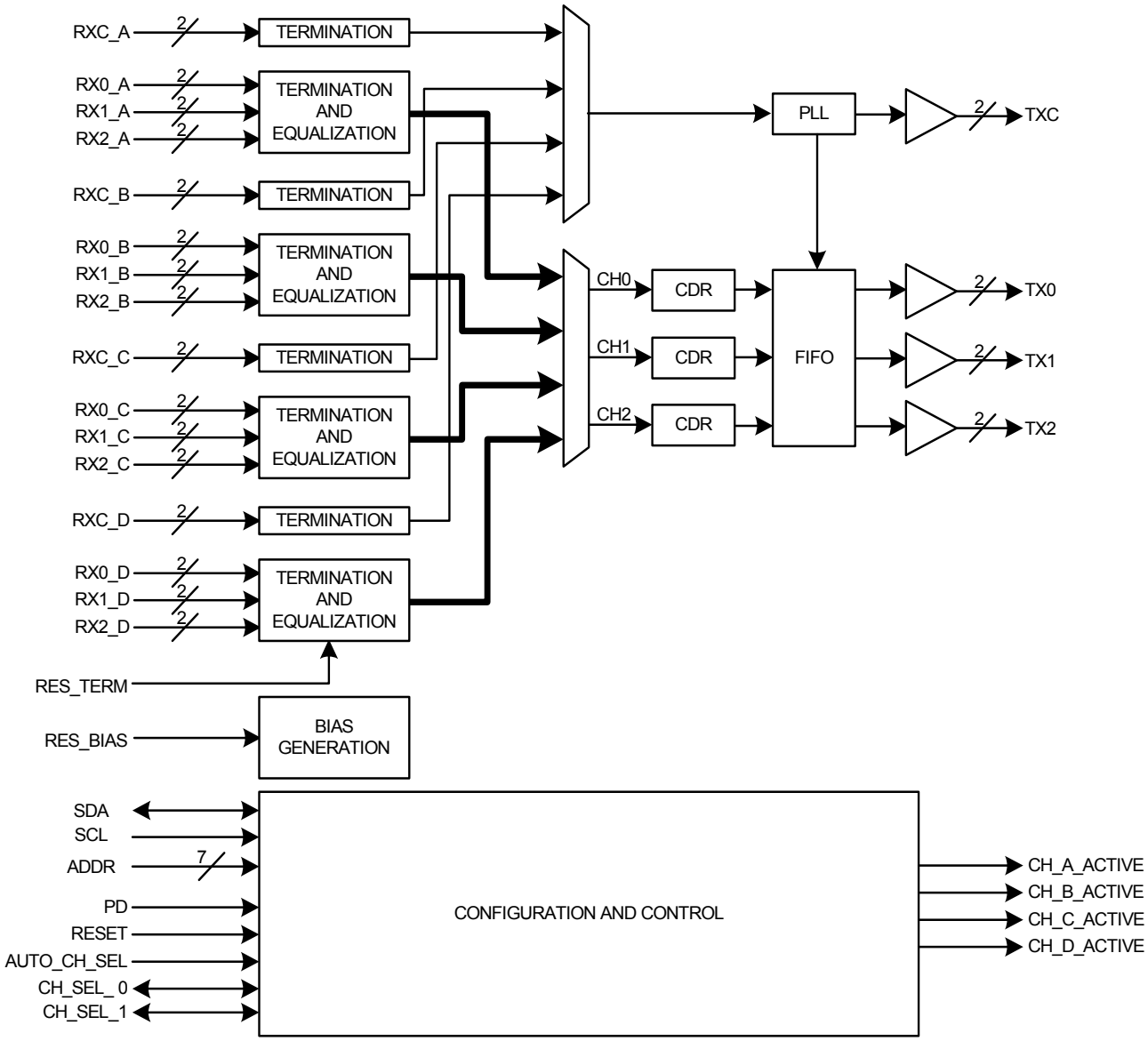
Applications

- KVM switches
- A/V receivers
- DVI/HDMI extenders
- Televisions/PC monitors/projectors

Block Diagrams



Block Diagram of ISL54100A *(ISL54101A, ISL54102A identical except for number of channels)*



Ordering Information

PART NUMBER (Note)	NUMBER OF CHANNELS	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54100ACQZ	4	0 to +70	128 Ld MQFP	MDP0055
ISL54101ACQZ	1	0 to +70	128 Ld MQFP	MDP0055
ISL54102ACQZ	2	0 to +70	128 Ld MQFP	MDP0055

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Voltage on V_D (referenced to GND). 4.0V
Voltage on any Input Pin (referenced to GND) . . . -0.3V to V_D+0.3V
Voltage on any “5V Tolerant” Input Pin
(referenced to GND). . . . . -0.3V to +6.0V
Current into any Output Pin . . . . . ±20mA
ESD Classification
Human Body Model . . . >4000V, higher voltage testing in progress
Machine Model . . . . . .>200V, higher voltage testing in progress

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
MQFP Package 60
Maximum Biased Junction Temperature . . . . . +125°C
Storage Temperature . . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature . . . . . 0°C to +70°C
Supply Voltage. . . . . V_D = 3.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Specifications apply for V_D = 3.3V, pixel rate = 165MHz, T_A = +25°C, RES_TERM = 1kΩ, RES_BIAS = 3.16kΩ, TMDS output load = 50Ω, TMDS output termination voltage V_{TERM} = 3.0V unless otherwise noted.

SYMBOL	PARAMETER	COMMENT	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
FULL CHANNEL CHARACTERISTICS						
f_{DATA_MAX}	Maximum Rx Clock Frequency/Pixel Rate	(Note 3)	165	225		MHz
f_{DATA_MIN}	Minimum Rx Clock Frequency/Pixel Rate				25	MHz
TMDS RECEIVER CHARACTERISTICS						
V_{SENS}	Minimum Differential Input Sensitivity			50	150	mV_{P-P}
R_{50}	50Ω Termination Resistance		45	50	55	Ω
R_{100}	100Ω Termination Resistance		90	97	110	Ω
CLK_{DUTY}	Rx Clock Duty Cycle		20		80	%
TMDS TRANSMITTER CHARACTERISTICS						
j_{TX_CLOCK}	Total Jitter on Clock Outputs	Independent of incoming jitter		32		ps
j_{TX_DATA}	Total Jitter on Data Outputs	Independent of incoming jitter		52		ps
$SKEW_{INTRA}$	Intra-Pair (+ to -) Differential Skew			±4		ps
$SKEW_{INTER}$	Inter-Pair (channel-to-channel) Skew	Added with respect to incoming inter-pair skew			2	UI
t_{RISE}	Rise Time into 50Ω Load to 3.3V	20% to 80%	80		240	ps
t_{FALL}	Fall Time into 50Ω Load to 3.3V	20% to 80%	80		240	ps
TX V_{OH}	Single-Ended High Level Output Voltage		V_{TERM} - 10		V_{TERM} + 10	mV
TX V_{OL}	Single-Ended Low Level Output Voltage		V_{TERM} - 600		V_{TERM} - 400	mV
DIGITAL SCHMITT INPUT CHARACTERISTICS						
V_{IH}	High Threshold Voltage		2.0			V
V_{IL}	High to Low Threshold Voltage				0.8	V
I	Input Leakage Current			±10		nA
R_{PU}	Internal Pull-Up Resistance	SDA and SCL pins		65		kΩ
R_{PD}	Internal Pull-Down Resistance	AUTO_CH_SEL, CH_SEL_x, RESET, ADDRx, PD pins		60		kΩ
C_{IN}	Input Capacitance			5		pF

Electrical Specifications

Specifications apply for V_D = 3.3V, pixel rate = 165MHz, T_A = +25°C, RES_TERM = 1kΩ, RES_BIAS = 3.16kΩ, TMDS output load = 50Ω, TMDS output termination voltage V_{TERM} = 3.0V unless otherwise noted.

SYMBOL	PARAMETER	COMMENT	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output HIGH Voltage, I_O = 8mA		2.4			V
V_{OL}	Output LOW Voltage, I_O = -8mA				0.4	V
POWER SUPPLY REQUIREMENTS						
V_D	Supply Voltage		3	3.3	3.6	V
I_D	Supply Current	All available inputs driven by 165Mpixel/s TMDS signals. Default register settings				
	ISL54100A			387	435	mA
	ISL54101A			357	405	mA
	ISL54102A			370	415	mA
I_D	Supply Current in Power-down Mode	All available inputs driven by 165Mpixel/s TMDS signals.		20	26	mA
AC TIMING CHARACTERISTICS (2-WIRE INTERFACE)						
f_{SCL}	SCL Clock Frequency		0		400	kHz
t_{AA}	SCL LOW to SDA Data Out Valid			200	470	ns
t_{BUF}	Time the Bus Must be Free Before a New Transmission Can Start		1.3			µs
t_{LOW}	Clock LOW Time		1.3	0.1		µs
t_{HIGH}	Clock HIGH Time		0.6	0.2		µs
$t_{SU:STA}$	Start Condition Setup Time		0.6	0.03		µs
$t_{HD:STA}$	Start Condition Hold Time		0.6	0.07		µs
$t_{SU:DAT}$	Data In Setup Time		100	0.03		ns
$t_{HD:DAT}$	Data In Hold Time		0			ns
$t_{SU:STO}$	Stop Condition Setup Time		0.6			µs
t_{DH}	Data Output Hold Time		160			ns

NOTE:

2. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
3. Operation up to 165MHz is guaranteed. While many parts will typically operate up to 225MHz, operation above 165MHz is not guaranteed.

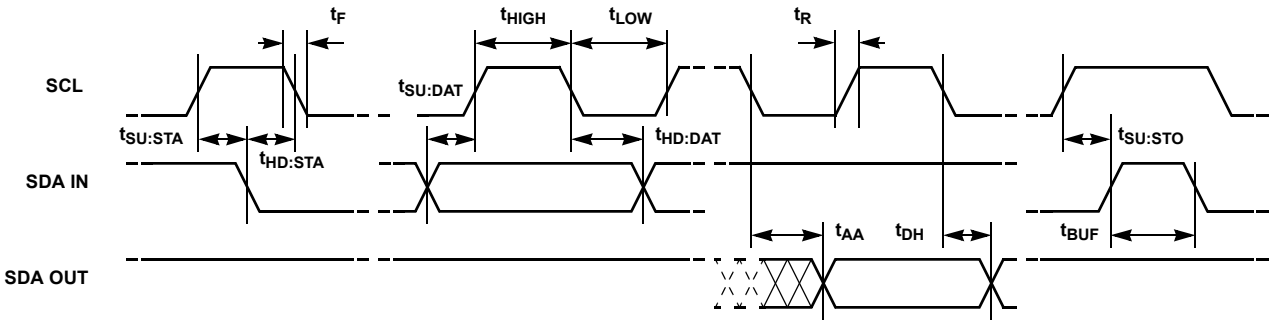
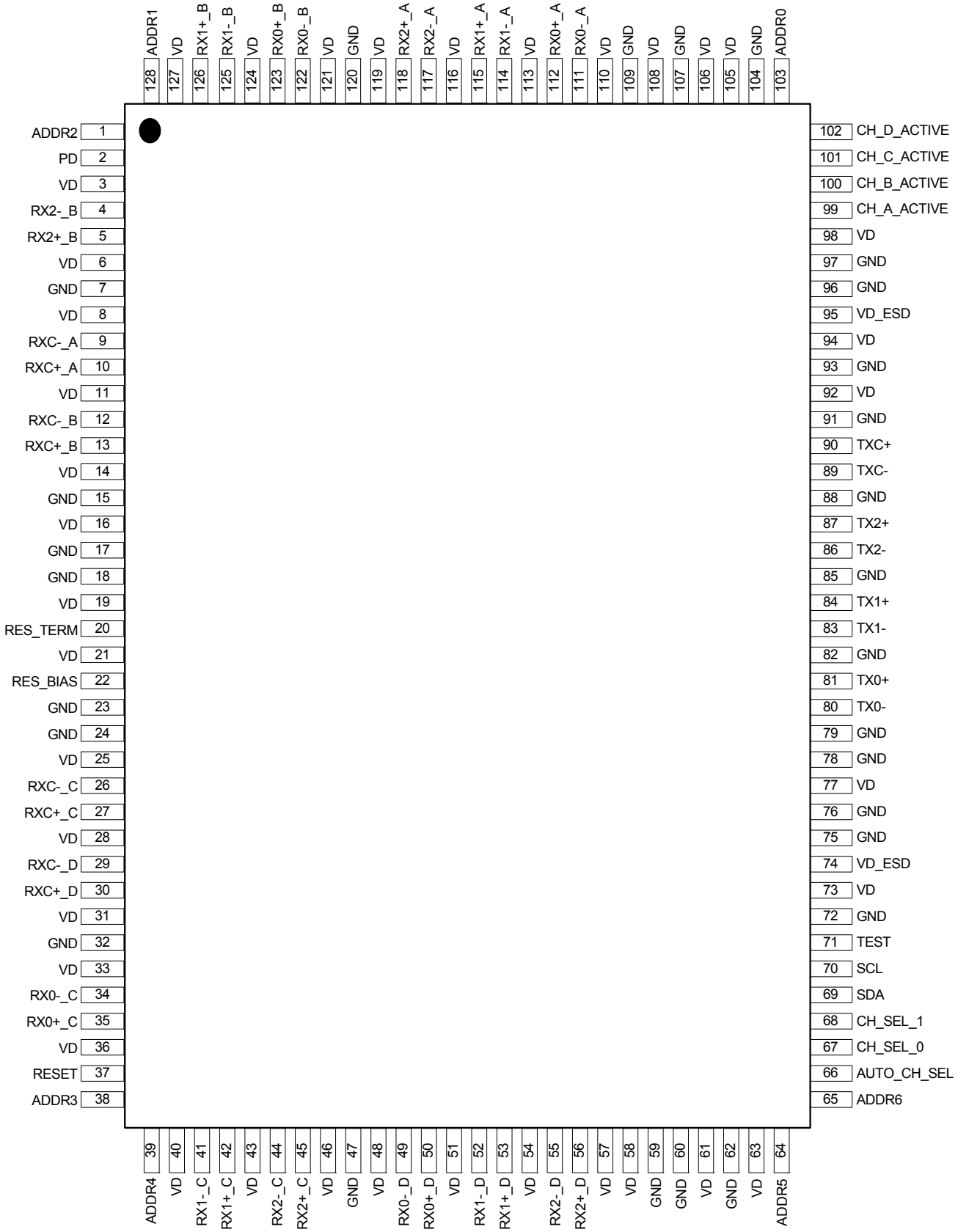
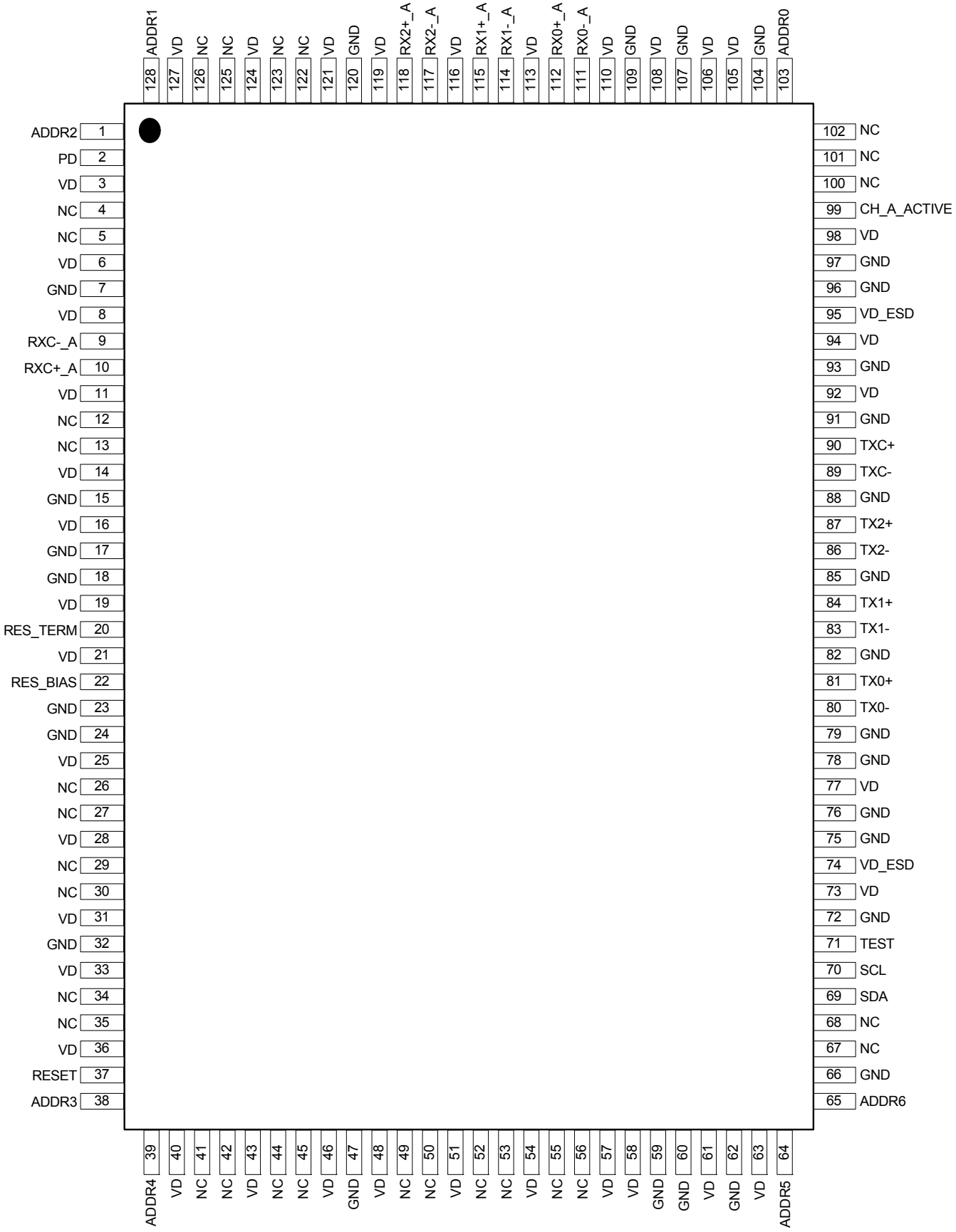


FIGURE 1. 2-WIRE INTERFACE TIMING

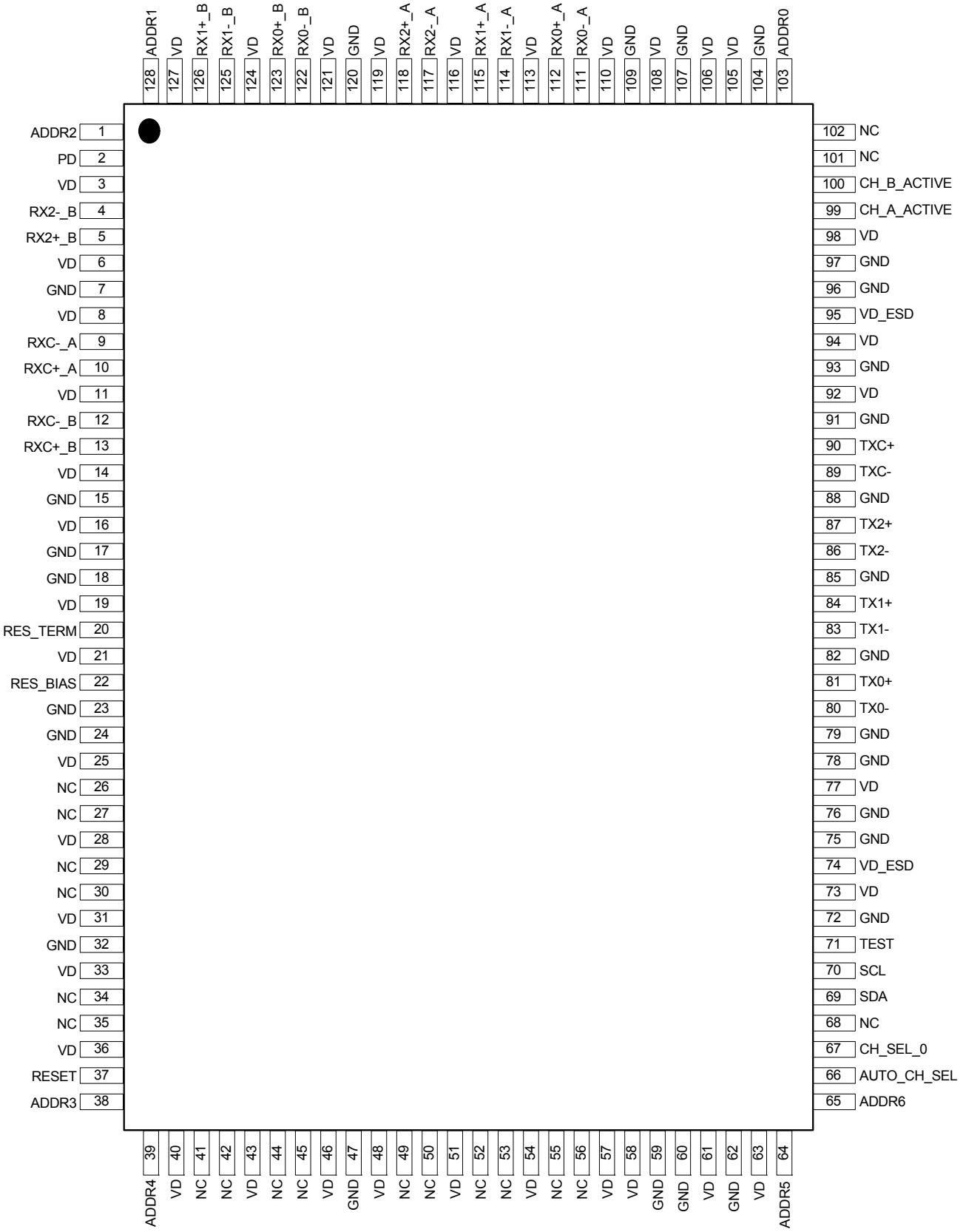
ISL54100A Pin Configuration



ISL54101A Pin Configuration



ISL54102A Pin Configuration



Pin Descriptions

SYMBOL	DESCRIPTION
RX0-_A, RX0+_A, RX1-_A, RX1+_A, RX2-_A, RX2+_A	TMDS Inputs. Incoming TMDS data signals for Channel A.
RX0-_B, RX0+_B, RX1-_B, RX1+_B, RX2-_B, RX2+_B	TMDS Inputs. Incoming TMDS data signals for Channel B (ISL54100A and ISL54102A only).
RX0-_C, RX0+_C, RX1-_C, RX1+_C, RX2-_C, RX2+_C	TMDS Inputs. Incoming TMDS data signals for Channel C (ISL54100A only).
RX0-_D, RX0+_D, RX1-_D, RX1+_D, RX2-_D, RX2+_D	TMDS Inputs. Incoming TMDS data signals for Channel D (ISL54100A only).
RXC-_A, RXC+_A, RXC-_B, RXC+_B, RXC-_C, RXC+_C, RXC-_D, RXC+_D	TMDS Inputs. Incoming TMDS clock signals for Channels A, B, C and D (ISL54100A), Channels A and B (ISL54102A), or Channel A (ISL54101A).
TX0-, TX0+, TX1-, TX1+, TX1-, TX1+	TMDS Outputs. TMDS output data for selected channel.
TXC-, TXC+	TMDS Outputs. TMDS output clock for selected channel.
SCL	Digital input, 5V tolerant, 500mV hysteresis. Serial data clock for 2-wire interface. Note: Internal 65kΩ pull-up to V_D.
SDA	Bidirectional Digital I/O, open drain, 5V tolerant. Serial data I/O for 2-wire interface. Note: Internal 65kΩ pull-up to V_D.
ADDR[6:0]	Digital inputs, 5V tolerant. 7-Bit address for serial interface. Note: Internal 60kΩ pull-down to GND.
CH_SEL_0, CH_SEL_1	Digital inputs, 3.3V. Channel select inputs for stand-alone operation. Pull to ground with a 47k resistor if unused.
AUTO_CH_SEL	Digital Input. Pull high to have the mux automatically select the highest channel (A is highest, D is lowest) with an active TMDS clock. Low is manual channel select.
CHA_Active, CHB_Active, CHC_Active, CHD_Active	Digital Outputs, 3.3V. Output goes high when there is an active TMDS clock on that channel's input. Used for activity detect in a stand-alone configuration. CHC_Active and CHD_Active are NC (do Not Connect) for the ISL54102A. CHB_Active, CHC_Active and CHD_Active are NC (do Not Connect) for the ISL54101A.
RES_BIAS	Tie to GND through a 3.16k external resistor. Sets up internal bias currents.
RES_TERM	Tie to VD through a 1.0k 1% external resistor. During calibration, the termination resistor closest in value to RES_TERM/20 (= 50Ω) is selected.
PD	Digital Input, 3.3V. PD = Power-down. Pull high to put the ISL5410xA in a minimum power consumption mode. **Note:** To ensure proper operation, this pin must be held low during power-up. It may be taken high 100ms after the power supplies have settled to 3.3V ±10%. When exiting Power-down, a termination resistor Recalibration cycle must be run to re-trim the termination resistors (see register 0x03[7]). Note: Internal 60kΩ pull-down to GND.
RESET	Digital Input, 3.3V. Pull high then low to reset the mux. Tie to GND in final application. Note: Internal 60k pull-down to GND.
TEST	Digital Input. Used for production testing only. Tie to GND in final application. This pin has an internal pulldown to GND, so it is also acceptable to leave this pin floating.
V_D	Power supply. Connect to a 3.3V supply and bypass each pin to GND with 0.1µF.
V_D_ESD	Power supply for ESD protection diodes. Connect one of these pins (pin 74 or 95) to the 3.3V V_D supply rail with a low V_F (0.4V or lower) Schottky diode, with the cathode connected to V_D_ESD and the anode connected to V_D. Bypass each pin to GND with 0.1µF.
GND	Ground return for V_D.

Register Listing

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x00	Device ID (read only)	3:0	Device Revision	1 = initial silicon, 2 = second revision, etc.
		7:4	Device ID	3 = ISL5410xA
0x01	Channel Activity Detect (read only)	0	Channel A Active	0: TMDS clock not present on Channel A 1: TMDS clock detected on Channel A
		1	Channel B Active	0: TMDS clock not present on Channel B 1: TMDS clock detected on Channel B
		2	Channel C Active	0: TMDS clock not present on Channel C 1: TMDS clock detected on Channel C
		3	Channel D Active	0: TMDS clock not present on Channel D 1: TMDS clock detected on Channel D
0x02	Channel Selection (0x0C)	1:0	Channel Select	Selects the input channel for the mux. These 2 bits are Read Only if Auto Channel Select is enabled. 0: Channel A selected 1: Channel B selected 2: Channel C selected 3: Channel D selected
		2	Auto Channel Select	0: Manual Channel Select (using bits 0 and 1). 1: Auto Channel Select. Mux always selects the active channel with the highest priority. A = 1st (highest), B = 2nd, C = 3rd, D = 4th (lowest) priority. An active channel is a channel that has clock activity on its TMDS clock lines. If no channels are active, the A channel is selected. (default)
		3	Hardware Channel Select	0: Software channel selection (using bits 0-2 of this register) 1: Hardware channel selection (using “Auto Channel Select” and “CH Sel 0/1” external pins) (default)
		4	Reset	Full chip reset. Write a 1 to reset. Will set itself to 0 when reset is complete.
		5	Power-down	0: Normal Operation 1: Puts the chip in a minimal power consumption mode, turning off all TMDS outputs and open-circuiting all TMDS inputs. This bit is OR'ed with the Power-down input pin. If either is set, the chip will enter power-down. Serial I/O stays operational in PD mode. Note: When exiting Power-down, a termination resistor Recalibration cycle must be run to re-trim the termination resistors (see register 0x03[7]).

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x03	Input Control (0x12) **Recommended default: 0x62**	0	Tri-state Unselected Clock Inputs	0: Normal Operation 1: Termination of unselected TMDS clock inputs is tri-stated to save power. Setting this bit will disable the activity detect function. This bit should not be set in crosspoint configuration because it will make the clock termination resistance variable depending on which 2 inputs are selected. In general, this bit should always be set to 0.
		1	Tri-state Unselected Data Inputs	0: Normal Operation 1: Unselected Data inputs are tri-stated to save power. This bit should not be set in crosspoint configuration because it will make the data input termination resistance variable depending on which 2 inputs are selected. (default)
		2	Tri-state Selected Clock Inputs	0: Selected Clock inputs are terminated into 50Ω/100Ω. 1: Selected Clock inputs are tri-stated (to allow chip to operate in parallel with another TMDS receiver with fixed 50Ω termination)
		3	Tri-state Selected Data Inputs	0: Selected Data inputs are terminated into 50Ω/100Ω. 1: Selected Data inputs are tri-stated (to allow chip to operate in parallel with another TMDS receiver with fixed 50Ω termination)
		4	Activity Detect Mode	0: AC Activity. Activity detection is based on the presence of AC activity on TMDS clock inputs. This setting (along with a hysteresis of 20mV enabled) provides reliable activity detection. (recommended setting) 1: Common Mode Voltage. If the common mode voltage is above ~3.05V, the input is considered inactive. This method has been found to be unreliable with small signal swings and should not be used. This setting is the silicon default but should be changed in software for more reliable activity detection.
		5	Clock Rx Hysteresis	Enables hysteresis for the clock inputs to prevent false clock detection when both inputs are high. Data inputs do not get hysteresis. 0: TMDS input hysteresis disabled 1: TMDS input hysteresis enabled. Eliminates false activity detects on unconnected channels. (recommended setting)
		6	Clock Rx Hysteresis Magnitude	Controls the amount of hysteresis in the clock inputs. 0: 10mV 1: 20mV (recommended setting)
		7	Recalibrate	0: Normal Operation 1: Recalibrates termination resistance. To recalibrate, take this bit high, wait at least 1ms, then take this bit low. Calibration is automatically done after power-on, but performing a recalibration after the supply voltage and temperature have stabilized may result in termination resistances closer to the desired 50Ω.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x04	Termination Control (0x00)	0	Data Termination A	0: Channel A TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel A TMDS Data inputs terminated into 100Ω (for paralleled inputs)
		1	Data Termination B	0: Channel B TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel B TMDS Data inputs terminated into 100Ω (for paralleled inputs)
		2	Data Termination C	0: Channel C TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel C TMDS Data inputs terminated into 100Ω (for paralleled inputs)
		3	Data Termination D	0: Channel D TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel D TMDS Data inputs terminated into 100Ω (for paralleled inputs)
		4	Clk Termination A	0: Channel A TMDS Clock inputs terminated into 50Ω (normal operation) 1: Channel A TMDS Clock inputs terminated into 100Ω (for paralleled inputs)
		5	Clk Termination B	0: Channel B TMDS Clock inputs terminated into 50Ω (normal operation) 1: Channel B TMDS Clock inputs terminated into 100Ω (for paralleled inputs)
		6	Clk Termination C	0: Channel C TMDS Clock inputs terminated into 50Ω (normal operation) 1: Channel C TMDS Clock inputs terminated into 100Ω (for paralleled inputs)
		7	Clk Termination D	0: Channel D TMDS Data inputs terminated into 50Ω (normal operation) 1: Channel D TMDS Data inputs terminated into 100Ω (for paralleled inputs)
0x05	Output Options (0x00)	0	Tri-state Clock Outputs	0: Normal Operation 1: Clock outputs tri-stated (allows another chip to drive the output clock pins)
		1	Tri-state Data Outputs	0: Normal Operation 1: Data outputs tri-stated (allows another chip to drive the output data pins)
		2	Invert Output Polarity	0: Normal Operation 1: The polarity of the TMDS data outputs is inverted (+ becomes -, - becomes +). TMDS clock unchanged.
		3	Reverse Output Order	0: Normal Operation 1: CH0 data is output on CH2 and CH2 data is output on CH0. No change to CH1.
0x06	Data Output Drive (0x00)	3:0	Transmit Current	Transmit Drive Current for data signals, adjustable in 0.125mA steps. Clock current is fixed at 10mA. 0x0: 10mA 0x8: 11mA 0xF: 11.875mA
		7:4	Transmit Pre-emphasis	Drive boost (in 0.125mA steps) added during first half of each bit period for data signals. Clock signals do not have pre-emphasis. 0x0: 0mA 0x8: 1mA 0xF: 1.875mA

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x07	Equalization 1 (0xCC)	3:0	Channel A Equalizer Gain	Boost (dB) = 1dB + <gain value> * 0.8dB 0x0: 1dB boost at 800MHz 0xC: 10.6dB boost at 800MHz (default) 0xF: 13dB boost at 800MHz
		7:4	Channel B Equalizer Gain	
0x08	Equalization 2 (0xCC)	3:0	Channel C Equalizer Gain	Boost (dB) = 1dB + <gain value> * 0.8dB 0x0: 1dB boost at 800MHz 0xC: 10.6dB boost at 800MHz (default) 0xF: 13dB boost at 800MHz
		7:4	Channel D Equalizer Gain	
0x09	Test Pattern Generator (0x00)	1:0	Generator Mode	When a 25MHz to 165MHz clock is applied to the selected channel's clock input, this function will output a PRBS7 pattern on the TX pins. 0: Normal operation (test patterns disabled) 1: PRBS7 pattern 2: Low frequency toggle (0000011111…) 3: High frequency toggle (1010101010…) Note: When switching from the high frequency toggle pattern to the low frequency toggle pattern, you must first select normal operation.
		2	Enable PRBS7 Error Counter	Enables PRBS7 error counter in registers 0x0A to 0x0C. 0: Disable PRBS7 Error Counter 1: Enable PRBS7 Error Counter
0x0A	PRBS7 Error Counter Link 0 (read only)	7:0	PRBS7 Error Counter Link 0	PRBS7 Error Counter of Link 0. Saturates at 0xFF. Reading this register clears this register at end of read
0x0B	PRBS7 Error Counter Link 1 (read only)	7:0	PRBS7 Error Counter Link 1	PRBS7 Error Counter of Link 1. Saturates at 0xFF. Reading this register clears this register at end of read
0x0C	PRBS7 Error Counter Link 2 (read only)	7:0	PRBS7 Error Counter Link 2	PRBS7 Error Counter of Link 2. Saturates at 0xFF. Reading this register clears this register at end of read
0x10	PLL Bandwidth (0x10) **Recommended default: 0x12**	1:0	PLL Bandwidth	Selects between 4 PLL bandwidth settings 0: 4MHz (silicon default) 1: 2MHz 2: 1MHz (recommended default) 3: 500kHz 1MHz provides slightly better performance with high jitter/ high noise signals.
		7:2	Reserved	Keep set to 000100 binary.

Application Information

The ISL54100A, ISL54101A, and ISL54102A are TMDS regenerators, locking to the incoming DVI or HDMI signal with triple Clock Data Recovery units (CDRs) and a Phase Locked Loop (PLL). The PLL generates a low jitter pixel clock from the incoming TMDS clock. The TMDS data signals are equalized, sliced by the CDR, re-aligned to the PLL clock, and sent out the TMDS outputs. The ISL54100A and ISL54102A also include an input multiplexer.

Compatibility With the ISL5410x Family

The ISL54100A and ISL54102A are plug-in and backwards compatible with the ISL54100 and ISL54102 in every respect except one: the CH_SEL pins.

The CH_SEL pins on the ISL54100 and ISL54102 are bi-directional. They can be used as inputs to externally chose which channel is selected, or they can be used as outputs to indicate which channel has been selected (either via I^2C programming or automatic selection).

However the CH_SEL pins on the ISL54100A and ISL54102A are *inputs only*. When channel selection is done via I2C programming or automatically, these pins are floating, and should be pulled to ground via 47k resistors.

The ISL54101A does not have any CH_SEL pins and is therefore 100% plug-in and backwards compatible with the ISL54100.

Multiplexer Operation

The ISL54100A and ISL54102A have 4:1 and 2:1 (respectively) input multiplexers. After power-up or a hardware reset, the IC defaults to hardware channel selection, using the AUTO_CH_SEL and CH_SEL_x pins. If AUTO_CH_SEL is pulled high, the highest priority channel with an active TMDS clock will be automatically selected (Channel A = highest priority, B = second highest priority, C = second lowest, and D = lowest priority). If, for example, a DVD player is attached to Channel A, a set-top-box (STB) is attached to Channel B, and a video game is attached to Channel C, the DVD player will have the highest priority, overriding the STB and the video game whenever the DVD player is transmitting a TMDS clock. Likewise, the STB will have higher priority than the video game. Table 1 shows the auto channel selection priority matrix.

TABLE 1. AUTO CHANNEL SELECTION PRIORITIES (ISL54102A OPTIONS IN BLUE)

CHANNEL A	CHANNEL B	CHANNEL C	CHANNEL D	OUTPUT
Inactive	Inactive	Inactive	Inactive	Inactive
Active	Don't Care	Don't Care	Don't Care	Channel A
Inactive	Active	Don't Care	Don't Care	Channel B
Inactive	Inactive	Active	Don't Care	Channel C
Inactive	Inactive	Inactive	Active	Channel D

In the auto channel select mode, the selected channel can be determined by reading register 0x02 bits 1:0.

If manual channel selection is desired, the AUTO_CH_SEL pin should be tied to ground and the CH_SEL_x pins used to select the desired channel.

The input multiplexer can also be controlled by software via the I^2C interface. Software control is initiated by writing a 0 to the Hardware Channel Select bit (bit 3 of register 0x02). In this case, the Auto Channel Select bit (bit 2 of register 0x02) and the Channel Select bits (bits 0 and 1 of register 0x02) perform the same functions as the external pins described above. In the Auto Channel Select mode, the Channel Select bits are read only, indicating the currently selected channel. In the Manual Channel Select mode, the Channel Select bits are read/write, and used to select the channel.

Activity Detection

A channel is considered active using one of two methods. The original default activity detect method (register 0x03b4 = 1) is to measure the common mode of the TMDS clock input for each channel. If the common mode is 3.3V, it indicates that there is nothing connected to that input, or that whatever is connected is turned off (inactive). This has been found to be relatively unreliable, particularly with weak signals.

The preferred method of activity detection is looking for an active AC signal on the TMDS clock input for that channel (register 0x03b4 = 1). This is more robust, however disconnected inputs will cause both inputs to the differential receiver to be the same level - 3.3V. If the offset error of the differential TMDS receiver is very small, the receiver can not resolve a 1 or a 0 and will randomly switch between states, which may be detected as an active clock. Register 0x03 bits 5 and 6 allow a 10mV or 20mV offset to be added to the input stage of the clock inputs, eliminating this problem. This offset will slightly reduce the sensitivity of TMDS receiver for the clock lines, but since the clock signals are much lower frequency than the data, they will not be nearly as attenuated, so this is not a problem in practice.

Again, using the AC activity detection method (register 0x03b4 = 0) is recommended.

Rx Equalization

Registers 0x07 and 0x08 control the amount of equalization applied to the TMDS inputs, with 4 bits of control for each channel. The equalization range available is from a minimum of 1dB boost to a maximum of 13dB at 800MHz, in 0.8dB increments. Ideally, the equalization is adjusted in the final application to provide optimal performance with the specific DVI/HDMI transmitter and cable used. In general, the amount of equalization required is proportional to the cable length. If the equalization must be fixed (can not be adjusted in the final application), an equalization setting of 0xA works well with short cables as well as medium to longer cables.

Tx Pre-emphasis

The transmit pre-emphasis function sinks additional current during the first bit after every transition, increasing the slew rate for a given capacitance, and helping to maintain the slew rate when using longer/higher capacitance cables. Pre-emphasis is controlled by register 0x06 bits 7:4, and ranges from a minimum of 0mA (no pre-emphasis) to 1.875mA (max pre-emphasis).

PLL Bandwidth

The 2-bit PLL Bandwidth register controls the loop bandwidth of the PLL used to recover the incoming clock signal. The default 4MHz setting works well in most applications, however a lower bandwidth of 1MHz has proven to work just as well with good TMDS sources and slightly better with marginal sources.

Power-down

The chip can be placed in a Power-down mode when not in use to conserve power. Setting the Power-down bit (register 0x02 bit 5) to a 1 or pulling the PD input pin high places the chip in a minimal power consumption mode, turning off all TMDS outputs and disconnecting all TMDS inputs. Serial I/O stays operational in PD mode. Note that the PD pin must be low during power-on in order to initialize the I^2C interface.

Note: When exiting Power-down, a termination resistor Recalibration cycle must be run to re-trim the termination resistors (see register 0x03[7]).

Power Dissipation and Supply Current

Due to the large number of TMDS inputs and outputs, a significant amount of current flows into and out of the SL5410x. This makes calculating the total power dissipation of the ISL5410xA slightly more complicated than simply multiplying the supply current by the supply voltage.

The supply current measurement includes the current flowing through all the active TMDS termination resistors. This current is supplied by the ISL5410xA's V_D supplies, but only 15% of it (0.5V*10mA per TMDS pair) is dissipated as power inside the ISL5410xA. The majority of the power (2.8V * 10mA per active TMDS pair) is dissipated in the TMDS transmitter driving the ISL5410xA. Likewise, the ISL5410xA dissipates 85% of the power generated by the current from the external receiver attached to the ISL5410xA's Tx pins. Any worst-case on-chip power dissipation calculation needs to account for this.

Inter-Pair (Channel-to-Channel) Skew

The read pointers for Channel 0, 1, and 2 of the FIFO that follows the CDR all have the same clock, so all 3 channels transition within a few picoseconds of each other - there is essentially no skew between the transitions of the three channels.

However the FIFO read pointers may be positioned up to 2 bits apart relative to each other, introducing a random, fixed channel-to-channel skew of skew of 1 or (much less frequently) 2 bits. The random skew is introduced whenever there is a discontinuity in the input signal (typically a video mode change or a new mux channel selection). After the CDRs and PLL lock, the skew is fixed until the next discontinuity. This adds up to 2 bits of skew in addition to any incoming skew, as shown in the following examples.

Figure 2 shows an input (the top three signals) with essentially no skew. After the ISL5410xA locks on to the signal, there may be 1 bit of skew on the output, as shown in Figure 2.

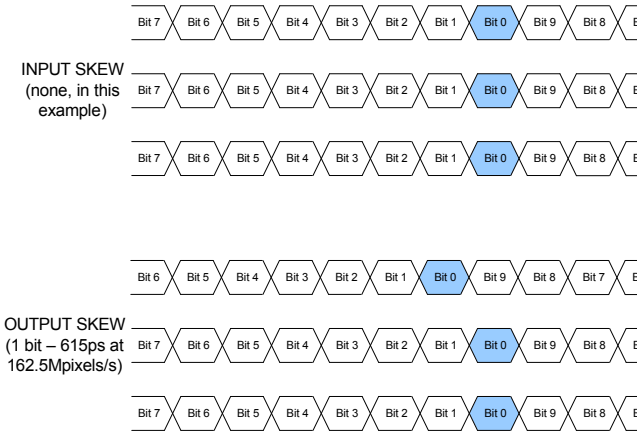


FIGURE 2. MAXIMUM ADDITIONAL INTERCHANNEL SKEW FOR INPUTS WITH NO OR LITTLE SKEW

When there is pre-existing skew on the input, the ISL5410xA can add up to 2 bits to the channel-to-channel skew. In the example in Figure 3, the incoming red channel has 2.3 bits of skew relative to the incoming green and blue. The FIFO's quantization (worst case) increases the total skew to 4.0 bits.

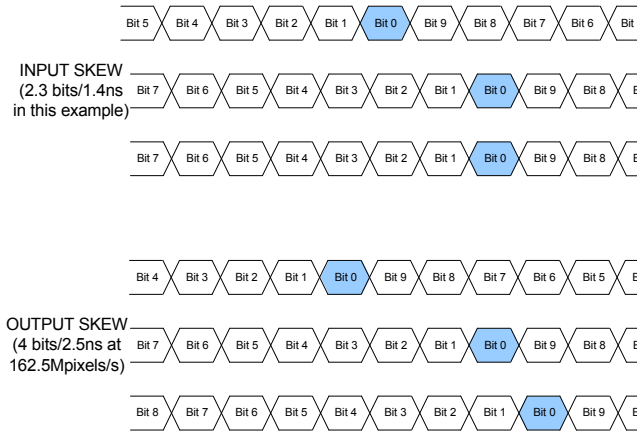


FIGURE 3. MAXIMUM ADDITIONAL INTERCHANNEL SKEW FOR INPUTS WITH MODERATE TO LARGE SKEW

While increasing skew is not desirable, DVI and HDMI receivers are required to have a minimum of 6 bits of inter-pair skew tolerance, so the addition of 2 bits of skew is only a problem with the most pathological cables and transmitters. It

does, however, limit the number of ISL5410xAs that can be put in series (although statistically, it is unlikely that all the skews would line up in a worst-case configuration).

Typical Performance

Setup A (Figure 4) was used to capture the TMDS eye diagrams shown in Figure 5 and Figure 6:

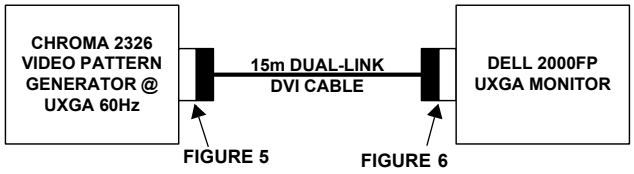


FIGURE 4. TEST SETUP A

The 162.5Mpixel/s (UXGA 60Hz) DVI output of the Chroma 2326 was terminated into a TPA2 Plug adapter and measured with a LeCroy differential probe and 6MHz SDA using the LeCroy's software clock recovery. As Figure 5 shows, the amplitude of the TMDS signal is slightly low, but the eye is otherwise acceptable.

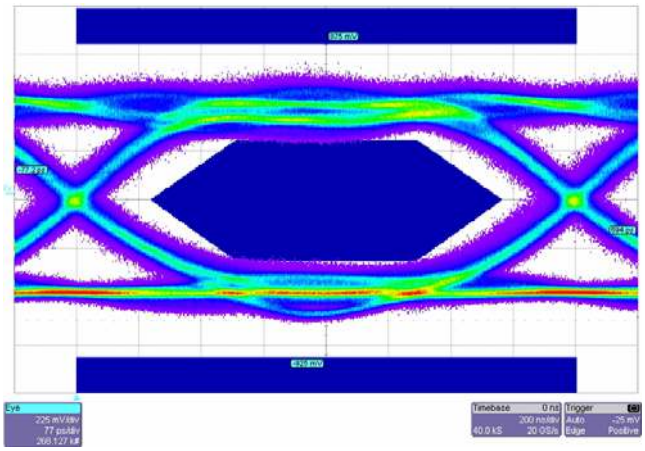


FIGURE 5. EYE DIAGRAM AT OUTPUT OF CHROMA GENERATOR

Next, a 15m DualLink DVI cable was attached and terminated into a female TPA2 adapter and the eye captured in Figure 6.

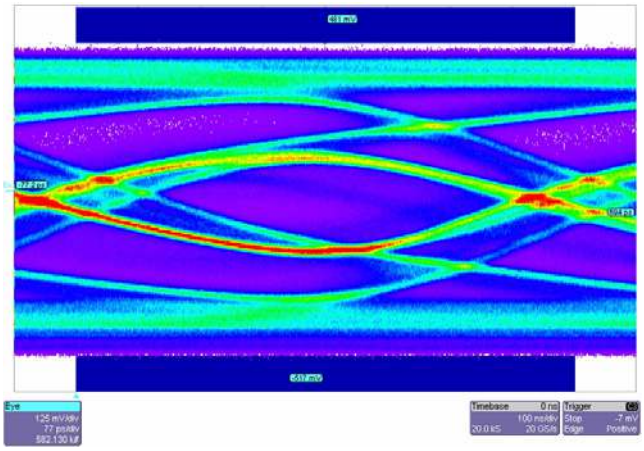


FIGURE 6. CHROMA EYE DIAGRAM AFTER 15m CABLE

The eye is not meeting the minimum requirements of either the HDMI or DVI standards and the Dell Monitor is unable to recover the data and display an image.

Setup B inserts an ISL54100A and an additional 15m cable between the pattern generator and the monitor:

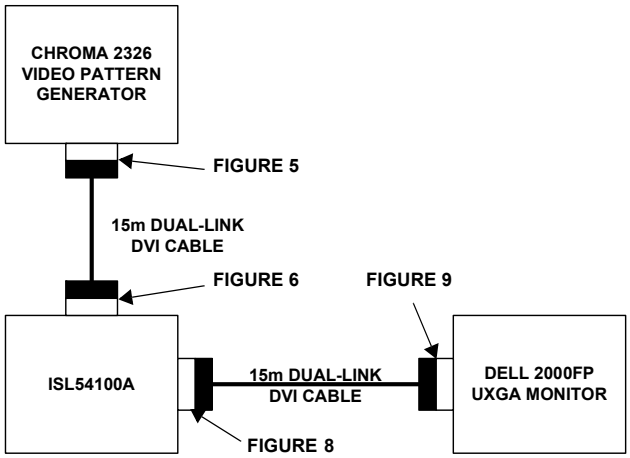


FIGURE 7. TEST SETUP B

Given the input signal shown in Figure 6, the ISL54100A's TMDS output signal (Figure 8) is extremely clean. The output is an improvement over the original signal coming from the pattern generator in both amplitude and jitter.

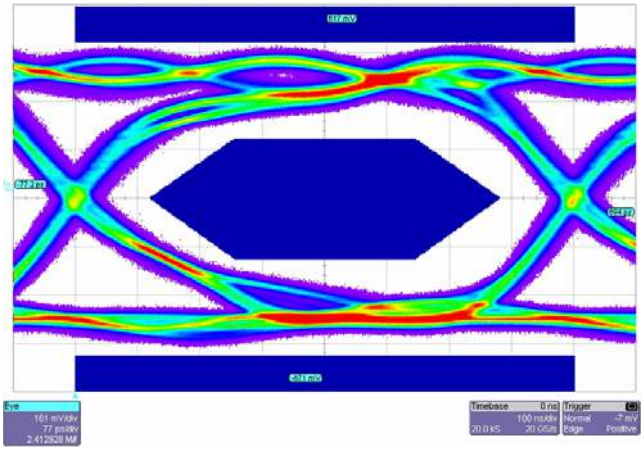


FIGURE 8. EYE DIAGRAM AT OUTPUT OF ISL54100

The cleaner signal generated at the output of the ISL54100A results in an improved eye at the end of another 15m cable (Figure 9). The eye is open enough that the Dell 2000FP can now display a UXGA image with no visible sparkle or other artifacts.

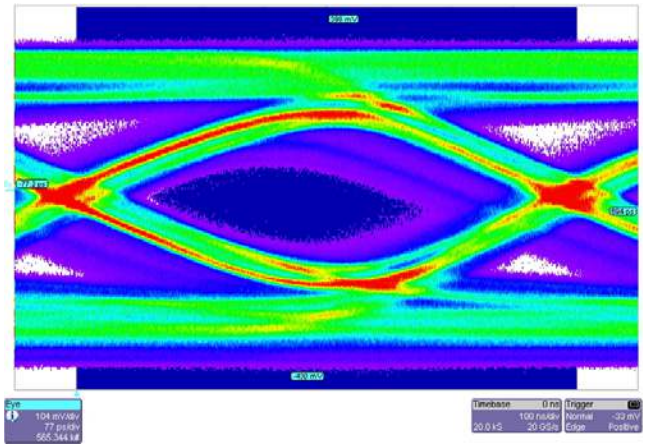


FIGURE 9. ISL54100 EYE DIAGRAM AFTER 15m CABLE

Tx Loading Considerations

When the ISL5410xA is powered-up and its Tx outputs are disabled, via either the PD (power-down) pin, the power-down register bit (register 0x02[5]), or the tri-state outputs bits (register 0x05[1:0]), the Tx pins are high impedance. In this state they will draw no current from the Rx pins of any TMDS receiver they may be connected to.

However if power to the ISL5410xA is removed, the Tx pins are no longer high-impedance. Figure 10 shows the relevant equivalent circuit, including the internal ESD protection diodes. For simplicity, only one of the eight Tx outputs, ESD protection diodes, and Rx termination resistors are shown.

When V_D to the ISL5410xA drops below ~2.7V and power is applied to the external TMDS receiver, ESD protection diodes inside the ISL5410xA can become forward-biased, drawing current from the external TMDS receiver it is attached to.

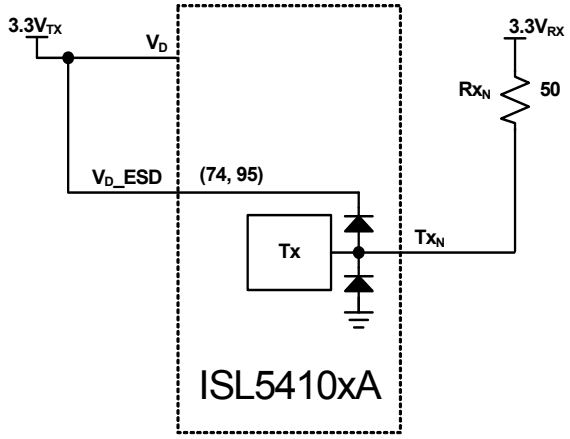


FIGURE 10. ISL5410xA ESD PROTECTION DIODES

This is non-ideal and will cause the ISL5410xA to fail HDMI Compliance Test 7-3 ("V_{OFF}"). V_{OFF} is the voltage across each 50Ω Rx_N resistor when the power is removed from the device containing the ISL5410xA.

To prevent this leakage current, insert a Schottky diode between the V_D power net and the V_D_ESD pins as shown in Figure 11. With the addition of this diode the system will pass compliance test 7-3.

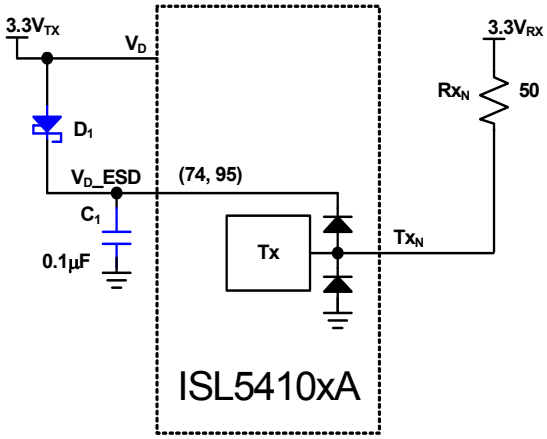


FIGURE 11. SCHOTTKY DIODE MODIFICATION

PCB Layout Recommendations

Because of the high speed of the TMDS signals, careful PCB layout is critical to maximize performance. The following guidelines should be adhered to as closely as possible:

- All TMDS pair traces should have a characteristic impedance of 50Ω with respect to the power/ground planes and 100Ω with respect to each other. Failure to meet this requirement will increase reflections, shrinking the available eye.
- Avoid vias for all 3 high speed TMDS pairs. Vias add inductance which causes a discontinuity in the characteristic impedance of the trace. Keep all the traces on the top (or the bottom) of the PCB. The TMDS clock can have vias if necessary, since it is lower speed and less critical. If you must use a via, ensure the vias are symmetrical (put identical vias in both lines of the differential pair).
- For each TMDS channel, the trace lengths of the 3 TMDS pairs (0, 1 and 2) should ideally be the same to reduce inter channel skew introduced by the board.
- The trace length of the clock pair **is not critical at all.** Since the clock is only used as a frequency reference, its phase/delay is inconsequential. In addition, since the TMDS clock frequency is 1/10th the pixel rate, the clock signal itself is much more noise-immune. So liberties (such as vias and circuitous paths) can be taken when routing the clock lines.
- Minimize capacitance on all TMDS lines. The lower the capacitance, the sharper the rise and fall times.
- Maintain a constant, solid ground (or power) plane under the 3 high speed TMDS signals. Do not route the signals over gaps in the ground plane or over other traces.

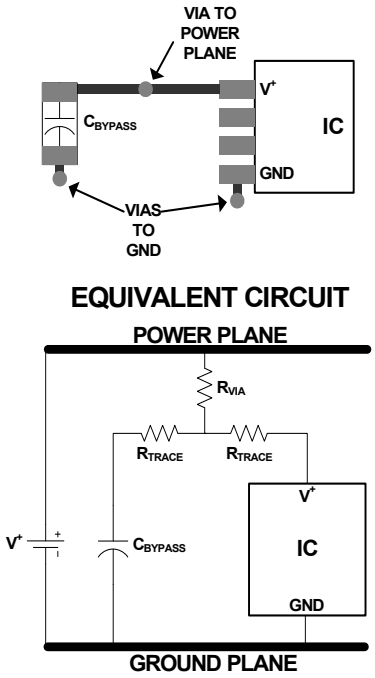


FIGURE 12. SUB-OPTIMAL BYPASS CAPACITOR LAYOUT

- Ideally each supply should be bypassed to ground with a 0.1µF capacitor. Minimize trace length and vias to minimize inductance and maximize noise rejection. Figure 12 demonstrates a common but non-ideal PCB layout and its equivalent circuit. The additional trace resistance between the bypass capacitor and the power supply/IC reduces its effectiveness. Figure 13 demonstrates a better layout. In this case there is still series trace resistance (it is impossible to completely eliminate it), but now it is being put to good use, as part of a “T” filter, attenuating supply noise before it gets to the IC, and reducing the amount of IC-generated noise that gets injected into the supply. Follow the good supply bypassing rules shown in Figure 13 to the extent possible.

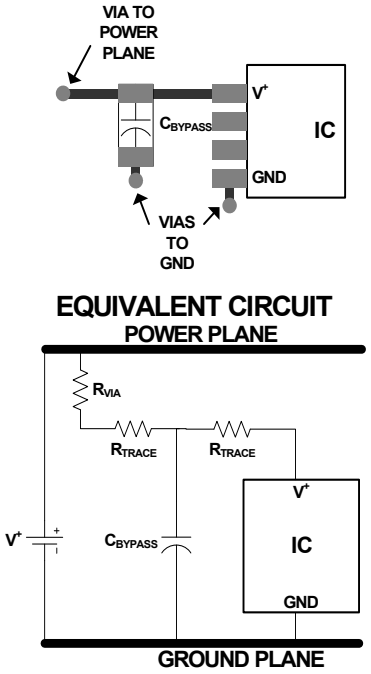


FIGURE 13. OPTIMAL (“T”) BYPASS CAPACITOR LAYOUT

ISL5410xA Serial Communication

Overview

The ISL5410xA uses a 2-wire serial bus for communication with its host. SCL is the Serial Clock line, driven by the host and SDA is the Serial Data line, which can be driven by all devices on the bus. SDA is open drain to allow multiple devices to share the same bus simultaneously.

Communication is accomplished in three steps:

1. The Host selects the ISL5410xA it wishes to communicate with.
2. The Host writes the initial ISL5410xA Configuration Register address it wishes to write to or read from.
3. The Host writes to or reads from the ISL5410xA’s Configuration Register. The ISL5410xA’s internal address pointer auto increments, so to read registers 0x00 through 0x1B, for example, one would write 0x00 in step 2, then repeat step three 28 times, with each read returning the next register value.

The ISL5410xA has a 7-bit address on the serial bus, determined by the ADDR0-ADDR6 bits. This allows up to 128 ISL5410xAs to be independently controlled by the same serial bus.

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high (Figure 14). The ISL5410xA continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. The host then transmits the 7-bit serial address plus a R/$\overline{W}$ bit, indicating if the next transaction will be a Read (R/$\overline{W}$ = 1) or a Write (R/$\overline{W}$ = 0). If the address transmitted matches that of any device on the bus, that device must respond with an ACKNOWLEDGE (Figure 15).

Once the serial address has been transmitted and acknowledged, one or more bytes of information can be written to or read from the slave. Communication with the selected device in the selected direction (read or write) is ended by a STOP command, where SDA rises while SCL is high (Figure 14), or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

Data on the serial bus must be valid for the entire time SCL is high (Figure 16). To achieve this, data being written to the ISL5410xA is latched on a delayed version of the rising edge of SCL. SCL is delayed and deglitched inside the ISL5410xA for three crystal clock periods (120ns for a 25MHz crystal) to eliminate spurious clock pulses that could disrupt serial communication.

When the contents of the ISL5410xA are being read, the SDA line is updated after the falling edge of SCL, delayed and deglitched in the same manner.

Configuration Register Write

Figure 17 shows two views of the steps necessary to write one or more words to the Configuration Register.

Configuration Register Read

Figure 18 shows two views of the steps necessary to read one or more words from the Configuration Register.

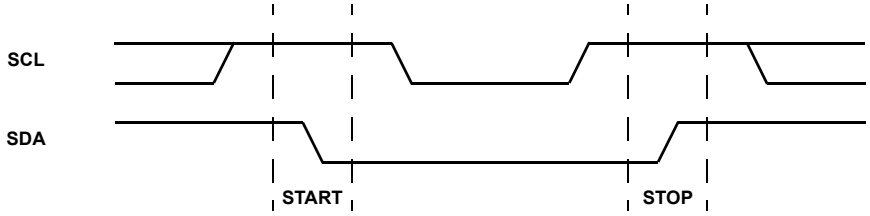


FIGURE 14. VALID START AND STOP CONDITIONS

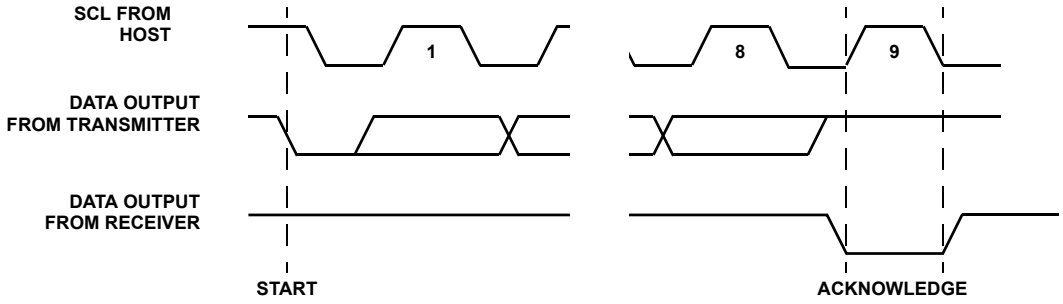


FIGURE 15. ACKNOWLEDGE RESPONSE FROM RECEIVER

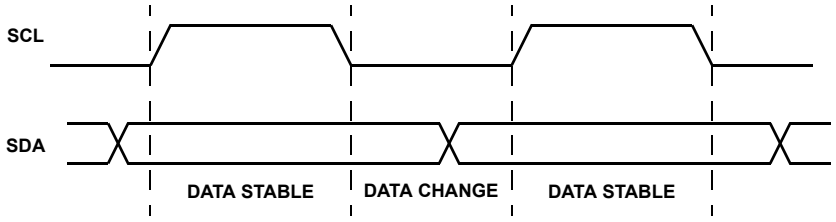
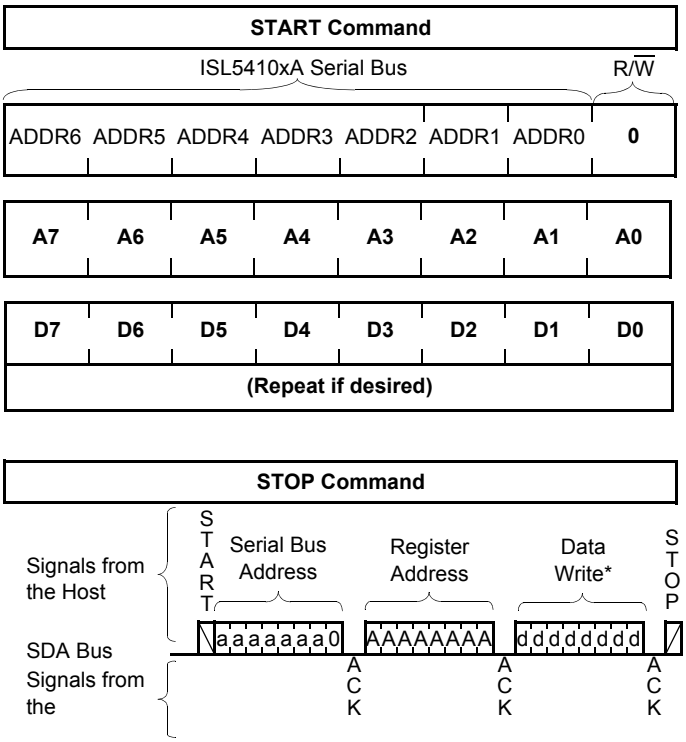


FIGURE 16. VALID DATA CHANGES ON THE SDA BUS



Signals the beginning of serial I/O

ISL5410xA Device Select Address Write

The first 7 bits of the first byte select the ISL5410xA on the 2-wire bus at the address set by the ADDR[6:0} pins. The R/$\overline{W}$ bit is a 0, indicating that the next transaction will be a write.

ISL5410xA Register Address Write

This is the address of the ISL5410xA's configuration register that the following byte will be written to.

ISL5410xA Register Data Write(s)

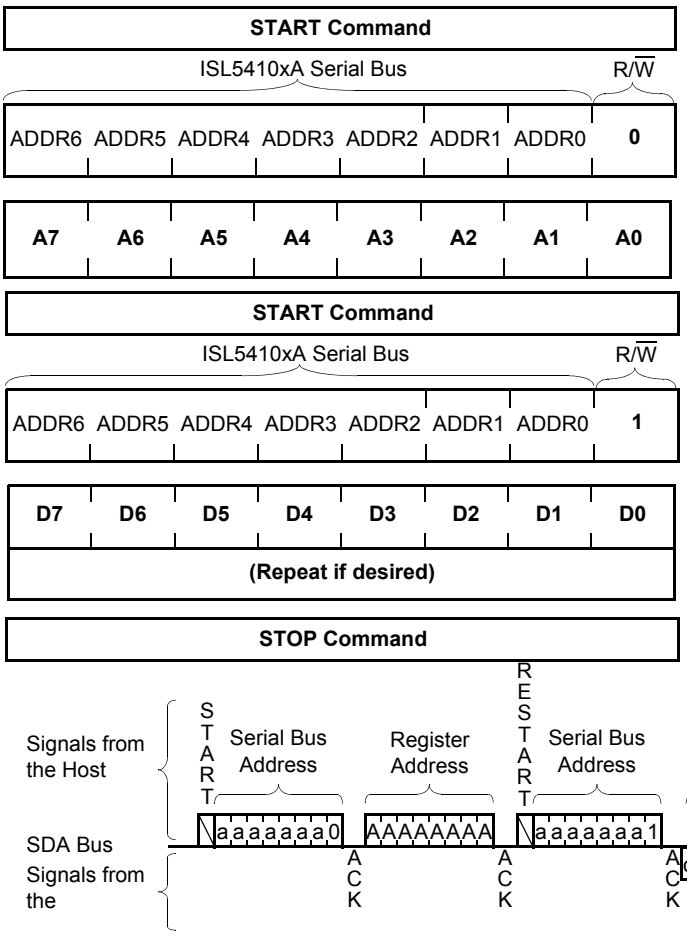
This is the data to be written to the ISL5410xA's configuration register.

Note: The ISL5410xA's Configuration Register's address pointer auto increments after each data write: repeat this step to write

Signals the ending of serial I/O

* The data write step may be repeated to write to the ISL5410xA's Configuration Register sequentially, beginning at the Register Address written in the previous step.

FIGURE 17. CONFIGURATION REGISTER WRITE



Signals the beginning of serial I/O

ISL5410xA Device Select Address Write

The first 7 bits of the first byte select the ISL5410xA on the 2-wire bus at the address set by the ADDR[6:0} pins. R/$\overline{W}$ = 0, indicating that the next transaction will be a write.

ISL5410xA Register Address Write

This sets the initial address of the ISL5410xA's configuration register for subsequent reading.

Ends the previous transaction and starts a new one

ISL5410xA Serial Bus Address Write

This is the same 7-bit address that was sent previously, however the R/$\overline{W}$ bit is now a 1, indicating that the next transaction(s) will be a read.

ISL5410xA Register Data Read(s)

This is the data read from the ISL5410xA's configuration register.

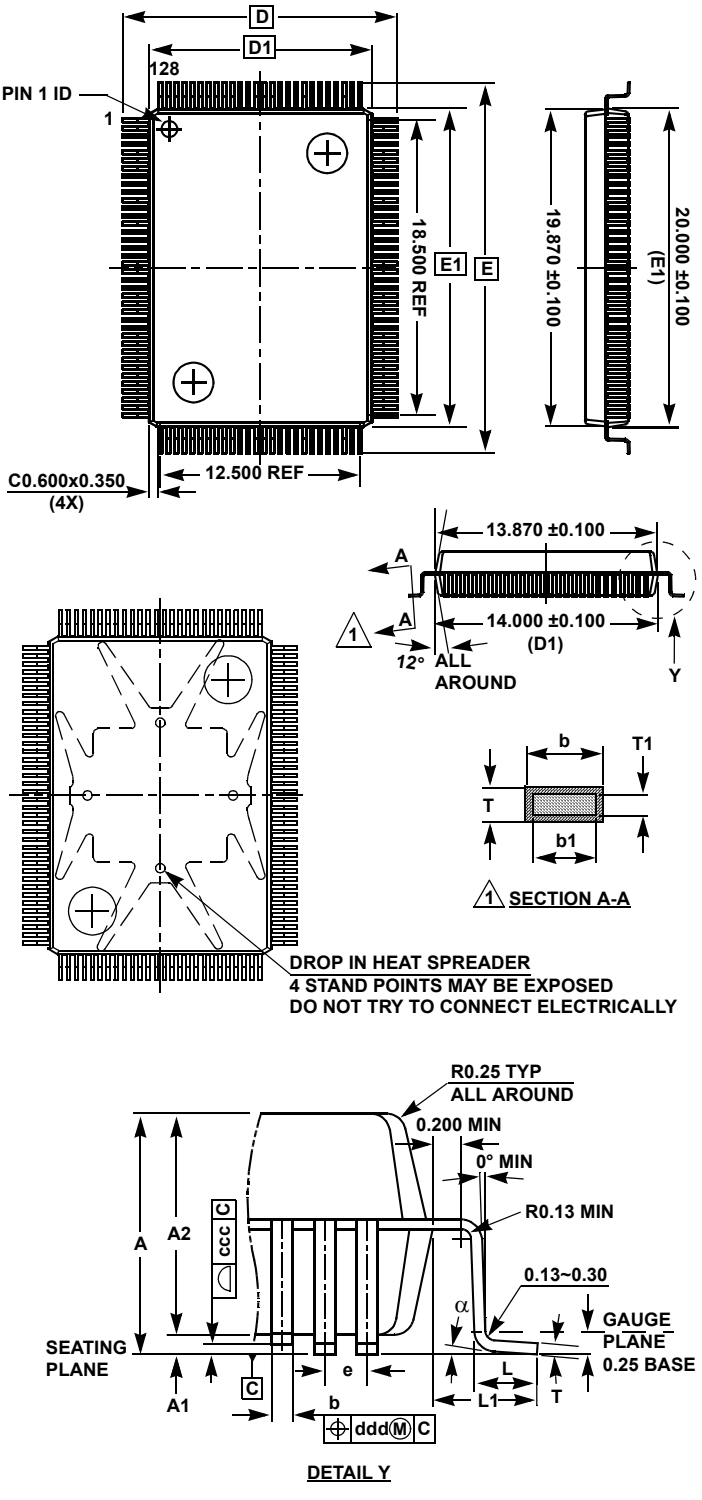
Note: The ISL5410xA's Configuration Register's address pointer auto increments after each data read: repeat this step to read multiple sequential bytes of data from the Configuration Register.

Signals the ending of serial I/O

* The data read step may be repeated to read from the ISL5410xA's Configuration Register sequentially, beginning at the Register Address written in the two steps previous.

FIGURE 18. CONFIGURATION REGISTER READ

Metric Plastic Quad Flatpack Packages (MQFP)



MDP0055

14x20mm 128 LEAD MQFP (WITH AND WITHOUT HEAT SPREADER) 3.2mm FOOTPRINT

SYMBOL	DIMENSIONS (MILLIMETERS)	REMARKS
A	Max 3.40	Overall height
A1	0.250~0.500	Standoff
A2	2.750 ±0.250	Package thickness
α	0°~7°	Foot angle
b	0.220 ±0.050	Lead width (1)
b1	0.200 ±0.030	Lead base metal width (1)
D	17.200 ±0.250	Lead tip to tip
D1	14.000 ±0.100	Package length
E	23.200 ±0.250	Lead tip to tip
E1	20.000 ±0.100	Package width
e	0.500 Base	Lead pitch
L	0.880 ±0.150	Foot length
L1	1.600 Ref.	Lead length
T	0.170 ±0.060	Frame thickness (1)
T1	0.152 ±0.040	Frame base metal thickness (1)
ccc	0.100	Foot coplanarity
ddd	0.100	Foot position

Rev. 2 2/07

NOTES:

1. General tolerance: Distance ±0.100, Angle +2.5°.
2. (1) Matte finish on package body surface except ejection and pin 1 marking (Ra 0.8~2.0um).
3. All molded body sharp corner RADII unless otherwise specified (Max RO.200).
4. Package/Leadframe misalignment (X, Y): Max. 0.127
5. Top/Bottom misalignment (X, Y): Max. 0.127
6. Drawing does not include plastic or metal protrusion or cutting burr.
7. (2) Compliant to JEDEC MS-022.