FUNCTION TABLE
(each latch)

INPUTS		OUTPUTS	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

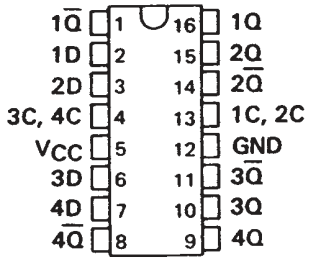
description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

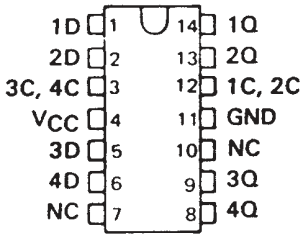
The '75 and 'LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77 and 'LS77 4-bit latches are available in 14-pin flat packages.

These circuits are completely compatible with all popular TTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54 and 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, and 74LS devices are characterized for operation from 0°C to 70°C.

SN5475, SN54LS75 . . . J OR W PACKAGE
SN7475 . . . N PACKAGE
SN74LS75 . . . D OR N PACKAGE
(TOP VIEW)



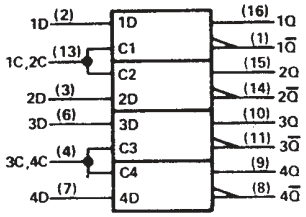
SN5477, SN54LS77 . . . W PACKAGE
(TOP VIEW)



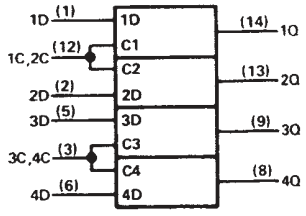
NC - No internal connection

logic symbols†

'75, 'LS75



'77, 'LS77



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

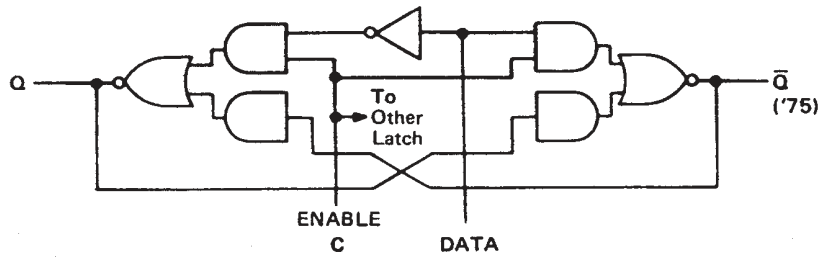
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage: '75, '77 . . . . . 5.5 V
'LS75, 'LS77 . . . . . 7 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0° C to 70°C
Storage temperature range . . . . . −65°C to 150°C

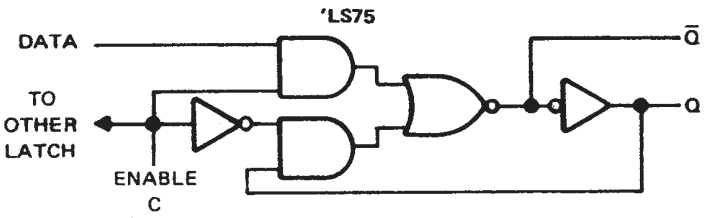
NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.

logic diagrams (each latch) (positive logic)

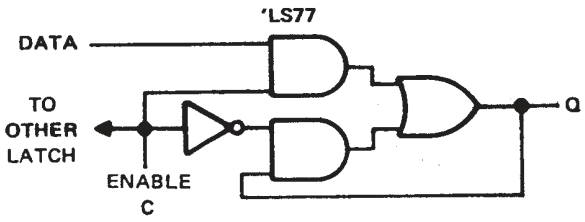
'75, '77



'LS75



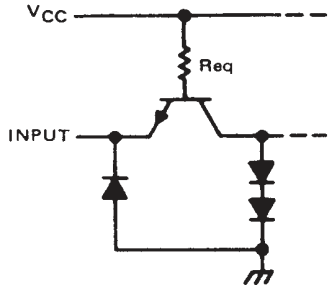
'LS77



schematics of inputs and outputs

'75, '77

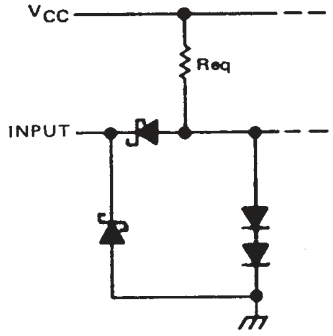
EQUIVALENT OF EACH INPUT



Data: R_{eq} = 2 kΩ NOM
Enable: R_{eq} = 1 kΩ NOM

'LS75, 'LS77

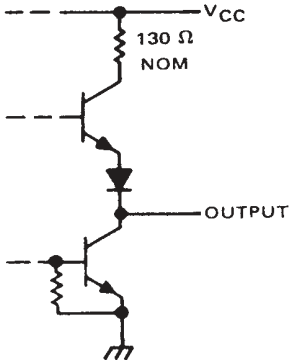
EQUIVALENT OF EACH INPUT



Data: R_{eq} = 17 kΩ
Enable: R_{eq} = 4.2 kΩ

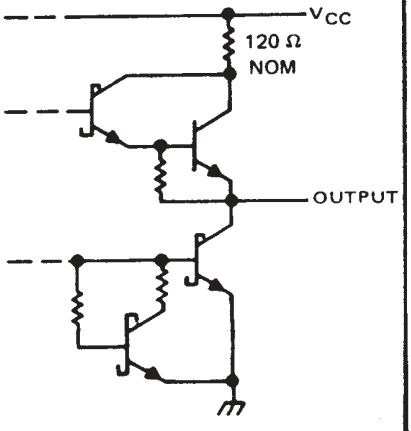
'75, '77

TYPICAL OF ALL OUTPUTS



'LS75, 'LS77

TYPICAL OF ALL OUTPUTS



recommended operating conditions

	SN5475, SN5477			SN7475			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μA
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = –12 mA				–1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	D input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		C input					160	
I_{IL}	Low-level input current	D input	V_{CC} = MAX, V_I = 0.4 V				–3.2	mA
		C input					–6.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54′	–20		–57	mA
				SN74′	–18		–57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	SN54′		32	46	mA
				SN74′		32	53	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1		16	30	ns
t_{PHL}					14	25	
t_{PLH}¶	D	$\overline{Q}$			24	40	ns
t_{PHL}¶					7	15	
t_{PLH}	C	Q			16	30	ns
t_{PHL}					7	15	
t_{PLH}¶	C	$\overline{Q}$			16	30	ns
t_{PHL}¶					7	15	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
¶These parameters are not applicable for the SN5477.

recommended operating conditions

	SN54LS75 SN54LS77			SN74LS75			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS75 SN54LS77			SN74LS75			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	D input			0.1			0.1	mA
				C input			0.4			0.4	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	D input			20			20	μA
				C input			80			80	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	D input			−0.4			−0.4	mA
				C input			−1.6			−1.6	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	'LS75		6.3	12		6.3	12	mA
				'LS77		6.9	13				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

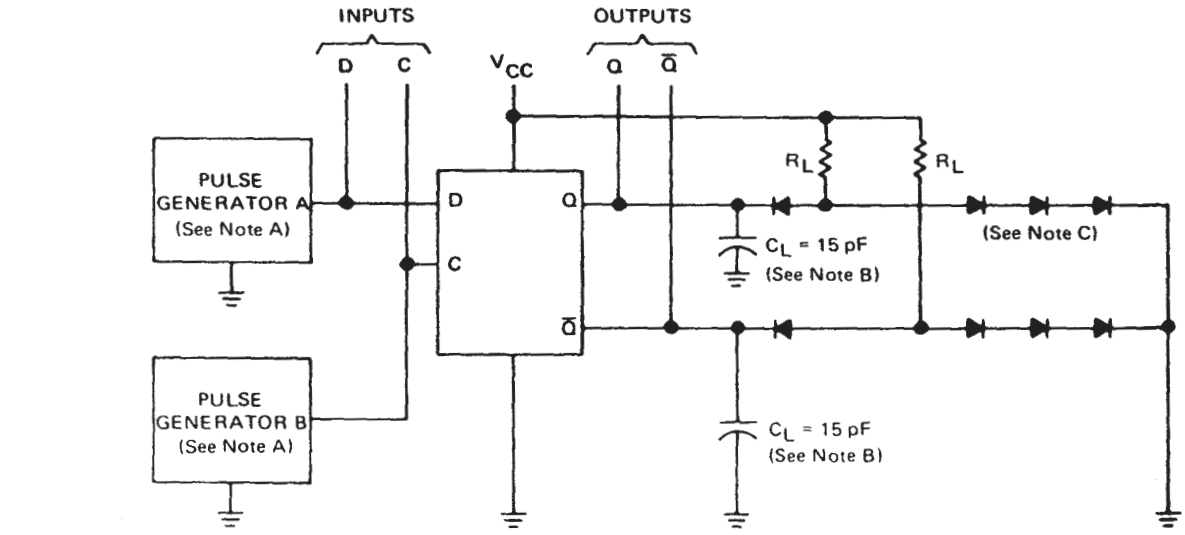
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS75			'LS77			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D	Q	C_L = 15 pF, R_L = 2 kΩ, See Figure 1		15	27		11	19	ns
t_{PHL}					9	17		9	17	
t_{PLH}	D	$\bar{Q}$			12	20				ns
t_{PHL}					7	15				
t_{PLH}	C	Q			15	27		10	18	ns
t_{PHL}					14	25		10	18	
t_{PLH}	C	$\bar{Q}$			16	30				ns
t_{PHL}					7	15				

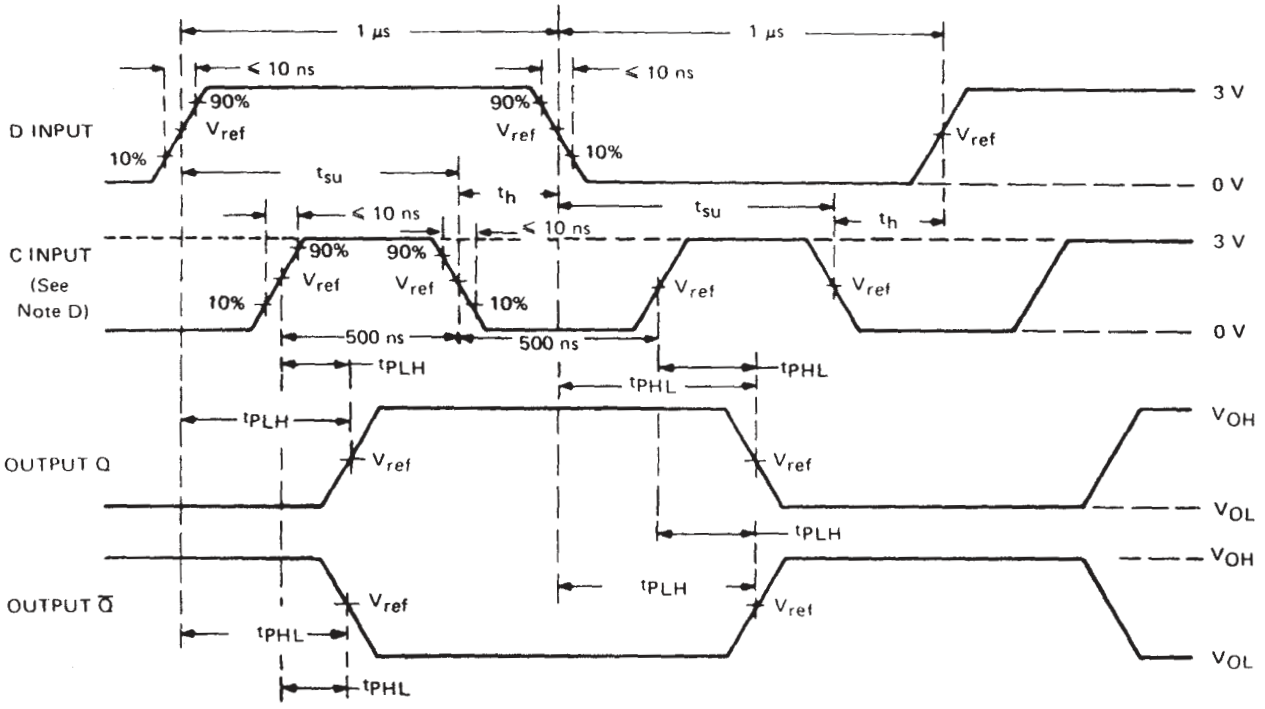
¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PLH} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

switching characteristics†



TEST CIRCUIT



VOLTAGE WAVEFORMS

†Complementary Q outputs are on the '75 and 'LS75 only.

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for pulse generator A, PRR ≤ 500 kHz; for pulse generator B, PRR ≤ 1 MHz. Positions of D and C input pulses are varied with respect to each other to verify setup times.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

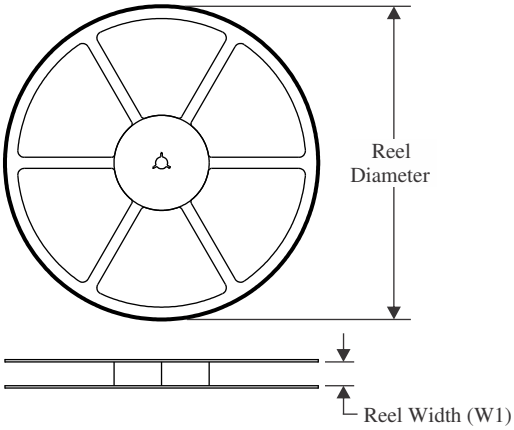
D. When measuring propagation delay times from the D input, the corresponding C input must be held high.

E. For '75 and '77, V_{ref} = 1.5 V; for 'LS75 and 'LS77, V_{ref} = 1.3 V.

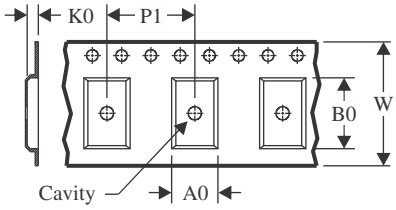
FIGURE 1

TAPE AND REEL INFORMATION

REEL DIMENSIONS

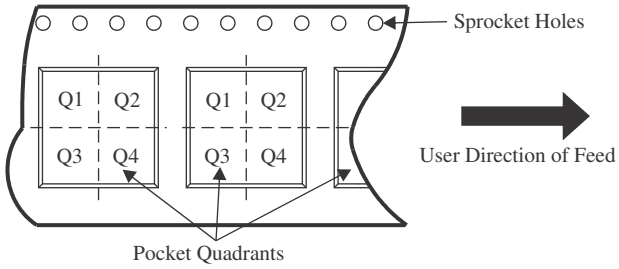


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

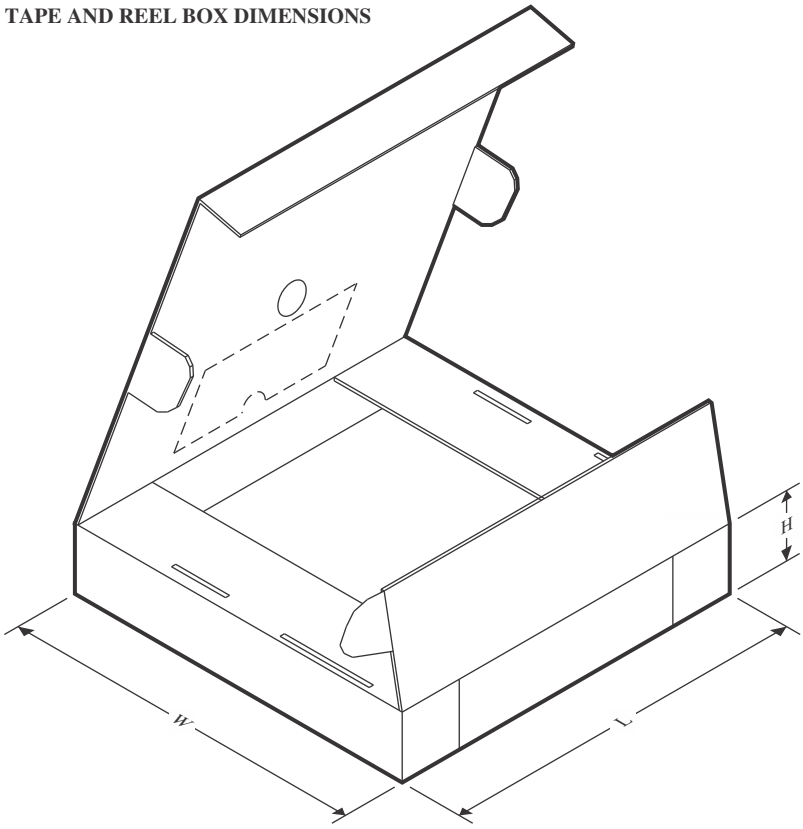
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS75DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS75NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

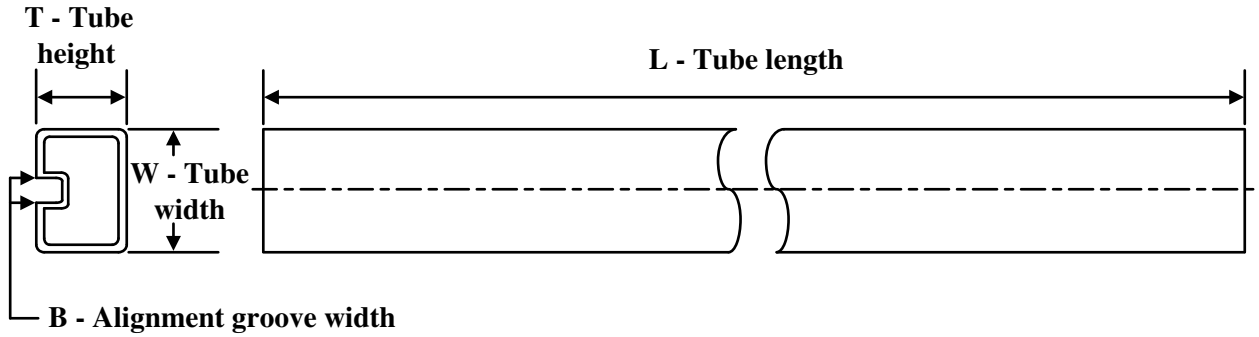
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS75DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS75NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
7601201FA	W	CFP	16	1	506.98	26.16	6220	NA
SN74LS75D	D	SOIC	16	40	507	8	3940	4.32
SN74LS75N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS75N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS75W	W	CFP	16	1	506.98	26.16	6220	NA

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