



# BUK9V13-40H

Dual N-channel 40 V, 13 mOhm logic level MOSFET in LFPAK56D (half-bridge configuration)

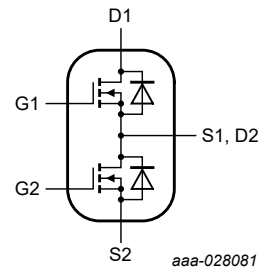
9 May 2023

Product data sheet

## 1. General description

Dual, logic level N-channel MOSFET in an LFPAK56D package (half-bridge configuration), using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101.

An internal connection is made between the source (S1) of the high-side FET to the drain (D2) of the low-side FET, making the device ideal to use as a half-bridge switch in high-performance automotive PWM applications.



## 2. Features and benefits

- LFPAK56D package with half-bridge configuration enables:
  - Reduced PCB layout complexity
  - PCB shrinkage through reduced component footprint for 3-phase motor drive
  - Improved system level  $R_{th(j-amb)}$  due to optimized package design
  - Lower parasitic inductance to support higher efficiency
  - Footprint compatibility with LFPAK56D Dual package
- Advanced AEC-Q101 grade Trench 9 silicon technology:
  - Low power losses, high power density
  - Superior avalanche performance
  - Repetitive avalanche rated
- LFPAK copper clip packaging provides high robustness and reliability
- Gull wing leads support high manufacturability and Automated Optical Inspection (AOI)

## 3. Applications

- 12 V automotive systems
- Powertrain, chassis, body and infotainment applications
- Brushless or brushed DC motor drive
- DC-to-DC systems
- LED lighting

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Limiting values FET1 and FET2</b>						
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	[1]	-	42	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	46	W

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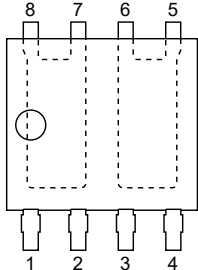
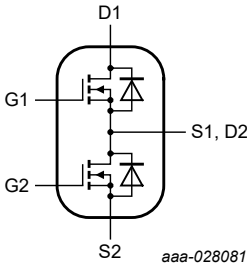
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	7.9	11.35	13.6	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 10\text{ A}$ ; $V_{DS} = 32\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	2.1	4.2	nC
<b>Source-drain diode FET1 and FET2</b>						
$Q_r$	recovered charge	$I_S = 10\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; <a href="#">[2]</a> ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ °C}$	-	16.2	-	nC

[1] 42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] includes capacitive recovery

## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S2	source2	 <p><b>LFPAK56D; Dual LFPAK (SOT1205)</b></p>	 <p>aaa-028081</p>
2	G2	gate2		
3	S1, D2	source1, drain2		
4	G1	gate1		
5	D1	drain1		
6	D1	drain1		
7	S1, D2	source1, drain2		
8	S1, D2	source1, drain2		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK9V13-40H	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
BUK9V13-40H	9V1340H

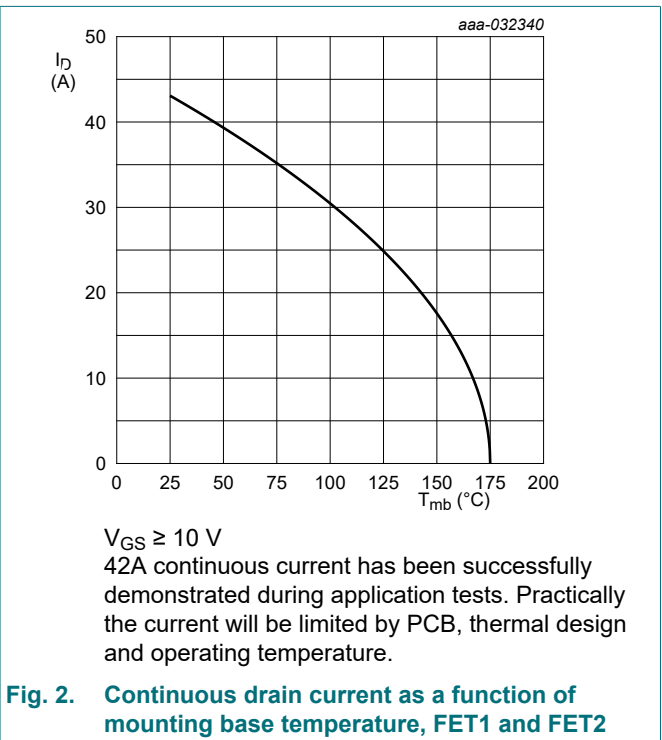
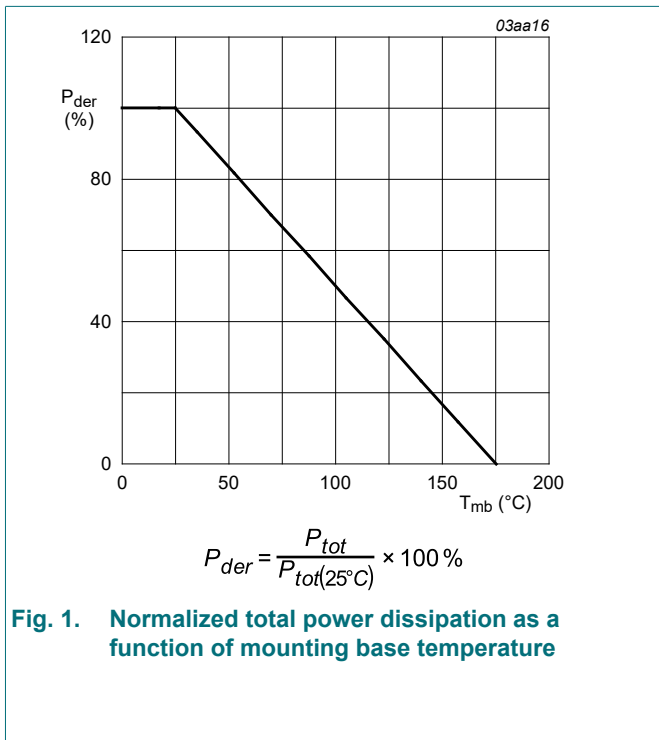
## 8. Limiting values

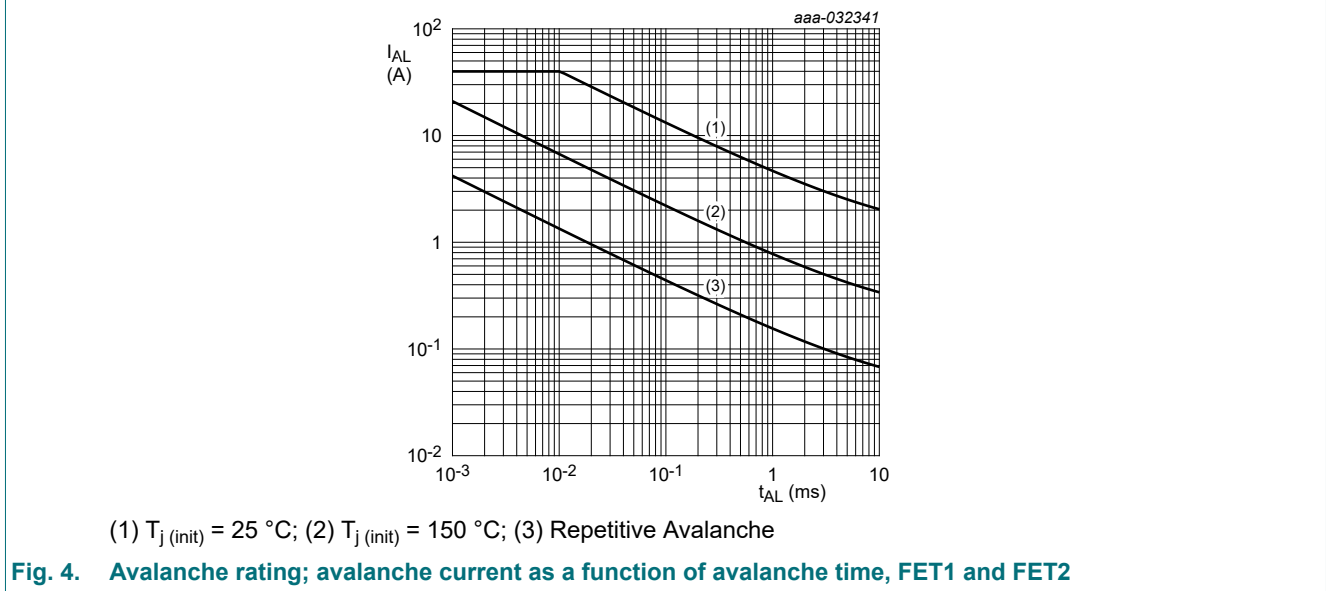
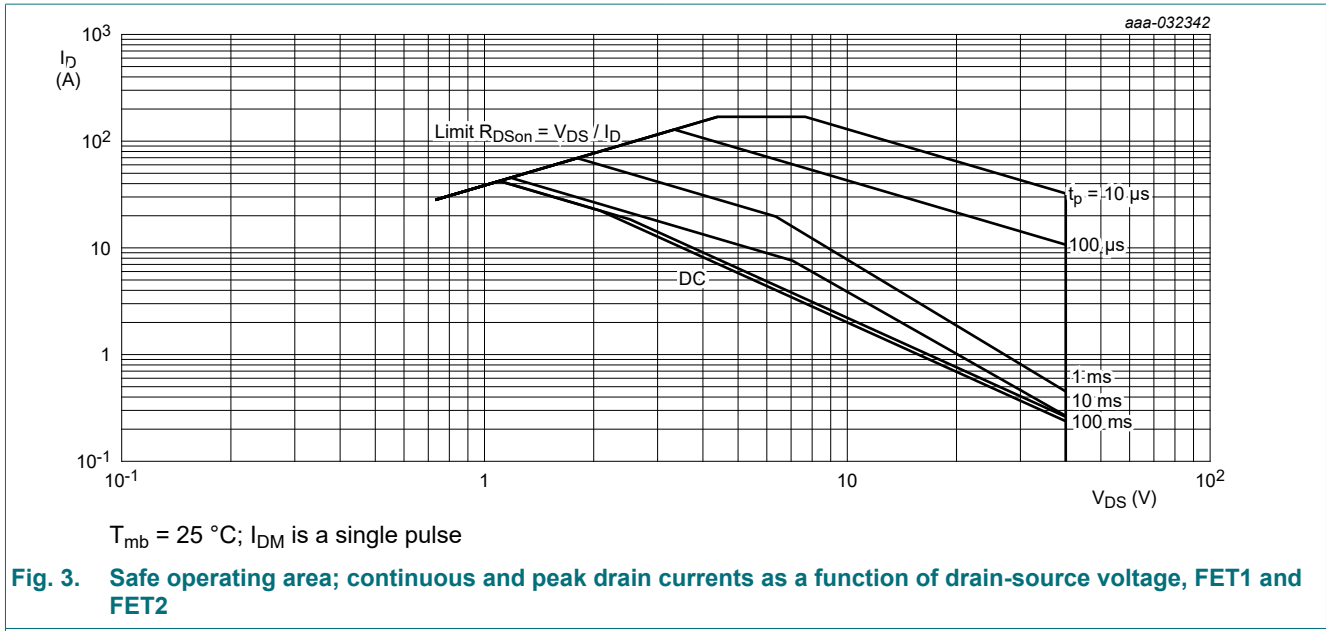
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Limiting values FET1 and FET2</b>						
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V
V <sub>GS</sub>	gate-source voltage	DC; T <sub>j</sub> = 25 °C		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1		-	46	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2	[1]	-	42	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2		-	30	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3		-	169	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode FET1 and FET2</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	42	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	169	A
<b>Avalanche ruggedness FET1 and FET2</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 39.9 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; Fig. 4	[2] [3]	-	10.6	mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> = 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω; Fig. 4	[4]	-	39.9	A

- [1] 42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Protected by 100% test





## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	3	3.23	K/W

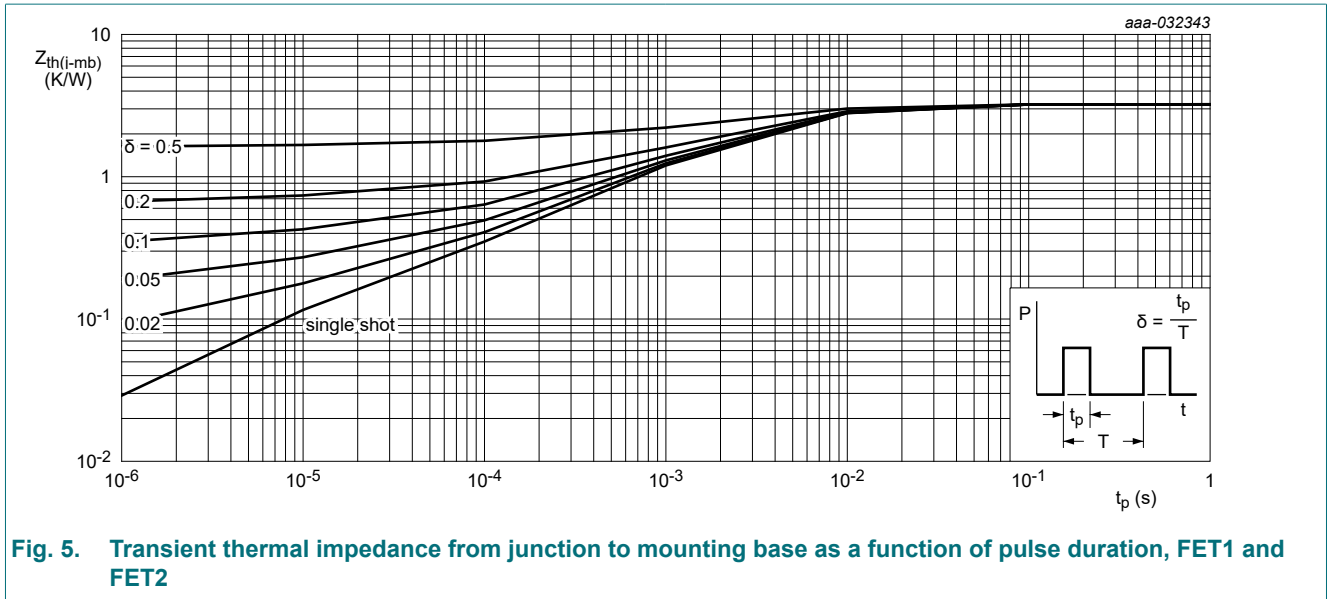


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	40.5	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9; Fig. 10}$	1.5	1.85	2.2	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 10}$	0.7	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 10}$	-	-	2.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	5	$\mu A$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	0.14	10	$\mu A$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	26	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

## Dual N-channel 40 V, 13 mOhm logic level MOSFET in LPAK56D (half-bridge configuration)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>	7.9	11.35	13.6	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 105 °C; <a href="#">Fig. 12</a>	10.9	16.87	20.4	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 125 °C; <a href="#">Fig. 12</a>	12	18.2	21.9	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a>	14.5	21.97	26.4	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>	9.8	14.04	16.9	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 105 °C; <a href="#">Fig. 12</a>	13.5	20.6	25.4	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 125 °C; <a href="#">Fig. 12</a>	14.8	22.24	27.2	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a>	18	26.65	32.8	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	0.7	1.7	4.2	Ω
<b>Dynamic characteristics FET1 and FET2</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	13.9	19.4	nC
		I <sub>D</sub> = 10 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	7.3	10.2	nC
Q <sub>GS</sub>	gate-source charge		-	2.5	3.8	nC
Q <sub>GD</sub>	gate-drain charge		-	2.1	4.2	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>	-	829	1160	pF
C <sub>oss</sub>	output capacitance		-	280	420	pF
C <sub>rss</sub>	reverse transfer capacitance		-	38	84	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 3 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C	-	5.6	-	ns
t <sub>r</sub>	rise time		-	8.1	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	9.1	-	ns
t <sub>f</sub>	fall time		-	6.5	-	ns
<b>Source-drain diode FET1 and FET2</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>	-	0.84	1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V;	-	21.5	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C	[1]	16.2	-	nC

[1] includes capacitive recovery

Dual N-channel 40 V, 13 mOhm logic level MOSFET in LPAK56D (half-bridge configuration)

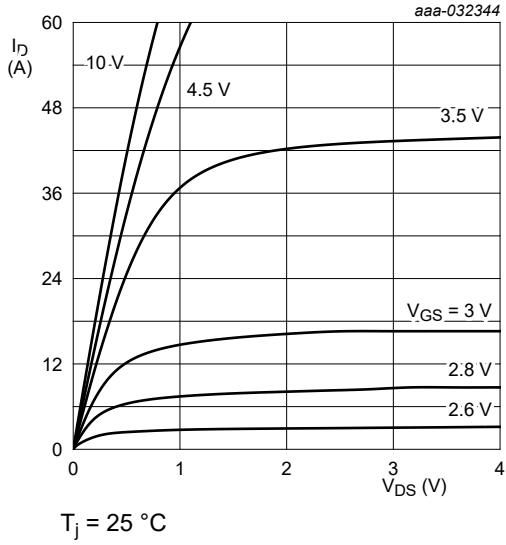


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2

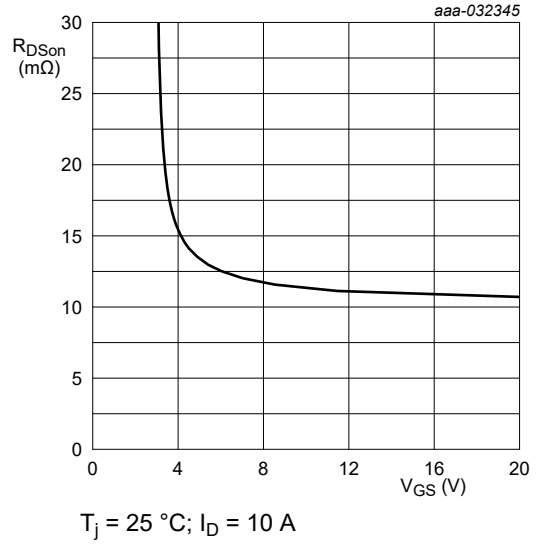


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2

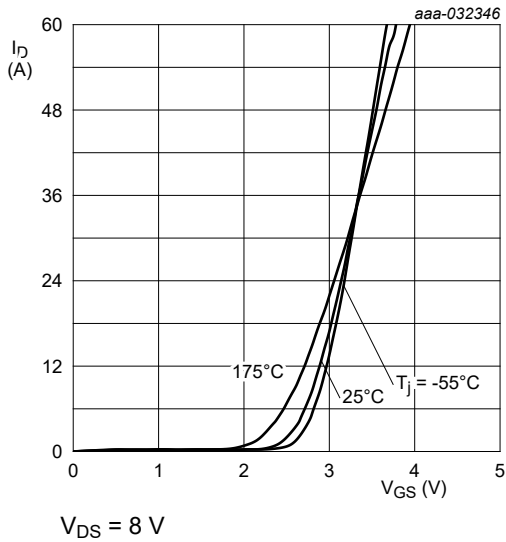


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

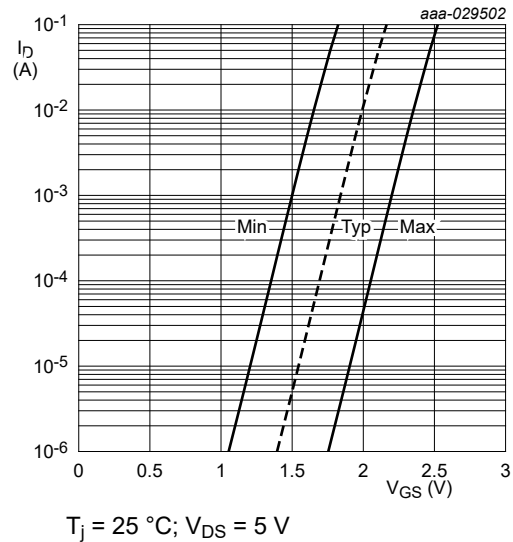


Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

Dual N-channel 40 V, 13 mOhm logic level MOSFET in LPAK56D (half-bridge configuration)

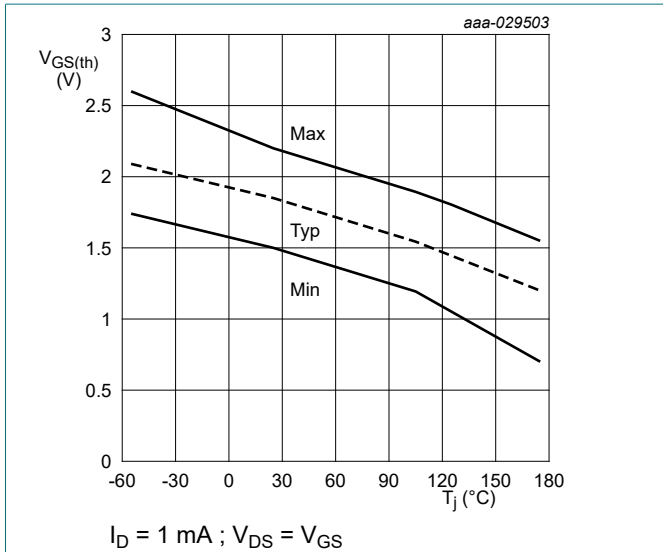


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

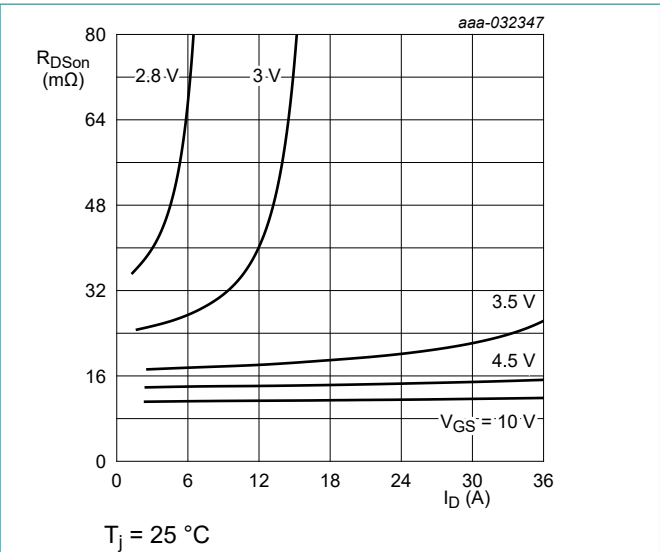


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

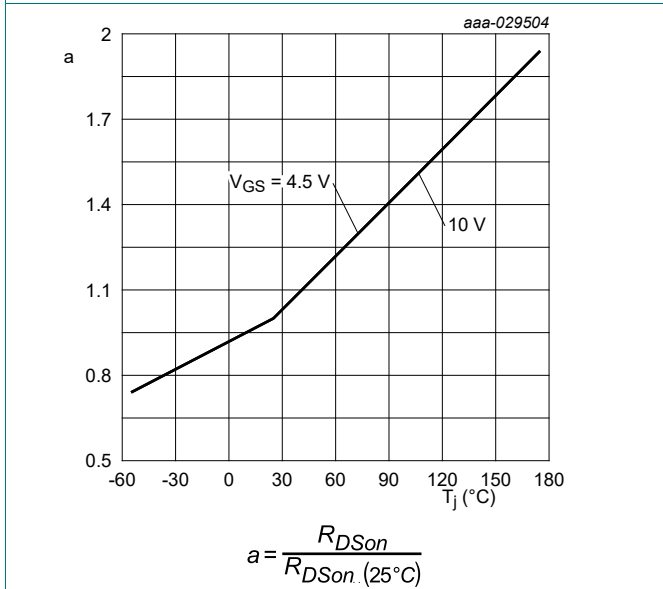


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

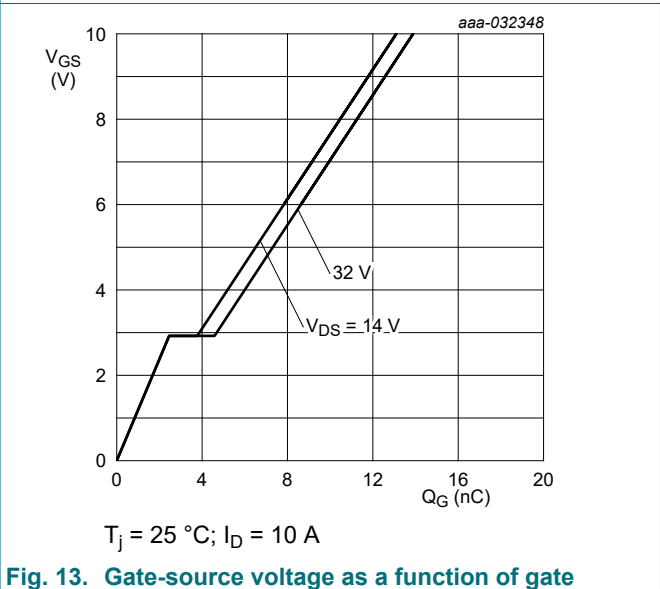


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2



Dual N-channel 40 V, 13 mOhm logic level MOSFET in LPAK56D (half-bridge configuration)

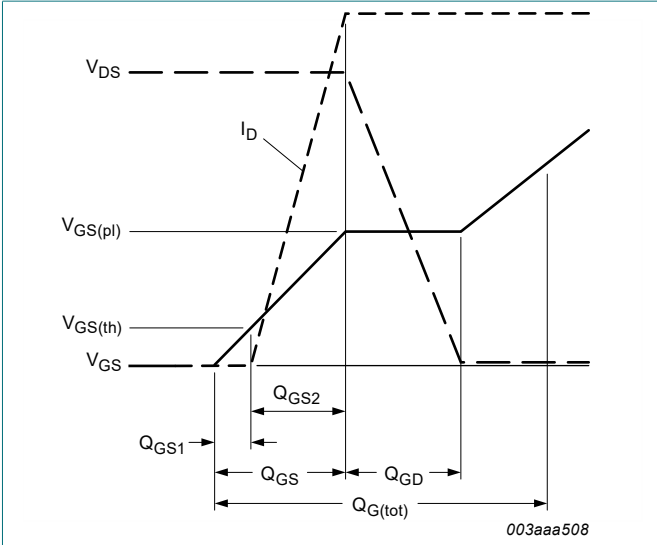


Fig. 14. Gate charge waveform definitions

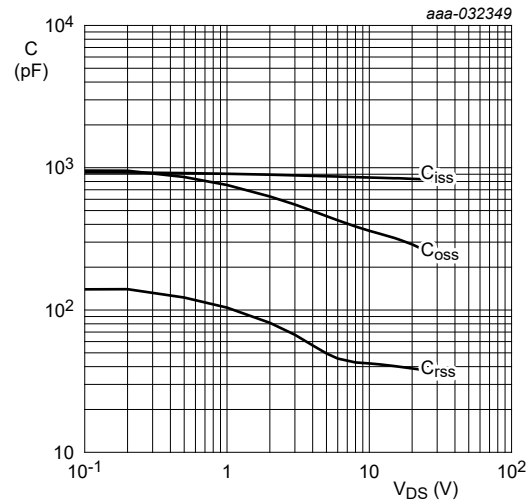
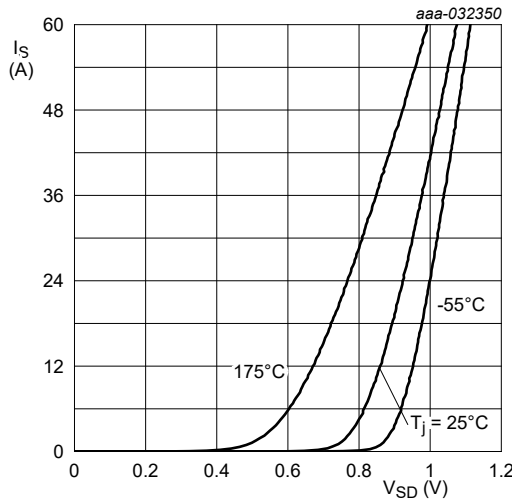


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



$V_{GS} = 0\text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

11. Package outline

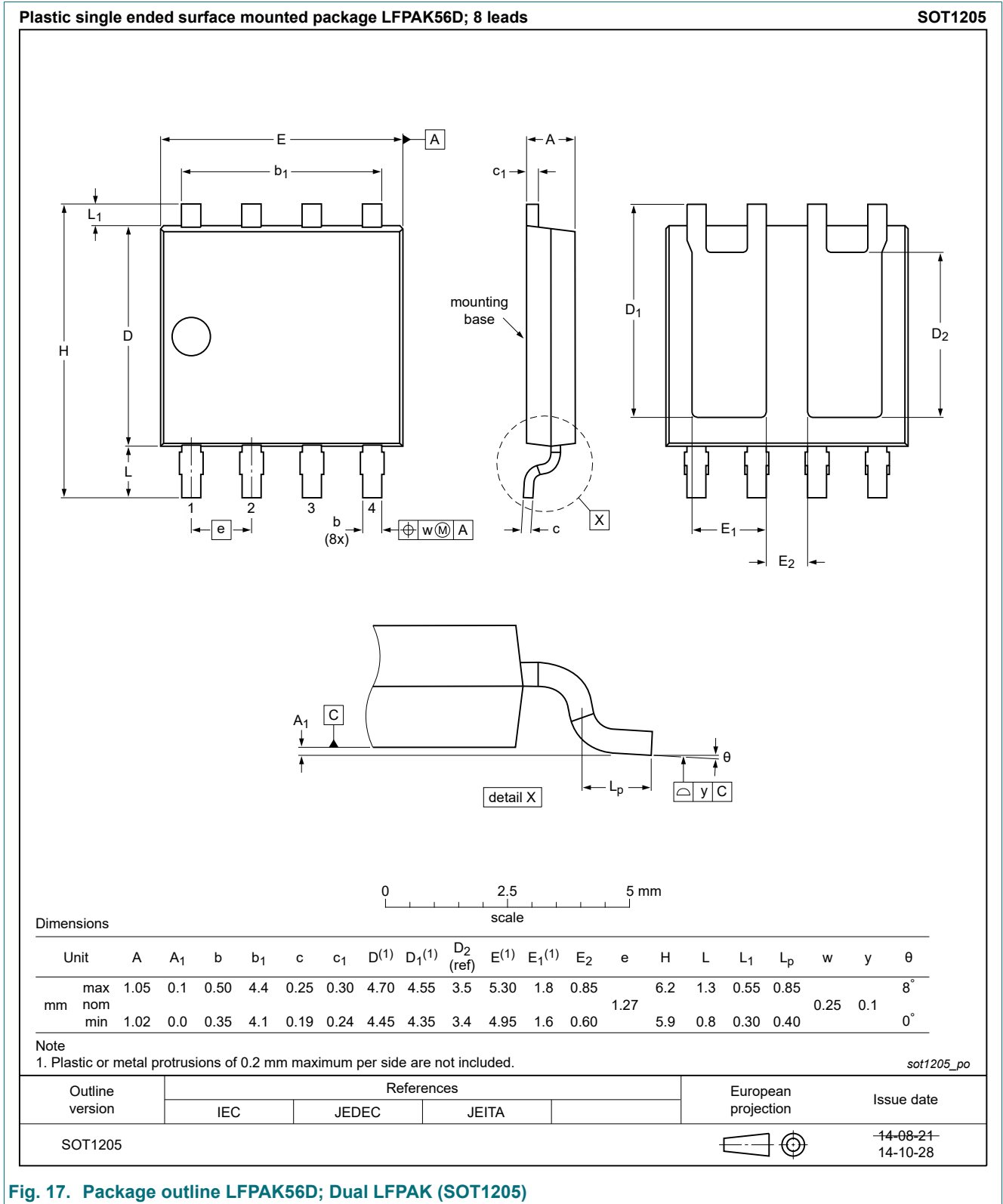


Fig. 17. Package outline LPAK56D; Dual LPAK (SOT1205)

## 12. Soldering

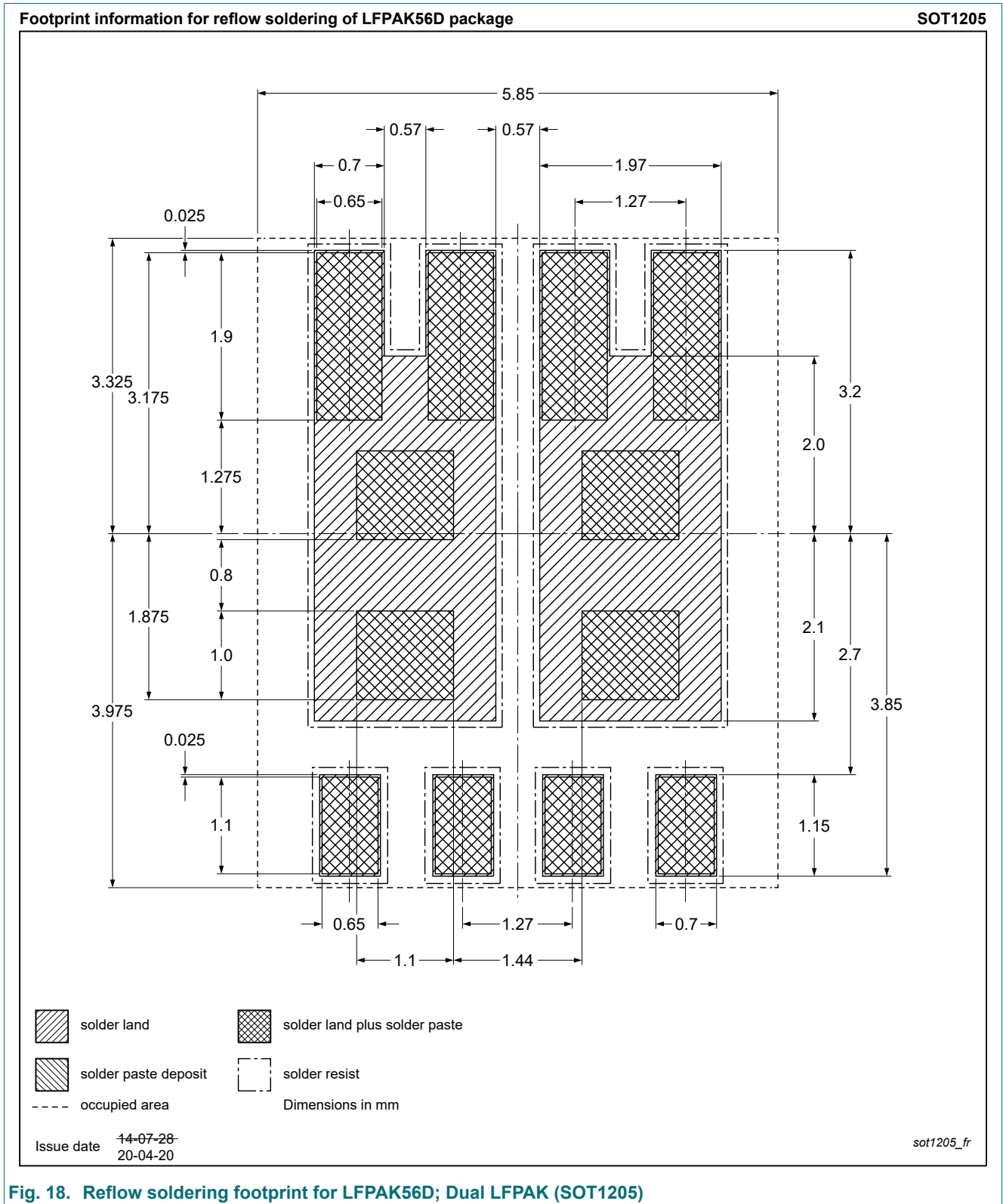


Fig. 18. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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