

This document describes how to implement a NEEK upgrade package with Cyclone III FPGA starter board to a Nios II Embedded Evaluation Kit.

Step 1. Screw 4 female standoffs on the back side of the Cyclone III FPGA starter board, as shown in Figure 1.

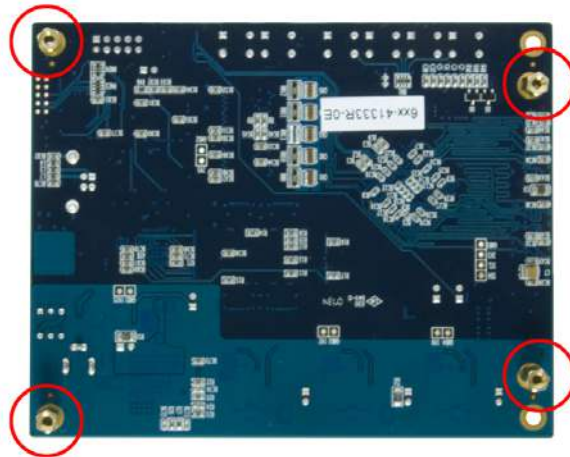


Figure 1. The back side view of the Cyclone III FPGA starter board after 4 female standoffs are screwed in position.

Step 2. Connect HSMC interface of Terasic Multimedia Touch Panel daughter board (MTDB) and Cyclone III FPGA starter board with each other, as shown in figure 2.

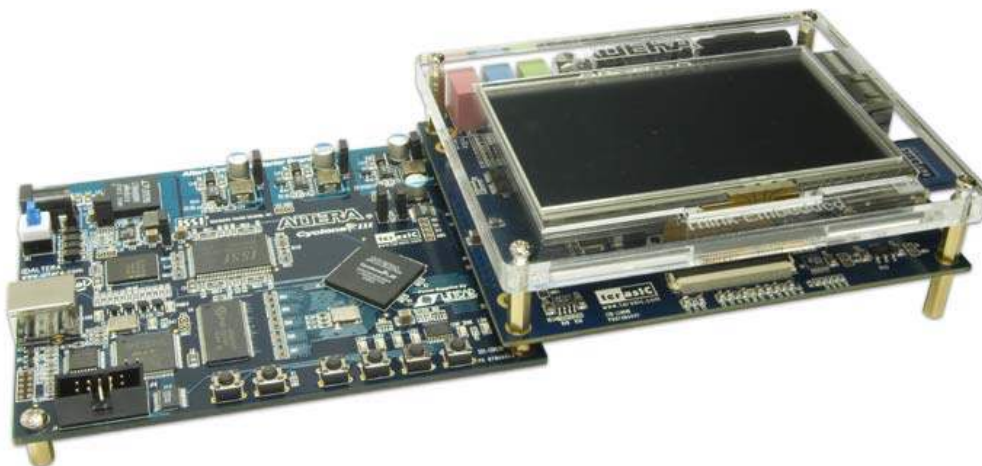


Figure 2. Connection of a MTDB Board and a Cyclone III Starter Board.

Step 3. Install the design software:

1. Install the following software from the accompanying DVD or from the Altera web page:

www.altera.com/download Install ALL of the following:

- Quartus II software version 8.0 or later
- Nios II EDS, version 8.0 or later
- Altera MegaCore® IP Library, version 8.0

2. Obtain a license file.

3. Install USB Blaster driver software.

4. Install tutorials and examples from the Nios II evaluation kit CD-ROM

By default these files will be installed to:

/altera/80/kits/cycloneIII_3c25_niosII_eval

Step 4. Build the factory image in the flash on the Cyclone III FPGA starter board:

To build the factory image, perform the following steps:

1. Plug the supplied 12-V DC power supply into an AC power outlet (100 V-240 V), and then connect this power supply to the development board.

2. Make sure the Quartus II and NIOS II software are installed in your PC.

2. Connect the development board to your computer using the supplied USB cable.

3. Turn on the development board power by pressing the red power switch.

4. Copy the Factory Image File from the directory named "Factory_Image" in the MTDB SYSTEM CD or from the Link : http://www.terasic.com/downloads/cd-rom/mtdb/Factory_Image.zip

5. Execute "My_FlashProgrammer.bat". A NIOS II EDS window will pop up and start to erase the flash and program the factory image file into flash as shown in Figure 3.

6. Figure 4 shows the factory image file has been programmed into flash.

7. Insert the SD card into the SD card slot on the MTDB board. You should now be able to reset the board to start the Application Selector.

```
Nios II EDS 8.0
Info: Ended Programmer operation at Mon Apr 27 10:16:20 2009
Info: Quartus II Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 62 megabytes
Info: Processing ended: Mon Apr 27 10:16:20 2009
Info: Elapsed time: 00:00:02
Info: Total CPU time (on all processors): 00:00:00

Welcome To Altera SOPC Builder

Version 8.0, Built Mon Jul 7 23:59:28 PDT 2008

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Welcome to the Nios II Embedded Design Suite
Version 9.0, Built Thu Feb 26 04:34:00 PST 2009

Example designs can be found in
/cygdrive/c/altera/90/nios2eds/examples

<You may add a startup script: c:/altera/90/nios2eds/user.bashrc>
Using cable "USB-Blaster [USB-0]", device 1, instance 0x00
Resetting and pausing target processor: OK
Checksums took 1.7s
00080000 <22%>: Erasing
```

Figure 3. Erasing the flash

```
Nios II EDS 8.0

Welcome to the Nios II Embedded Design Suite
Version 9.0, Built Thu Feb 26 04:34:00 PST 2009

Example designs can be found in
/cygdrive/c/altera/90/nios2eds/examples

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<You may add a startup script: c:/altera/90/nios2eds/user.bashrc>
Using cable "USB-Blaster [USB-0]", device 1, instance 0x00
Resetting and pausing target processor: OK
Checksums took 1.7s
Erased 1824kB in 17.3s <105.4kB/s>
Device contents checksummed OK
Leaving target processor paused
Using cable "USB-Blaster [USB-0]", device 1, instance 0x00
Resetting and pausing target processor: OK
Checksums took 0.4s
Erase not required
Programmed 1743KB in 87.6s <19.8KB/s>
Device contents checksummed OK
Leaving target processor paused
```

Figure 4. Programming the Factory Image file has been finished



Figure 5. View of the Application Selector User Interface