

NAU82011VG 3.1W Mono Filter-Free Class-D Audio Amplifier

1 GENERAL DESCRIPTION

The NAU82011VG is a mono high efficiency filter-free Class-D audio amplifier with variable gain, which is capable of driving a 4Ω load with up to 3.1W output power. This device provides chip enable pin with extremely low standby current and fast start-up time of 4ms.

The NAU82011VG is ideal for battery driven portable applications, as it has advanced features 91% efficiency, low quiescent current (i.e. 1.25mA at 3.6V) and superior EMI performance. It has the ability to configure the inputs in either single-ended or differential mode.

NAU82011VG is available in Miniature 9 ball WL-CSP (1.17mm x 1.19mm in 0.4mm pitch).

FEATURES

- Low Quiescent Current:
 - 1.25mA at 3.6V
 - 1.8mA at 5V
 - 1.61 W (4Ω @ 3.6V, 10% THD+N)
 - 1.30 W (4Ω @ 3.6V, 1% THD+N)
 - 0.85 W (8Ω @ 3.6V, 10% THD+N)
 - 0.69 W (8Ω @ 3.6V, 1% THD+N)
- Powerful Mono Class-D Amplifier:
 - 3.1W (4Ω @ 5V, 10% THD+N)
 - 2.38W (4Ω @ 5V, 1% THD+N)
 - 1.70W (8Ω @ 5V, 10% THD+N)
 - 1.38W (8Ω @ 5V, 1% THD+N)
- Low Output Noise: 20 μV_{RMS}
- Low Current Shutdown Mode
- Integrated Image Reject Filter
- Click-and- Pop Suppression
- Integrated feedback resistor of 300 kΩ
- 1.17mm x 1.19mm WL-CSP (0.4mm Pitch)

Applications

- Smartphones
- Tablet PCs
- Personal Navigation Devices

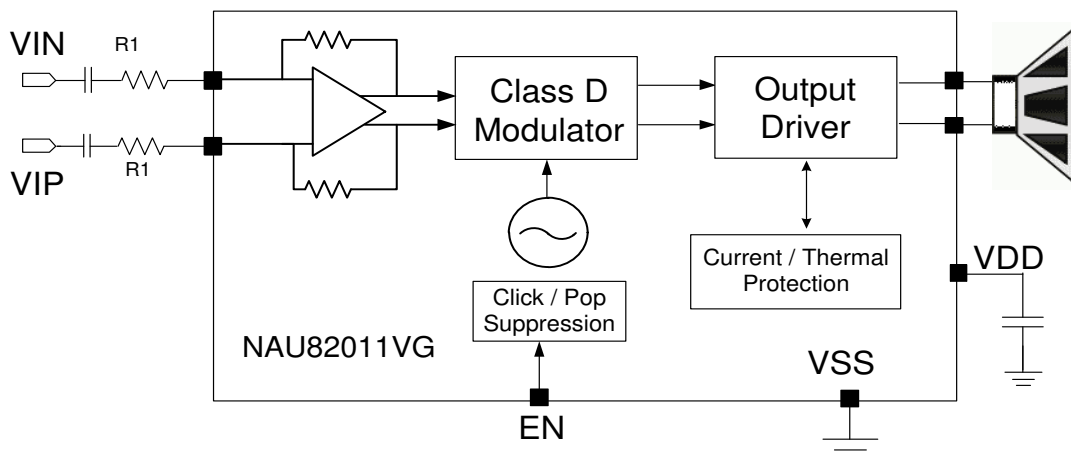
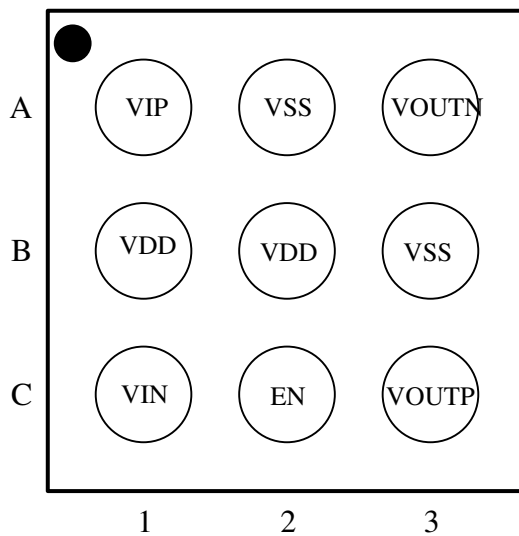


Figure 1: NAU82011VG Block Diagram

Pin out (Top View)



Part Number	Dimension	Package	Package Material
NAU82011VG	1.17mm x 1.19mm	9-ball WL-CSP (0.4mm pitch)	Green

Pin Descriptions

Pin #	Name	Type	Functionality
A1	VIP	Analog Input	Positive Differential Input
A2	VSS	Supply	High Current Ground
A3	VOUTN	Analog Output	Negative BTL Output
B1	VDD	Supply	Power Supply
B2	VDD	Supply	Power Supply
B3	VSS	Supply	High Current Ground
C1	VIN	Analog Input	Negative Differential Input
C2	EN	Digital Input	Chip Enable (High = Power Up; Low = Power Down)
C3	VOUTP	Analog Output	Positive BTL Output

Table 1: NAU82011VG Pin description

Electrical Characteristics

Conditions: EN = VDD = 5V, VSS = 0V, Av = 6dB, R1 = 150kΩ, ZL = ∞, Bandwidth = 20Hz to 22kHz, TA = 25 °C

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units	
Power Delivered							
Output Power	P _{out}	Z _L = 4Ω + 33μH	VDD = 5.0V		3.10		W
		THD + N = 10%	VDD = 3.6V		1.61		
		Z _L = 4Ω + 33μH	VDD = 5.0V		2.38		
		THD + N = 1%	VDD = 3.6V		1.30		
		Z _L = 8Ω + 68μH	VDD = 5.0V		1.70		
		THD + N = 10%	VDD = 3.6V		0.85		
		Z _L = 8Ω + 68μH	VDD = 5.0V		1.38		
		THD + N = 1%	VDD = 3.6V		0.69		

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Chip Enable (EN)						
Voltage Enable High	V _{EN,H}	VDD = 2.5V to 5.5V	1.3			V
Voltage Enable Low	V _{EN,L}	VDD = 2.5V to 5.5V			0.35	V
Input Leakage Current				0.1	2.0	μA
Thermal and Current Protection						
Thermal Shutdown Temperature				150		°C
Thermal Shutdown Hysteresis				20		°C
Over Current Threshold	I _{OC}			2.0		A
Gain	A _V	VDD = 2.5V to 5.5V, R1 in kΩ	255/R1	300/R1	345/R1	V/V
Resistance (EN pin to GND)	R _{EN}			300		kΩ

Electrical Characteristics (continued)

Conditions: $V_{EN} = V_{DD} = 5V$, $V_{SS} = 0V$, $A_v = 6dB$, $R_1 = 150k\Omega$, $Z_L = \infty$, Bandwidth = 20Hz to 22kHz, $T_A = 25^\circ C$

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Normal Operation						
Quiescent Current Consumption	I_{QUI}	$V_{DD} = 3.6V$		1.25		mA
		$V_{DD} = 5V$		1.8		mA
Shut Down Current	I_{OFF}	$EN = 0$		0.1		μA
Oscillator Frequency	f_{OSC}			300		kHz
Efficiency	η	WL-CSP		91		%
Start Up Time	T_{start}			4		msec
Output Offset Voltage	V_{OS}			± 1		mV
Common Mode Rejection Ratio	$CMRR^1$	$f_{IN} = 1kHz$		80		dB
Click-and-Pop Suppression		1Hz Shutdown ($Z_L=8\Omega$)		83		dBV
Power Supply Rejection Ratio	PSRR	DC PSRR		90		dB
		AC PSRR $V_{RIPPLE} = 0.2V_{pp}@1kHz$		65		dB
Noise Performance		$V_{DD} = 3.6V$ (A-weighted)		20		μV_{RMS}

Note 1: The CMRR measurement is limited by the device as well as external resistors (R_1) matching.

Absolute Maximum Ratings

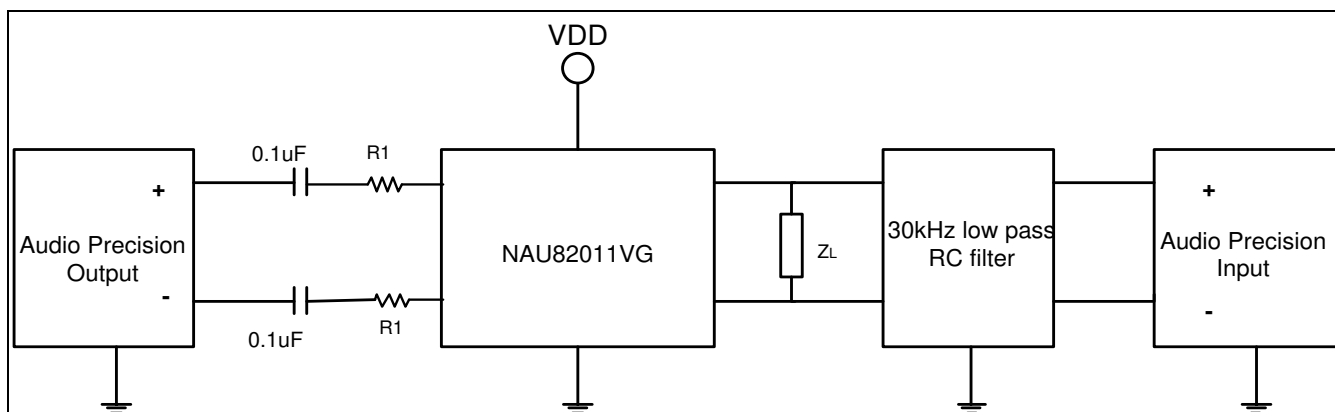
Parameter	Min	Max	Units
Analog supply	-0.50	+5.50	V
Industrial operating temperature	-40	+85	$^\circ C$
Storage temperature range	-65	+150	$^\circ C$
Junction temperature range	-40	+150	$^\circ C$

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Analog supply range	VDD	2.50	5.00	5.50	V
Ground	VSS		0		V
Input Resistor (Gain \leq 26dB)	R1	15			k Ω
Common mode Input voltage range VDD = 2.5V to 5.5V and CMRR \geq 49dB	V _{IC}	0		VDD - 1.0	V

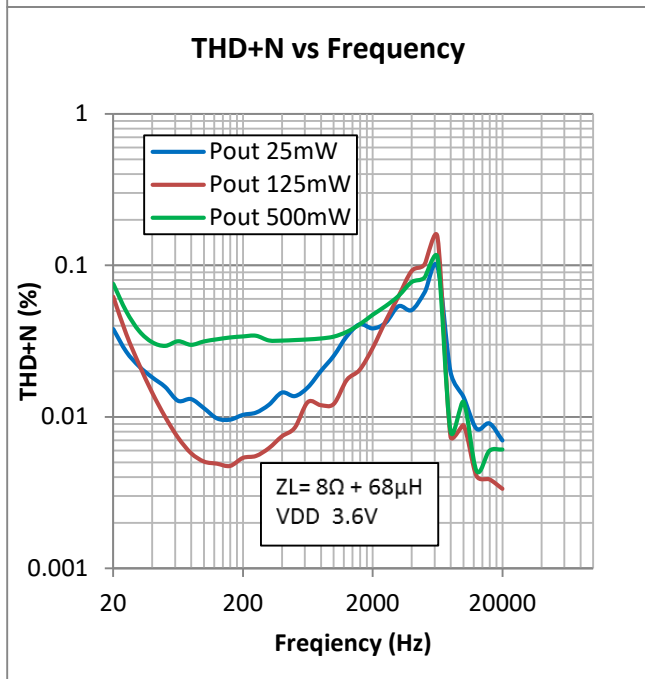
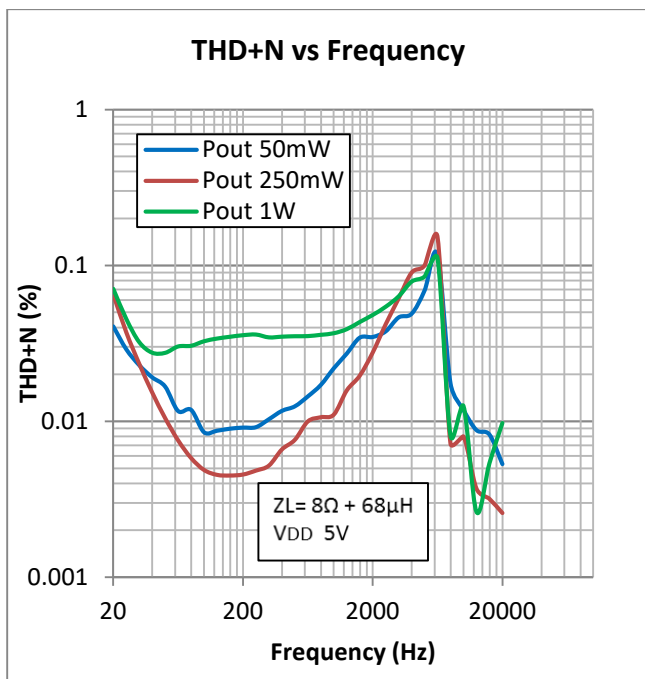
Test Set up

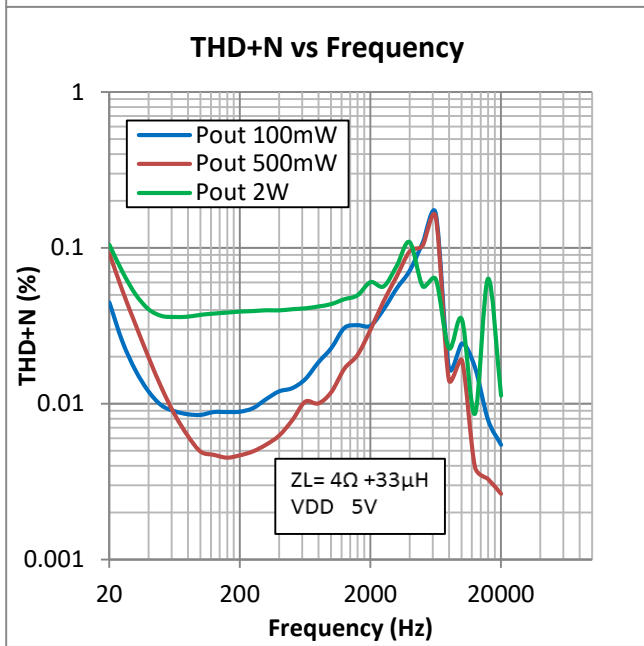
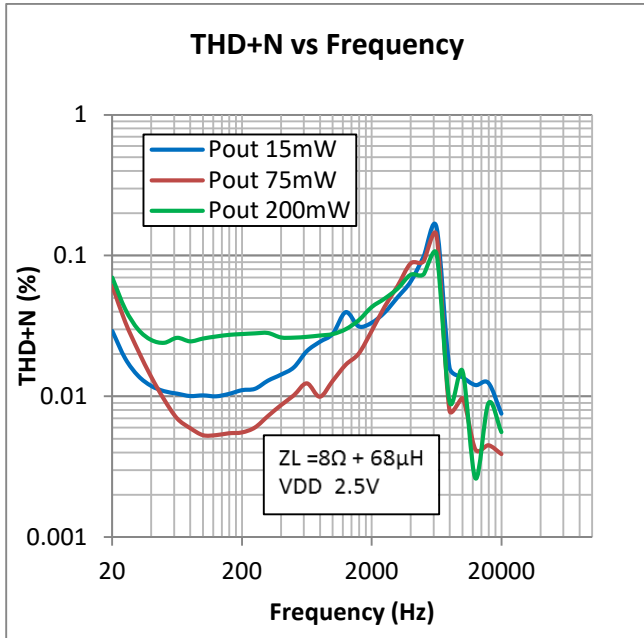


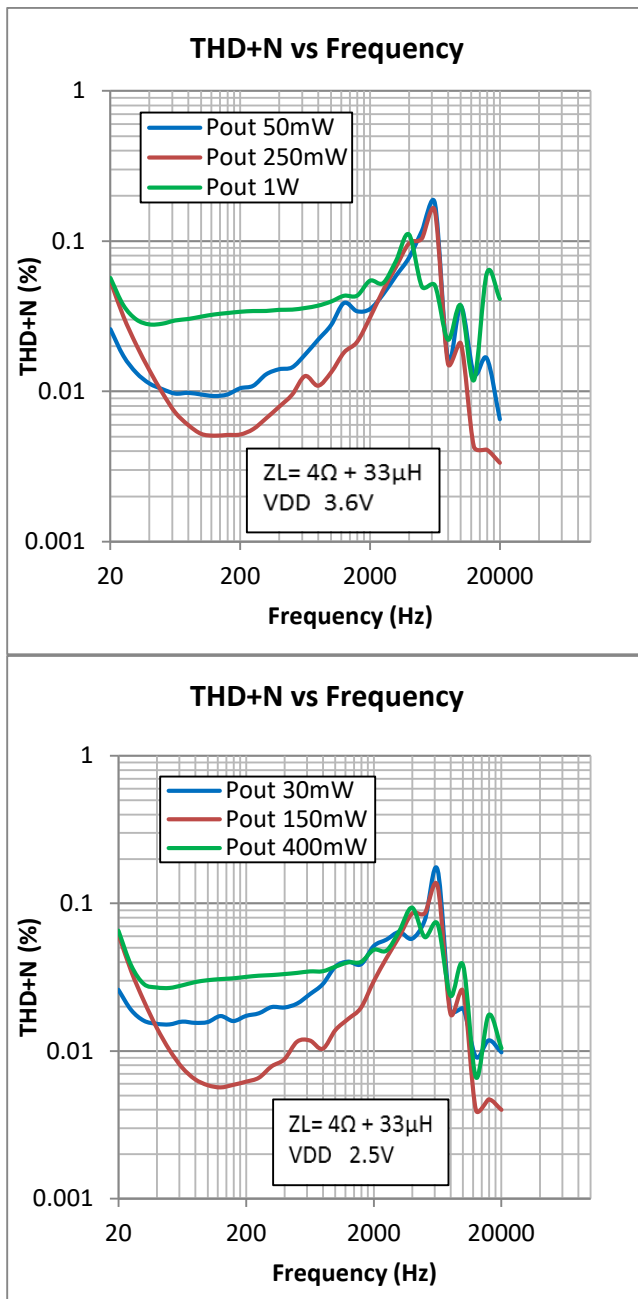
Note: The 30kHz low pass RC filter is implemented by using R= 1k Ohm and C = 4.7nF

Typical Operating Characteristics

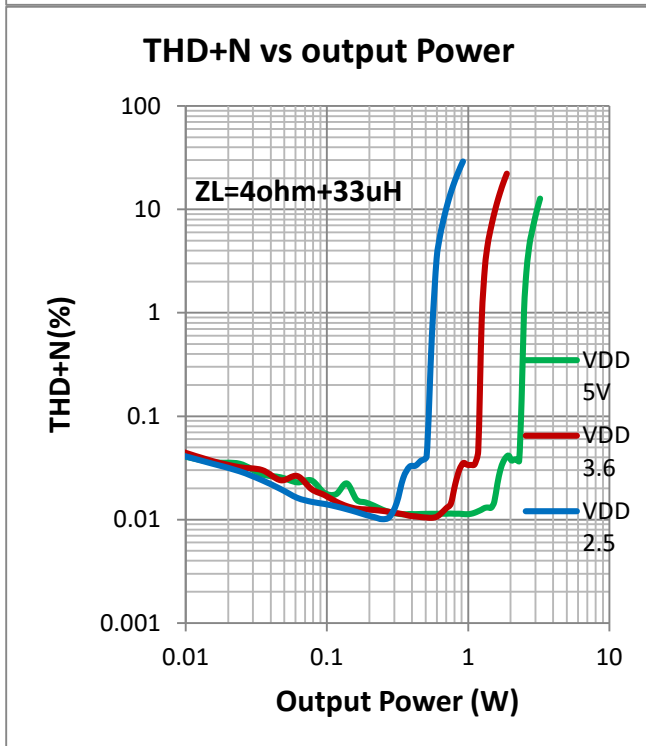
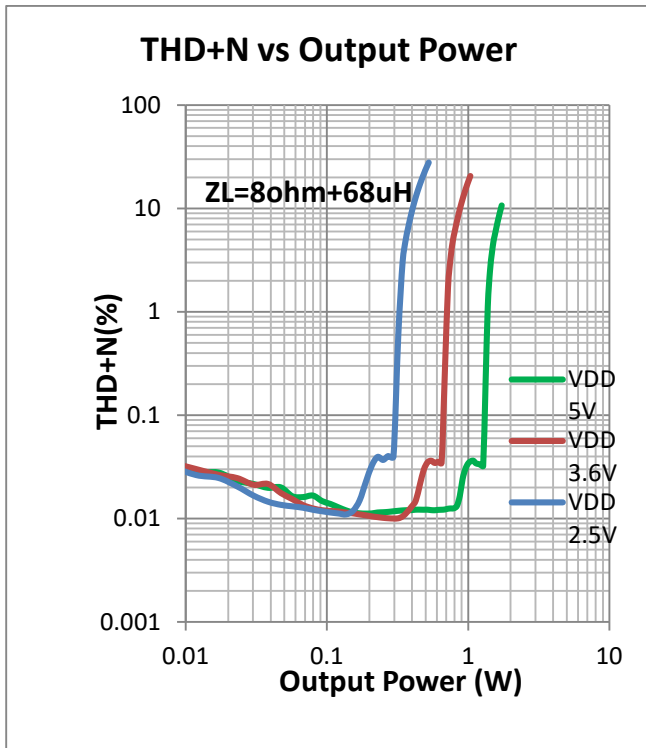
Conditions: $V_{DD} = 5V$, $V_{SS} = 0V$, $A_v = 6dB$ ($R=150k\Omega$), $Z_L = \infty$, Bandwidth = 20Hz to 22kHz, $T_A = 25^\circ C$, unless otherwise noted

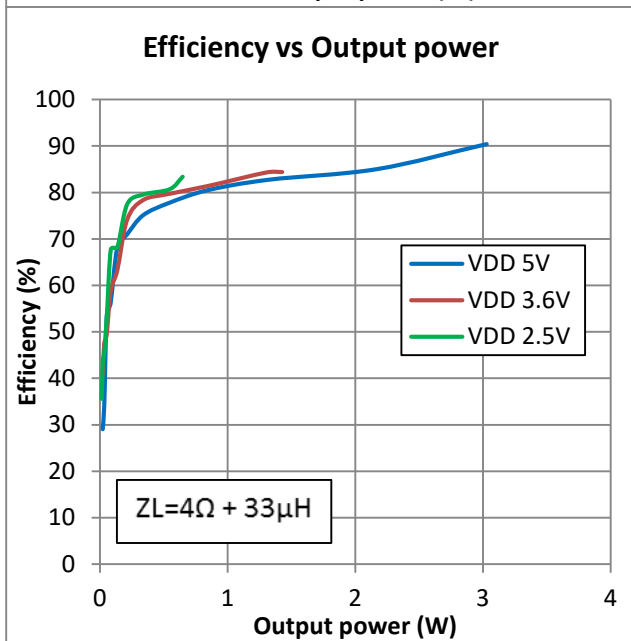
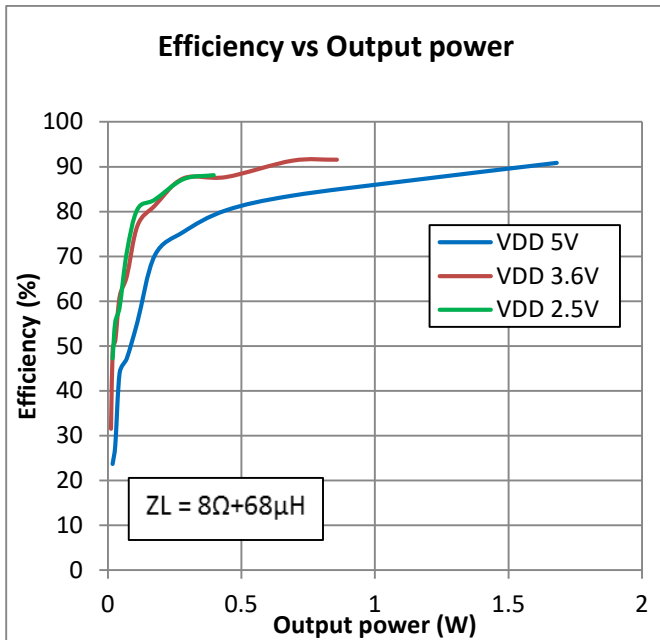


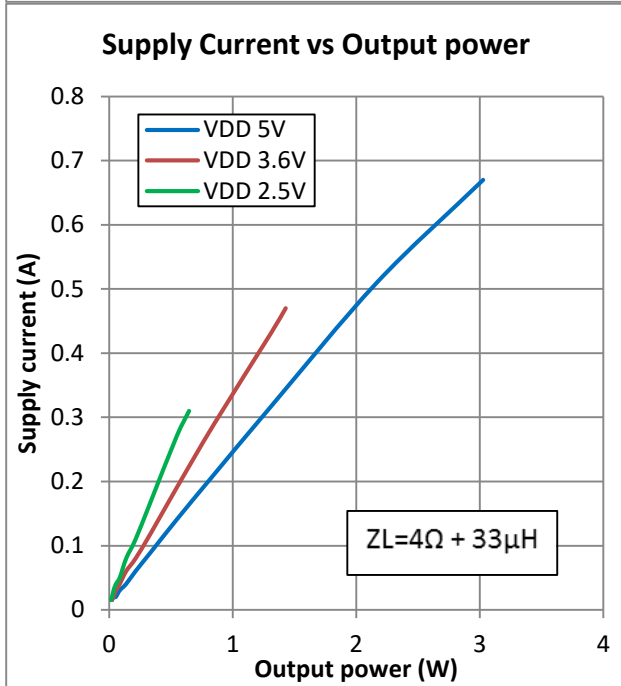
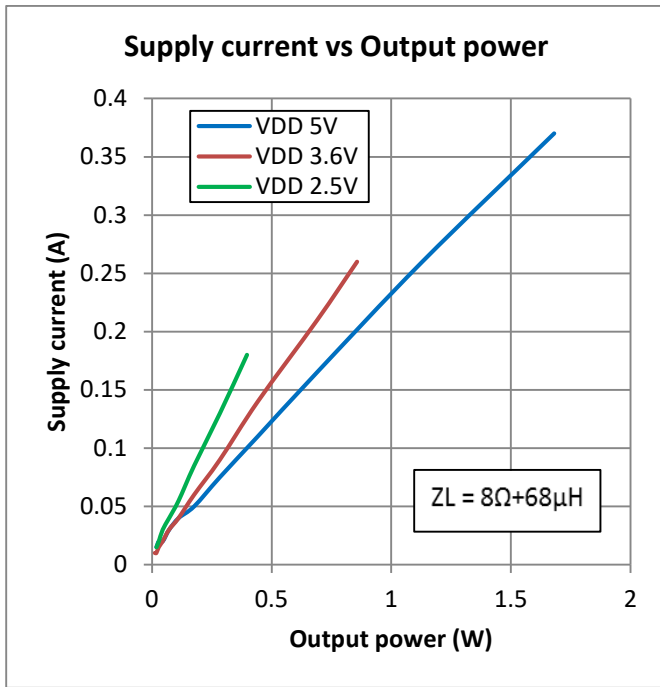


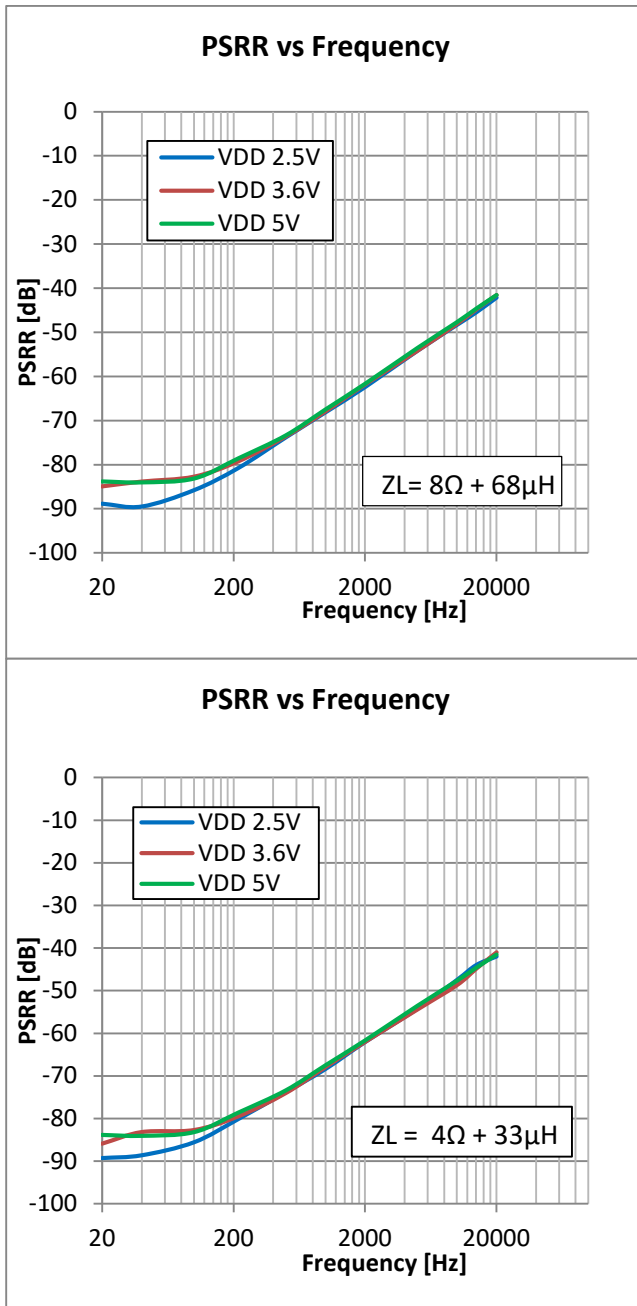


Note: All the above plots are captured with 0.1uF input capacitor. It is recommended to use 2.2uF input capacitor to get a flat low frequency response.

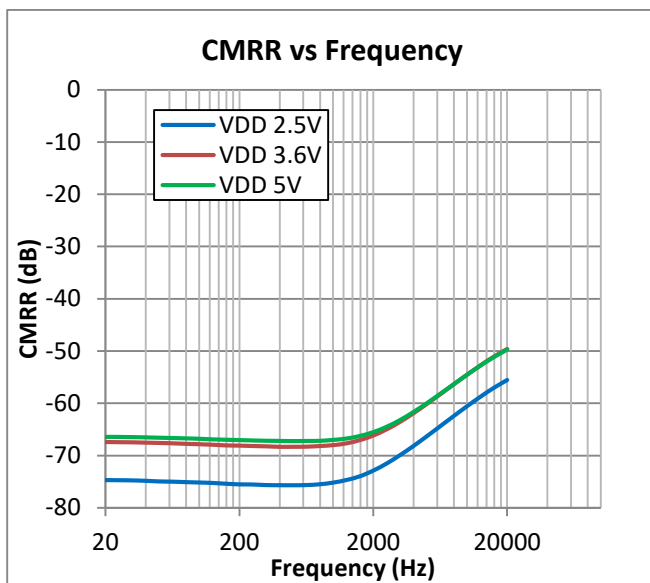








Note : The above PSRR plots are captured with input capacitors 2.2uF



Special Feature Description

The NAU82011VG offers excellent quantity performance including high efficiency, high output power and low quiescent current. It also provides the following special features.

1.1 Device Protection

The NAU82011VG includes device protection for three operating scenarios. They are

1. Thermal Overload
2. Short circuit
3. Supply under voltage

1.1.1 Thermal Overload Protection

When the device internal junction temperature reaches 150°C, the NAU82011VG will disable the output drivers. When the device cools down and a safe operating temperature of 130°C has been reached for at least about 100ms, the output drivers will be enabled again.

1.1.2 Short Circuit Protection

If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 16.7μs, the output drivers will be disabled for 100ms. The output drivers will then be enabled again and checked for the short circuit. If the short circuit is still present, the output drivers are disabled after 16.7μs. This cycle will continue until the short circuit is removed. The short circuit threshold is 2.0A at 3.6V.

1.1.3 Supply under Voltage Protection

If the supply voltage drops under 2.1V, the output drivers will be disabled while the NAU82011VG control circuitry still operates. This will avoid the battery supply being dragged down too low before the host processor can safely shut down the devices in the system. If the supply drops further below 1.6V, the internal power on reset is activated and puts the entire device in power down state.

1.1.4 Power up and Power down Control

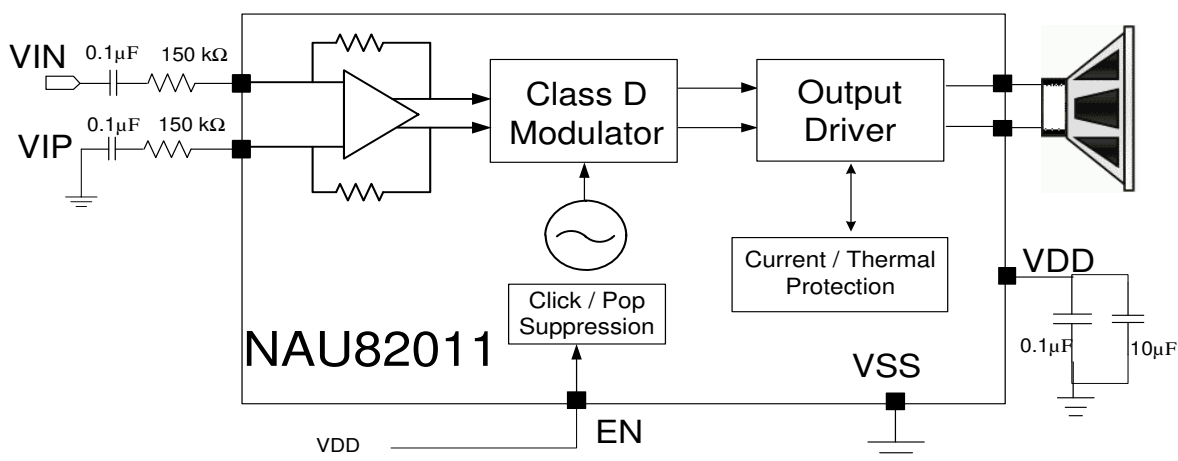
When the supply voltage ramps up, the internal power on reset circuit gets triggered. At this time all internal circuits will be set to power down state. The device can be enabled by setting the EN pin high. Upon setting the EN pin high, the device will go through an internal power up sequence in order to minimize ‘pops’ on the speaker output. The complete power up sequence will take about 4ms. The device will power down in about 30μs, when the EN pin is set low.

It is important to keep the input signal at zero amplitude in order to minimize the ‘pops’ when the EN pin is toggled.

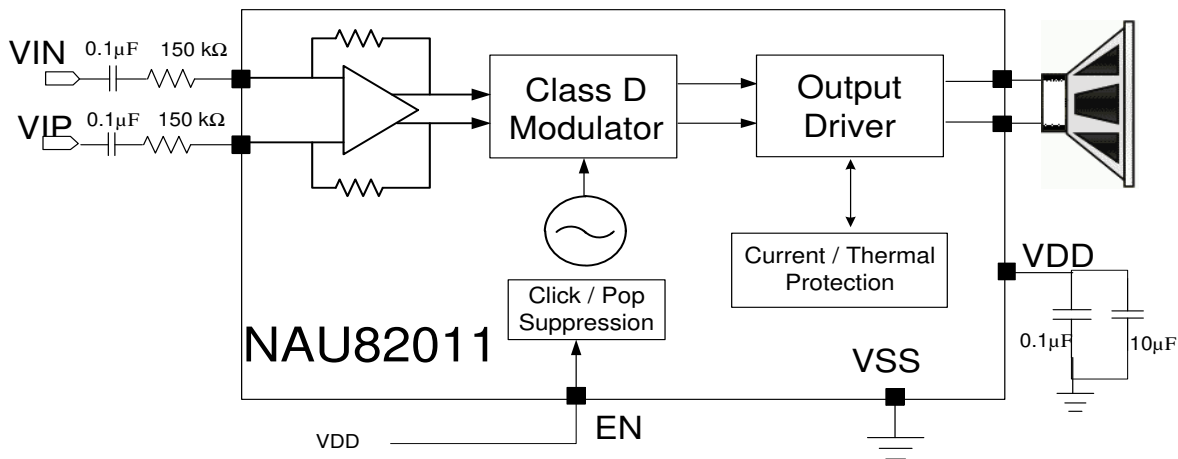
Application Information

1.2 Application diagram

1.2.1 Single ended input configuration



1.2.2 Differential input configuration



1.3 Component selection

1.3.1 Input resistors for Gain

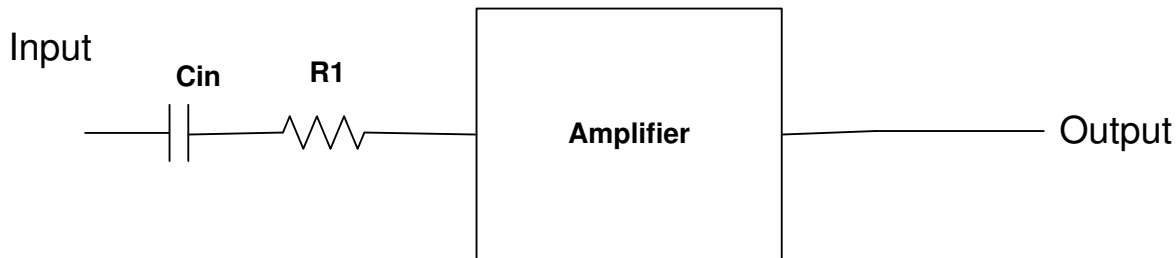
NAU82011VG has a provision for variable gain setting by using external input resistors. The gain is expressed as the ratio of the internal feedback resistor of 300kΩ and the external input resistor R. The Gain is expressed as

$$Gain = \frac{300 \text{ k}\Omega}{R \text{ k}\Omega} \left(\frac{V}{V} \right) \quad Gain \text{ (dB)} = 20 \log \frac{300 \text{ k}\Omega}{R \text{ k}\Omega}$$

1.3.2 Coupling Capacitors

An ac coupling capacitor (C_{in}) is used to block the dc content from the input source. The input resistance of the amplifier (R) together with the C_{in} will act as a high pass filter. So depending on the required cut off frequency the C_{in} can be calculated by using the following formula

$$C_{in} = 1/2\pi R f_c \quad \text{Where } f_c \text{ is the desired cut off frequency of the High pass filter.}$$

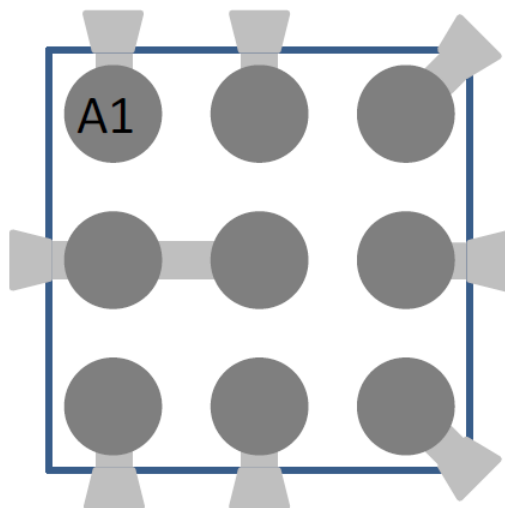


1.3.3 Bypass Capacitors

Bypass capacitors are required to remove the ac ripple on the VDD pins. The value of these capacitors depends on the length of the VDD trace. In most cases, 10uF and 0.1uF are enough to get the good performance.

1.4 Layout considerations

Good PCB layout and grounding techniques are essential to get the good audio performance. It is better to use low resistance traces as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

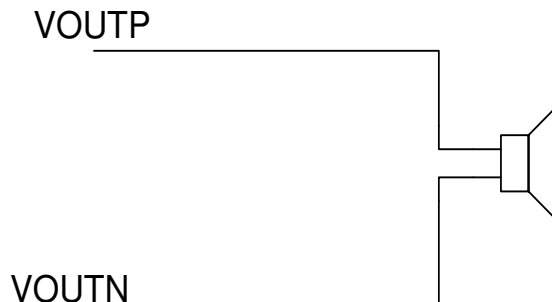


Recommended PCB footprint for NAU82011VG

The recommended PCB footprint for NAU82011VG is shown in the above diagram.

1.5 Class D without filter

The NAU82011VG is designed for use without any filter on the output line. That means the outputs can be directly connected to the speaker in the simplest configuration. This type of filterless design is suitable for portable applications where the speaker is very close to the amplifier. In other words, this is preferable in applications where the length of the traces between the speaker and amplifier is short. The following diagram shows this simple configuration.



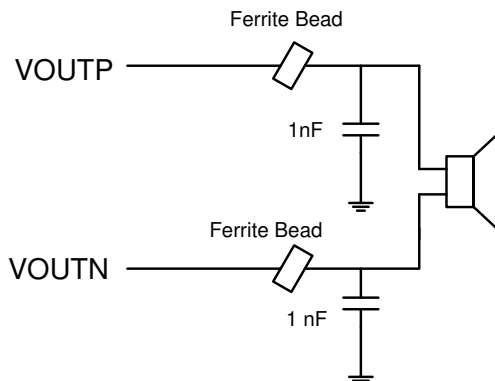
NAU82011VG outputs connected to speaker without filter circuit

1.6 Class D with filter

In some applications, the shorter trace lengths are not possible because of speaker size limitations and other layout reasons. In these applications, the long traces will cause EMI issues. There are two types of filter circuits available to reduce the EMI effects. These are ferrite bead and LC filters.

1.6.1 Ferrite Bead filter

The ferrite bead filters are used to reduce the high frequency emissions. The typical circuit diagram is shown in the figure.

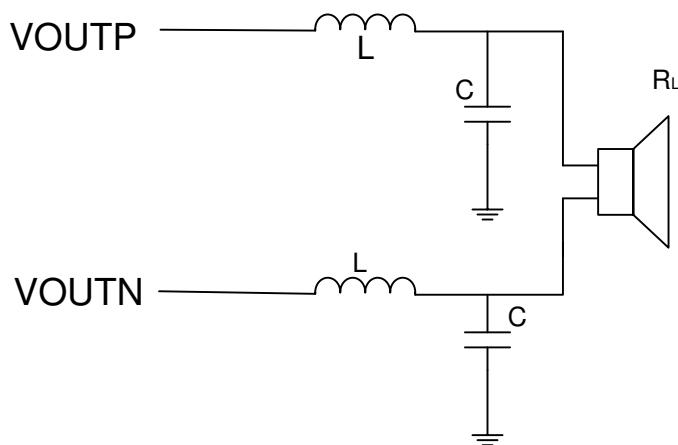


NAU82011VG outputs connected to speaker with Ferrite Bead filter

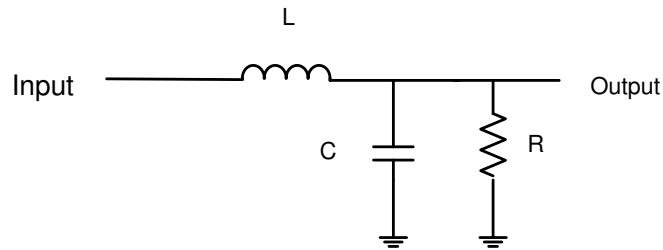
The characteristic of ferrite bead is such that it offers higher impedance at high frequencies. For better EMI performance select ferrite bead which offers highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. Usually the ferrite beads have low impedance in the audio range, so it will act as a pass through filter in the audio frequency range.

1.6.2 LC filter

The LC filter is used to suppress the low frequency emissions. The following diagram shows the NAU82011VG outputs connected to the speaker with LC filter circuit. R_L is the resistance of the speaker coil.



NAU82011VG outputs connected to speaker with LC filter



Standard Low pass LCR filter

The following are the equations for the critically damped ($\zeta = 0.707$) standard low pass LCR filter

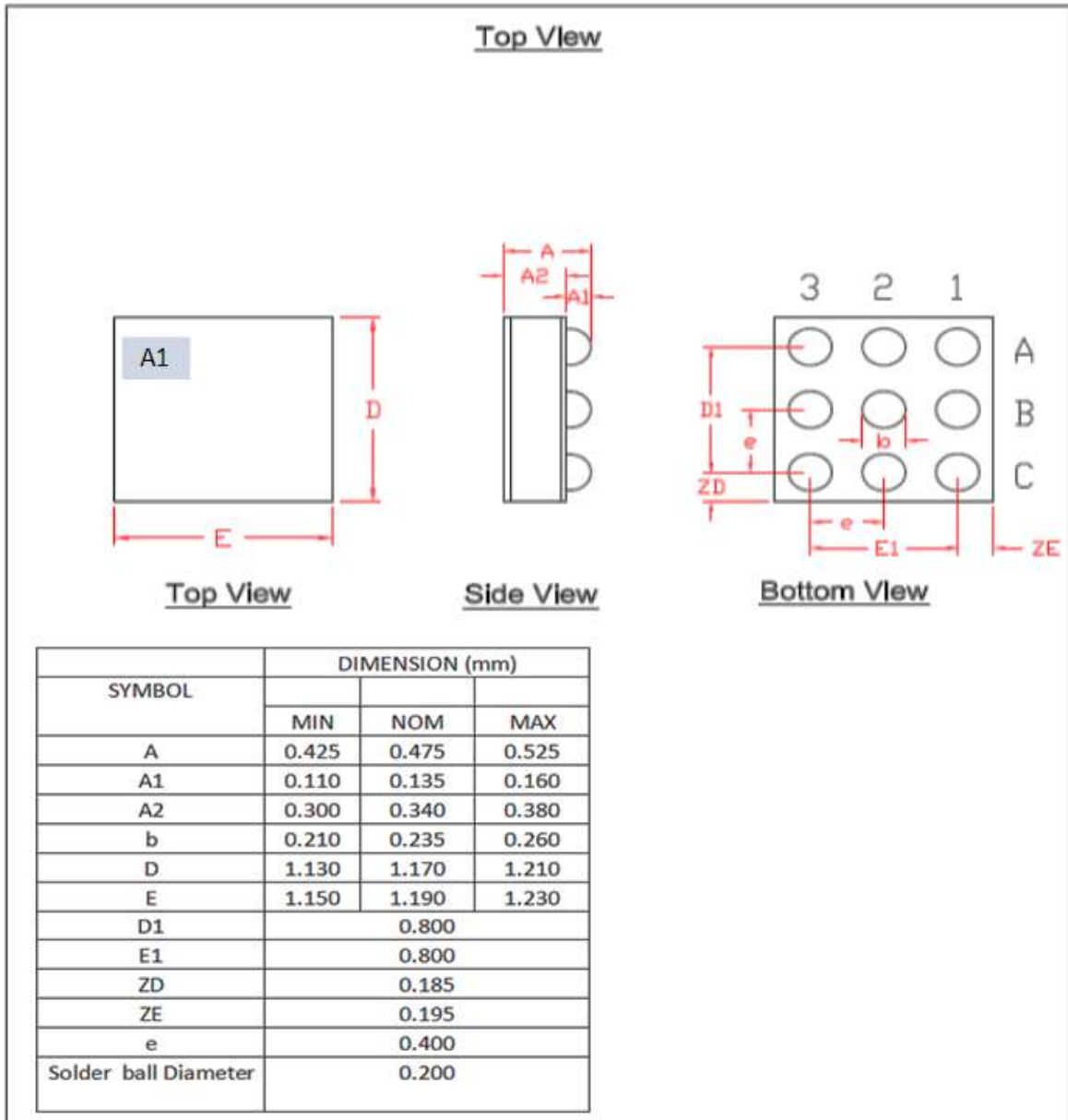
$$2\pi f_c = \frac{1}{\sqrt{LC}} \quad f_c \text{ is the cutoff frequency}$$

$$\zeta = 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

The L and C values for differential configuration can be calculated by duplicating the single ended configuration values and substituting $R_L = 2R$.

Package Dimensions

1.7 9 ball WL-CSP (0.4mm pitch)(1.17mm x1.19mm)



Ordering Information

Part Number	Dimension	Package	Package Material
NAU82011VG	1.17x1.19 mm	WLCSP-9	Green

NAU82011 _ _

Package Material:

G = Pb-free Package

Package Type:

V = 9-Pin WLCSP Package

REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
Rev1.0	Oct, 2012	NA	Revision1.0
Rev1.1	Jan, 2013	NA	<ol style="list-style-type: none"> 1. Removed MSOP 8 package information 2. Changed package material from pb-free to Green
Rev1.2	Oct, 2015	1, 7	<p>Updated 40mh loading power at THD+N=1% and 10%</p> <p>Put new THD vs Po plot</p>
Rev1.3	Jan, 2021	All	Update Document Format

Table 1: Revision History

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