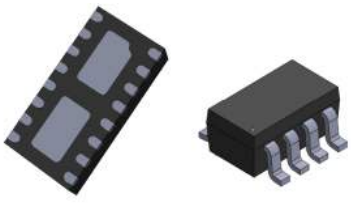
CLT03-2Q3, CLT03-1SC3

Datasheet

Self powered digital input current limiter



QFN-16L 4.0 x 2.0 x 0.9 mm SOT23-8L 2.9 x 2.8 mm

Product label

Product status link

CLT03-2Q3, CLT03-1SC3

Features

- Single and dual isolated channel devices
- No power supply needed
- Digital input current limitation
- Enables input to meet type 1 and 3 characteristic of IEC 61131-2 standard
- Deglitch filter for EMC robustness
- High side / Low side compatible
- Inputs are reverse plugin compatible
- Drive isolated opto-couplers or non-isolated LVTTL digital input termination
- Operating ambient temperature range from -30 °C to 125 °C
- Two packages
  - SOT23-8L - 650 µm pitch
  - QFN-16L - 500 µm pitch
- **Complies with the following standards**:
  - IEC 61000-4-2 level 1: ±4 kV (air discharge)
  - IEC 61000-4-2 level 1: ±2 kV (contact discharge)

Applications

Where current limitation is required in factory automation applications:

- Programmable logic controller
- Remote input module

Description

The CLT03 series is a digital input current limiter which drastically reduces the power dissipation of the digital inputs.

It does not require external power supply as the device is activated with the input signal and it consumes no power in off state.

The CLT03 series is high side and low side compatible, as well as reverse plugin compatible. It can drive either opto-coupler or 3.3 V LVTTL circuit.

The CLT03-2Q3 can be evaluated thanks to the STEVAL-IFP035V1 evaluation board which embeds an isolated and non-isolated digital inputs configuration.

1 I/O pin description

Table 1. CLT03-1SC3 pins name, type, and description

Name	Pin #	Type	Description
INA	2	Signal input	Logic input with current limitation
INATT	3	Signal input	Logic input with current limitation for non-isolated configuration
INB	1	Signal input	Logic input with current limitation
TP	8	Test input	Test pulse input for capacitor
VBUF	7	Power output	Buffer capacitor
OUTN	4	Ground	Logic output ground (channel 1 output ground)
OUTP	6	Signal output	Data output
PD	5	Ground	Logic output ground with pull down resistor (non-isolated mode)

Figure 1. SOT23-8L pinout (top view)

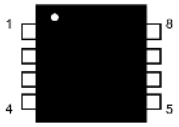
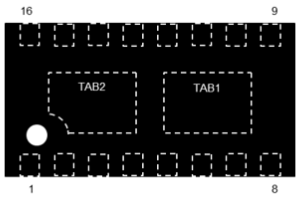


Table 2. CLT03-2Q3 pins name, type, and description

Name	Pin #	Type	Description
INA1 / INA2	7 / 3	Signal input	Logic input with current limitation
INATTL1 / INATTL2	6 / 2	Signal input	Logic input with current limitation for non-isolated configuration
INB1 / INB2	8 / 4	Signal input	Logic input with current limitation
TP1 / TP2	9 / 14	Test input	Test pulse input for capacitor
VBUF1 / VBUF2	10 / 15	Power output	Buffer capacitor
OUTN1	5 / TAB1	Ground	Logic output ground (channel 1 output ground)
OUTN2	13 / TAB2	Ground	Logic output ground (channel 2 output ground)
OUTP1 / OUTP2	11 / 16	Signal output	Data output
PD1/PD2	12 / 1	Ground	Logic output ground with pull down resistor (non-isolated mode)

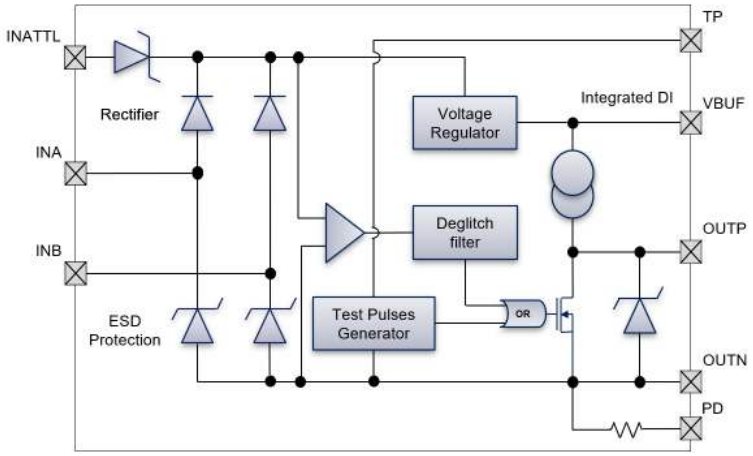
Figure 2. QFN-16L 4.0 x 2.0 pinout (top view)



2 Characteristics

2.1 Circuit block diagram

Figure 3. Channel diagram



2.2 Absolute maximum ratings

Stresses outside the absolute ratings range may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter name	Value	Unit
V_{PP}	Peak pulse voltage, HBM, MIL STD 883J-Method 3015.9	±2	kV
V_{PP} (1)(2)	Peak pulse voltage (pins INA, INATTL & INB), IEC 61000-4-2 (contact)	±2	kV
V_{IN}	Input voltage	-60 to +60	V
V_{ISO}	CLT03-2Q3: Isolation between channel 1 and 2	230	V_{AC}
T_j	Junction temperature	-30 to +125	°C
T_{STG}	Storage temperature	-55 to +150	°C

1. *See application schematic*
2. *Performance level depends on layout and environment*

Table 4. Thermal resistance parameter

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	CLT03-1SC3: Thermal resistance junction to ambient, according to EIA/JEDEC JESD51-7 and JESD51-5	120	°C/W
$R_{th(j-a)}$	CLT03-2Q3: Thermal resistance junction to ambient, according to EIA/JEDEC JESD51-7 and JESD51-5	41	°C/W
Ψ_{JT}	CLT03-2Q3: Thermal characterization parameter from junction to the top of the package surface (°C/W) according to EIA/JEDEC JESD51-2A	32	°C/W

2.3 Electrical characteristics

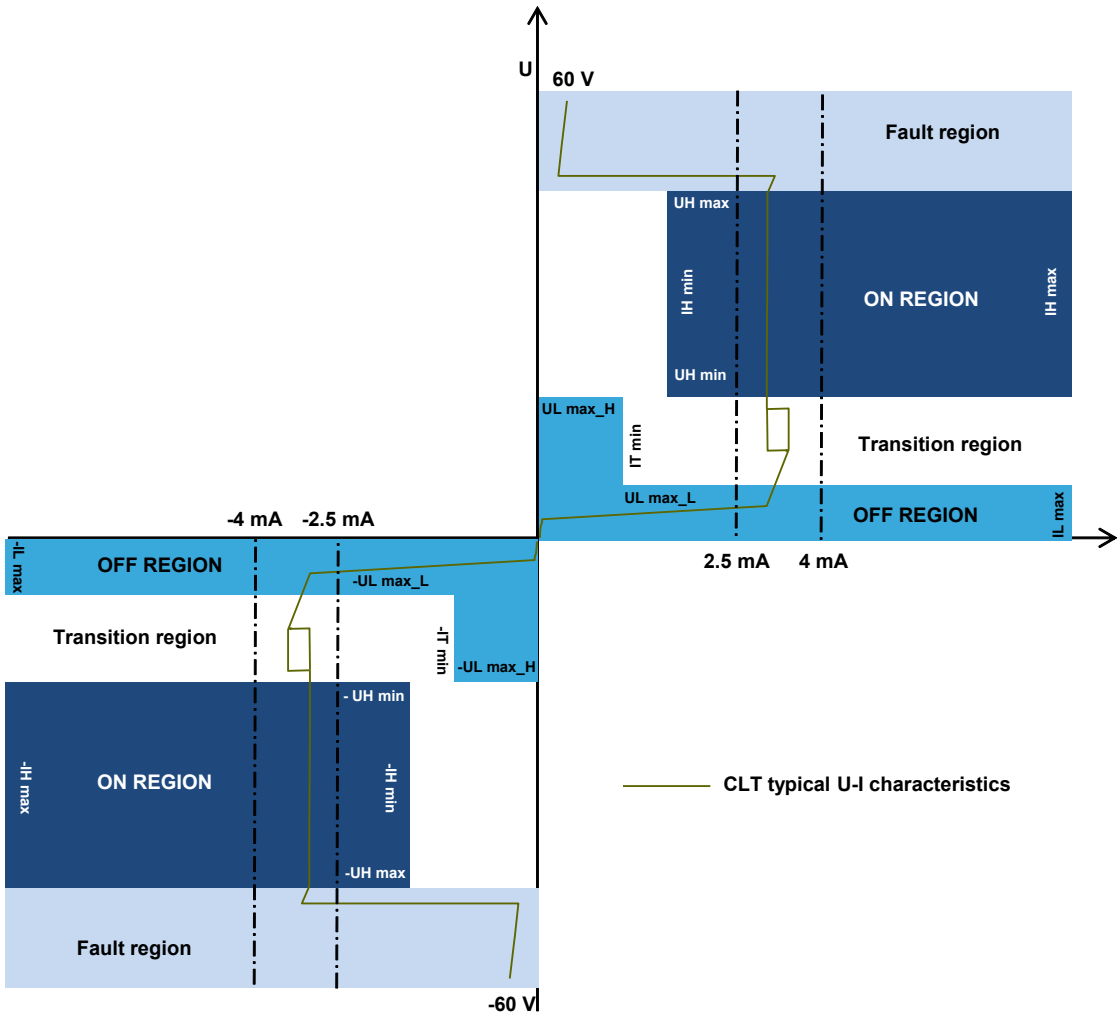
Table 5. Electrical characteristics (-30 °C < $T_{ambient}$ < +125 °C, unless otherwise specified) (values)

Symbol	Description	Name	Min.	Typ.	Max.	Unit
Input						
I_{LIM}	Input current – On state		2.5		4	mA
I_{IN}	Input current at V_{IN} = 5 V		2.5			mA
V_{TLH}	Low to High state input voltage			9.4	11	V
V_{THL}	High to Low state input voltage		5	7.5		V
V_{HYST}	Input triggering voltage hysteresis		1.2		2.6	V
V_{FAULT}	Fault mode threshold voltage		30	40		V
I_{FAULT}	Input current in fault region V_{IN} > V_{FAULT}		1		2.5	mA
Timing parameters						
f_{IN}	Input frequency				35	kHz
t_{FAULT}	Fault mode triggering latency after V_{IN} > V_{FAULT}			25		µs
t_{PLH}	Input to output low to high propagation time (including deglitch filter)(1)		2		5	µs
t_{PHL}	Input to output high to low propagation time (including deglitch filter) (1)		2		5	µs
Ouput						
I_{OUT}	On state	Isolated mode	2		4	mA
		Non-isolated mode			1	mA
	Off state	Isolated and non-isolated mode	-10		10	µA
V_{OUT}	On state	Isolated mode	0.7		3.6	V
		Non-isolated mode	3		3.6	V
	Off state	Isolated and non-isolated mode	-0.3		0.4	V
R_{OUT}	OUTP to OUTN internal equivalent output resistance (V_{INA} - V_{INB} = 0 V)			24		kΩ
R_{PD}	OUTN to PD internal pull down resistor		2.85		4.25	kΩ

1. *See Figure 10. t_{PLH} and t_{PHL} test condition*

3 U-I operation description

Figure 4. **Input U-I operation and IEC61131-2 characteristic limits**

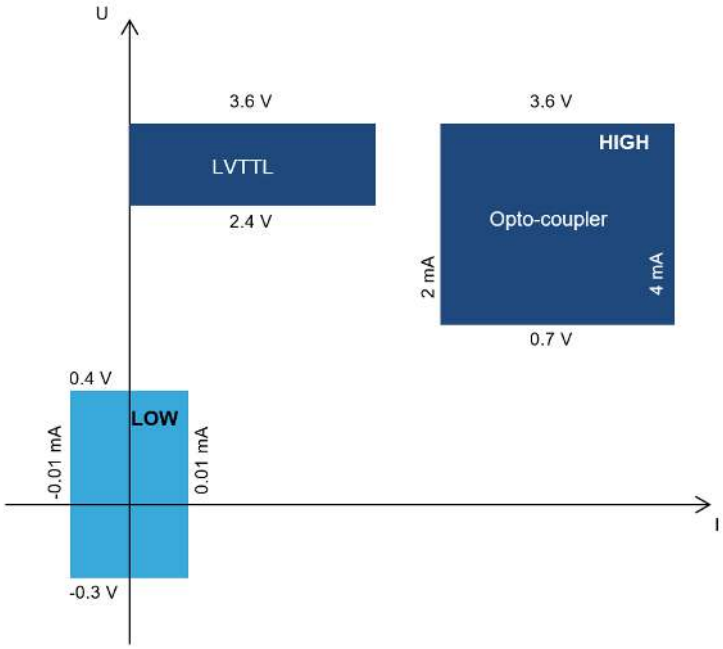


Note: When the input current stays below 2.5 mA, the CLT03 output remains in the OFF state.

Table 6. **IEC61131-2 Input characteristic limits**

Symbol	Type 1	Type 3
UL max_H	15 V	11 V
UL max_L	5 V	5 V
IL max.	15 mA	15 mA
IT min.	0.5 mA	1.5 mA
UH min.	15 V	11 V
UH max.	30 V	30 V
IH min.	2 mA	2 mA
IH max.	15 mA	15 mA

Figure 5. **Output U-I operation**



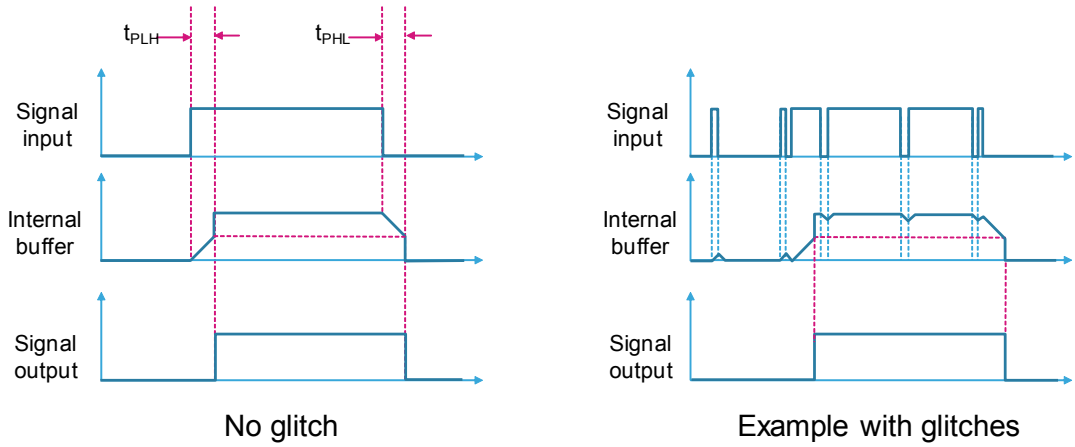
4 Fault mode description

When the input voltage V_{IN} exceeds a threshold V_{FAULT} = 30 V the CLT03 series activates the Fault Mode with a defined latency t_{FAULT}. In this mode the CLT03 series further reduces the input current limitation down to I_{FAULT} and the corresponding output channel is deactivated.

Fault mode ensures defined and safe operation of the CLT03 series in overvoltage condition as it is often required by safety regulations.

5 Deglitch filter

Figure 6. Deglitch filter



To provide the best EMI robustness solution, a deglitch filter based on a non-resettable mono-stable has been integrated. As described in Figure 6. Deglitch filter, to avoid parasitic spike in output signal when glitches occur in input signals, the integrated internal buffer cleans the glitch effect.

The output activation and deactivation action times is defined by t_{PLH} and t_{PHL} when no glitch.

6 Test pulse feature description

The built-in test pulse feature eases diagnostic checks. It is possible to know on a regular basis that the CLT03 is still working properly.

This feature is especially important for safety applications and often required by safety regulations.

In order, to enable the Test Pulse feature a capacitor should be connected between TP and OUTN pins. When such a capacitor is connected, the OUTP value will be forced to low state every TP period (P_{TP}) for a define test pulse width (t_{TP}). TP period is equal to 256 times t_{TP}.

The frequency of the “Test Pulse low state” is managed through the capacitor value. In order to disable this feature, TP should be shorted to OUTN.

Table 7. Test pulse parameters

Symbol	Description	Min.	Typ.	Max.	Unit
f_{TP}	Test pulse frequency	4.1		219	kHz
C_{TP}	External capacitor range	100		4700	pF
t_{TP}	Test pulse width	$1/f_{TP}$			ms
P_{TP}	Test pulse period	256 x t_{TP}			ms
Δf_{TP}	Test pulse frequency variation (out of capacitance variation)	-60		+60	%

Figure 7. Test Pulse parameters description

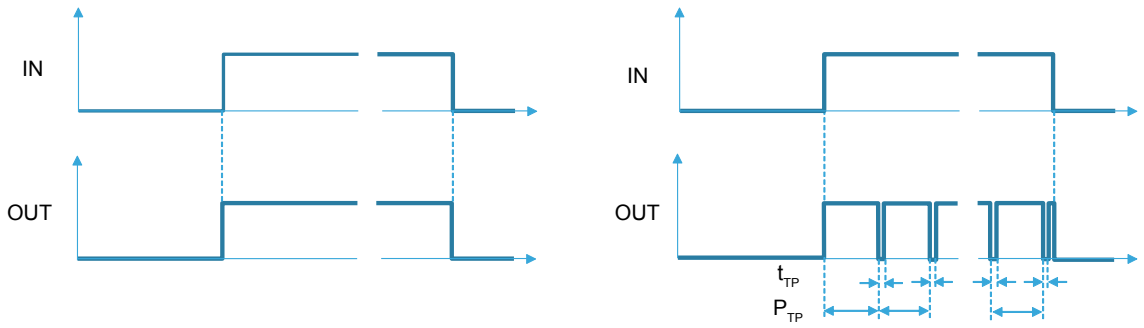


Figure 8. f_{TP} versus C_{TP} value

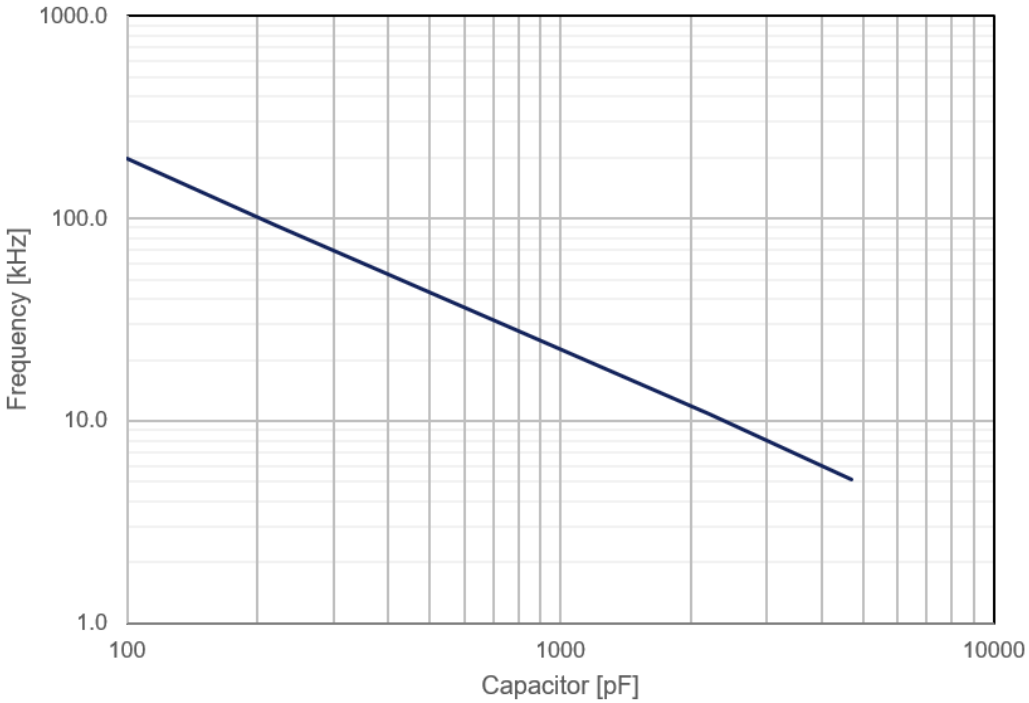
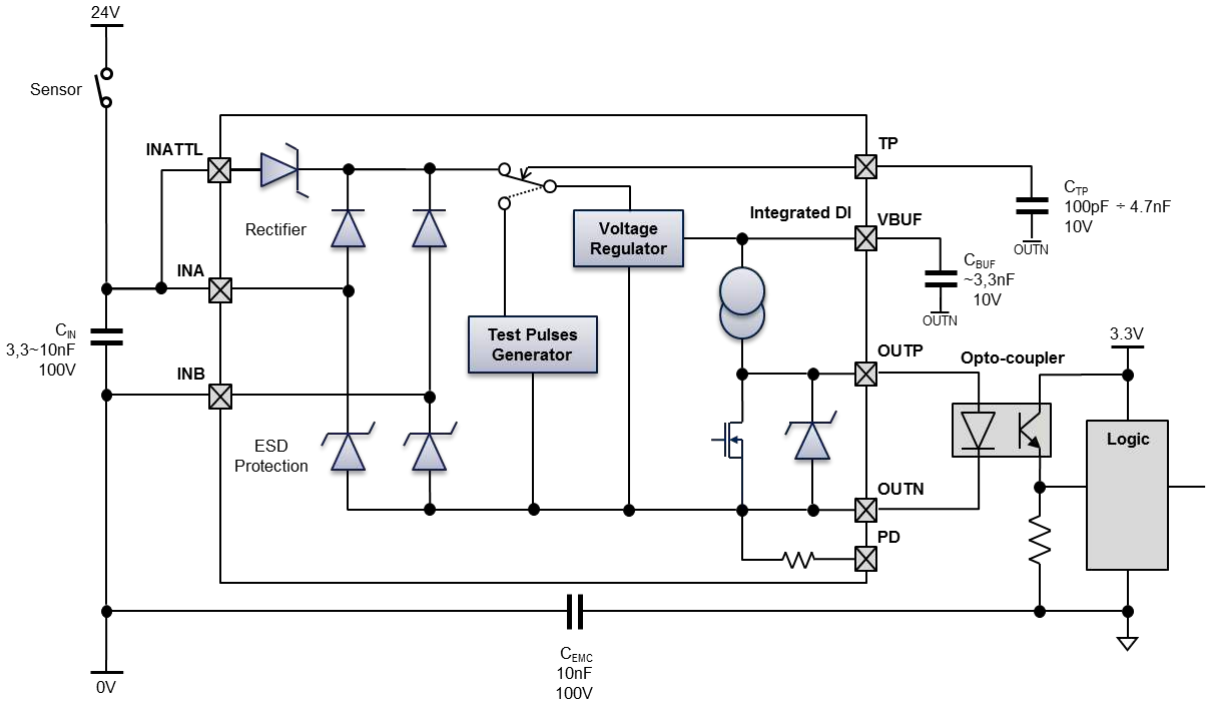
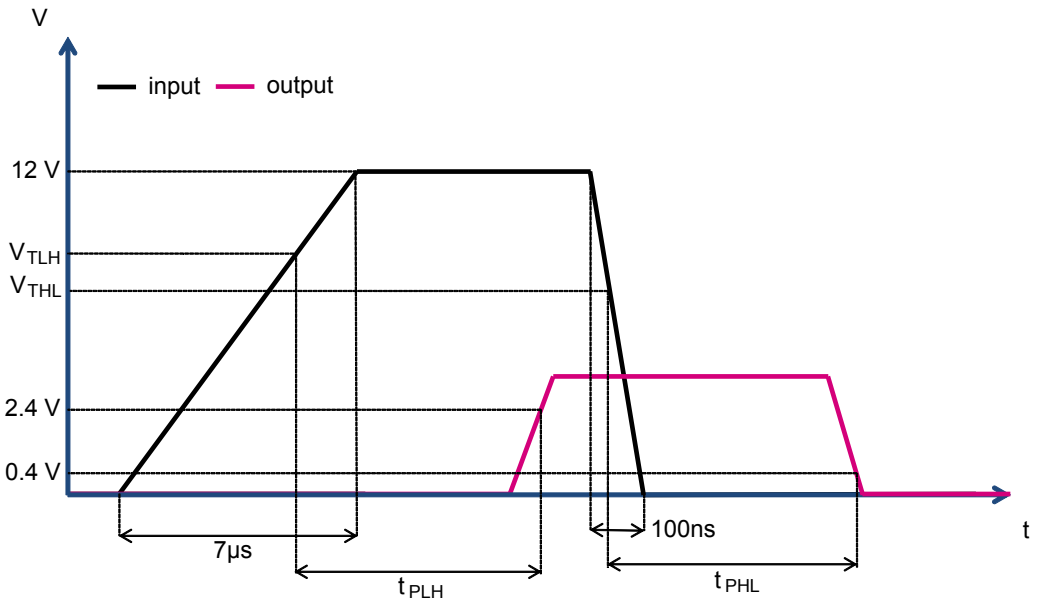


Figure 9. High side - isolated configuration - test pulse activated



7 Propagation time measurement description

Figure 10. t_{PLH} and t_{PHL} test condition



Note: for t_{PLH} and t_{PHL} measurement, V_{TLH} and V_{THL} should be determined for each sample. Timing measurement should be done with these samples specific V_{TLH} and V_{THL} thresholds.

8 Simplified application schematic

Table 8. Configuration compatibility of CLT03 series

Symbol	High Side	Low Side
Isolated	Yes	Yes
Non-isolated	Yes	No

Each circuit given in this section is given for 1 channel only.

For each circuit, the test pulse feature is disabled.

In order to activate the test pulse feature, a capacitor must be added between TP and OUTN (see Section 6 Test pulse feature description).

Figure 11. High side - isolated configuration - test pulse not activated

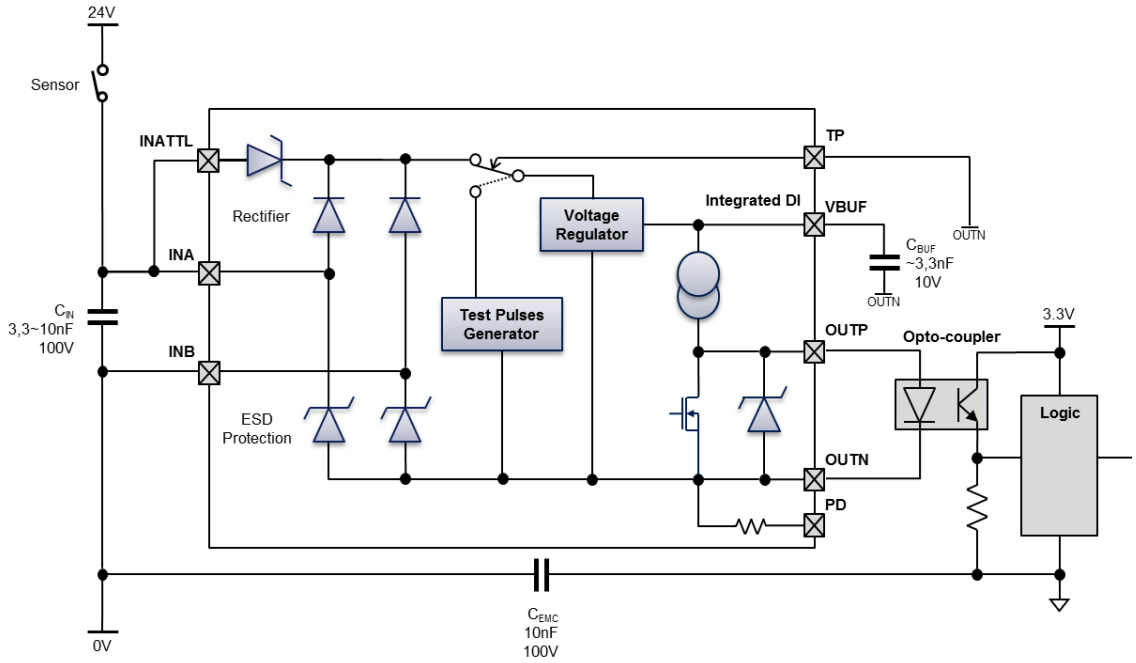


Figure 12. **Low side - isolated configuration - test pulse not activated**

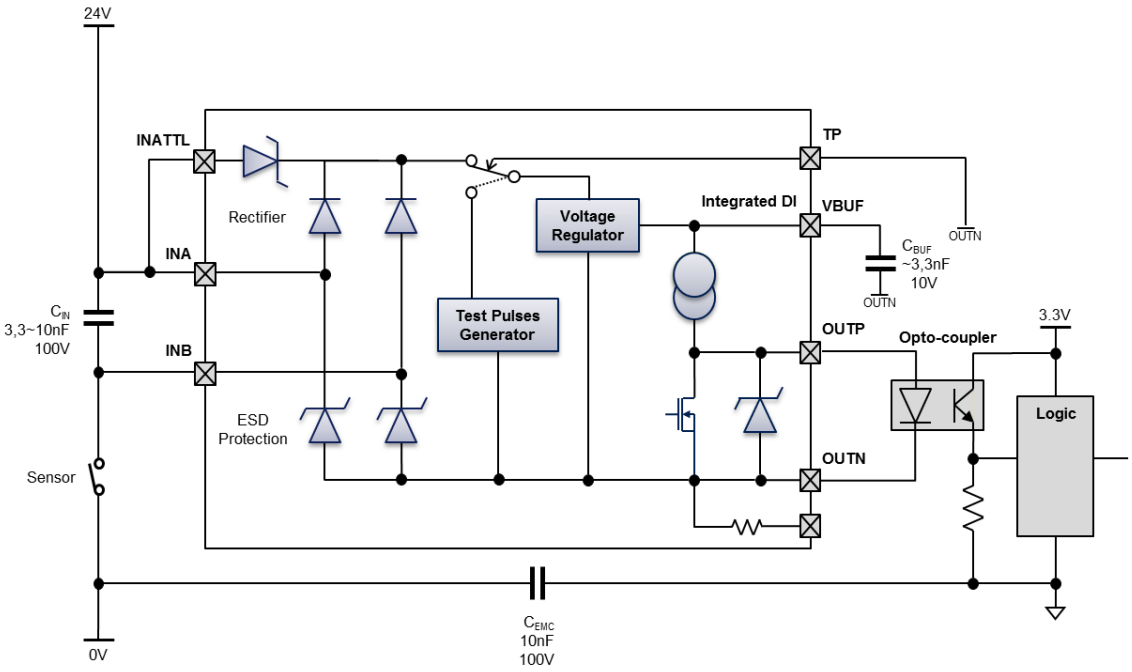
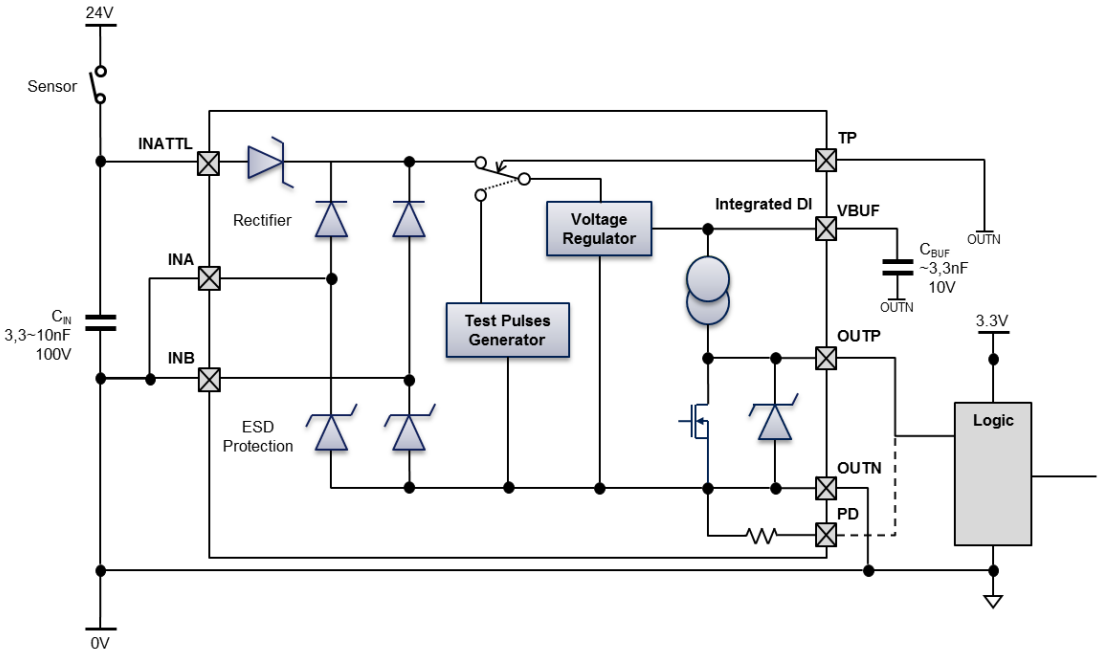


Figure 13. **High side - non-isolated configuration - test pulse not activated**



Note: OUTP to PD connection is optional.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 SOT23-8L 2.9 x 2.8 mm package information

Figure 14. SOT23-8L 2.9 x 2.8 mm package outline

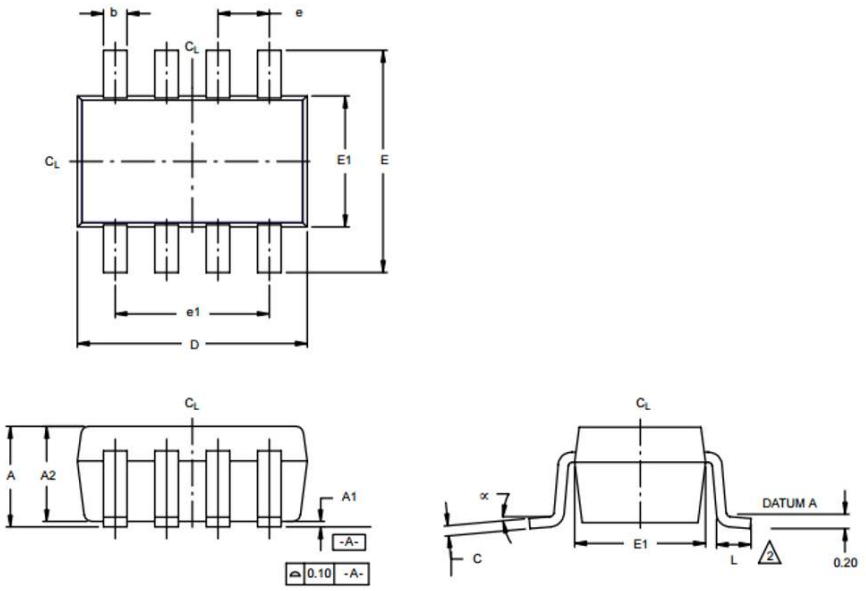


Table 9. SOT23-8L 2.9 x 2.8 mm package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.27	1.45	0.035	0.050	0.057
A1	0.00	0.762	0.15	0.000	0.003	0.006
A2	0.90	1.20	1.30	0.035	0.047	0.051
b	0.22	0.30	0.38	0.009	0.012	0.0115
C	0.09	0.152	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.65	1.75	0.059	0.065	0.069
e		0.65 REF			0.026 REF	
e1		1.95 REF			0.077 REF	
L	0.35	0.45	0.55	0.014	0.018	0.022
a	0°		8°	0°		8°

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 15. Footprint recommendations, dimensions in mm

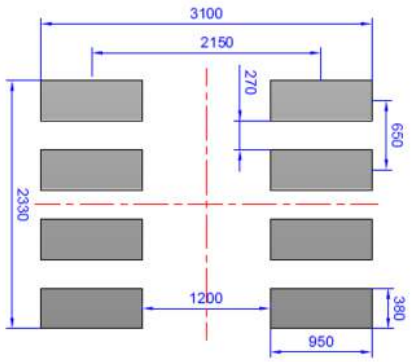
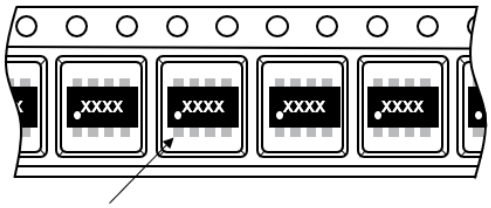


Figure 16. SOT23-8L 2.9 x 2.8 mm marking

XXXX: Marking

refer to ordering information table for marking value

Figure 17. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Figure 18. Tape and reel orientation

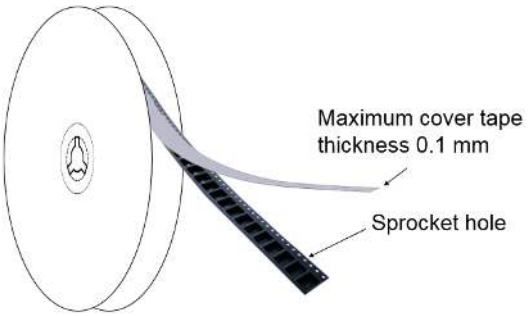


Figure 19. 7" reel dimension values

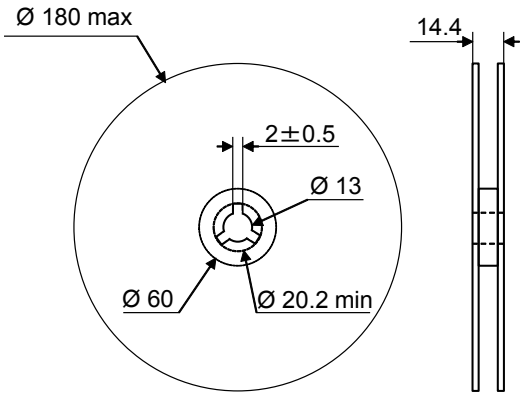


Figure 20. Inner box dimension values

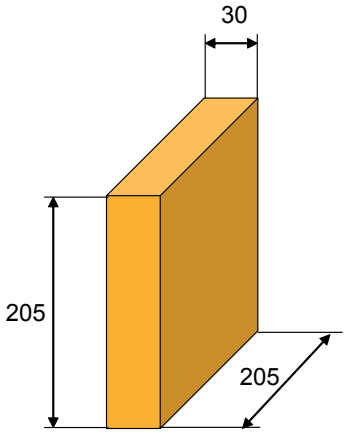
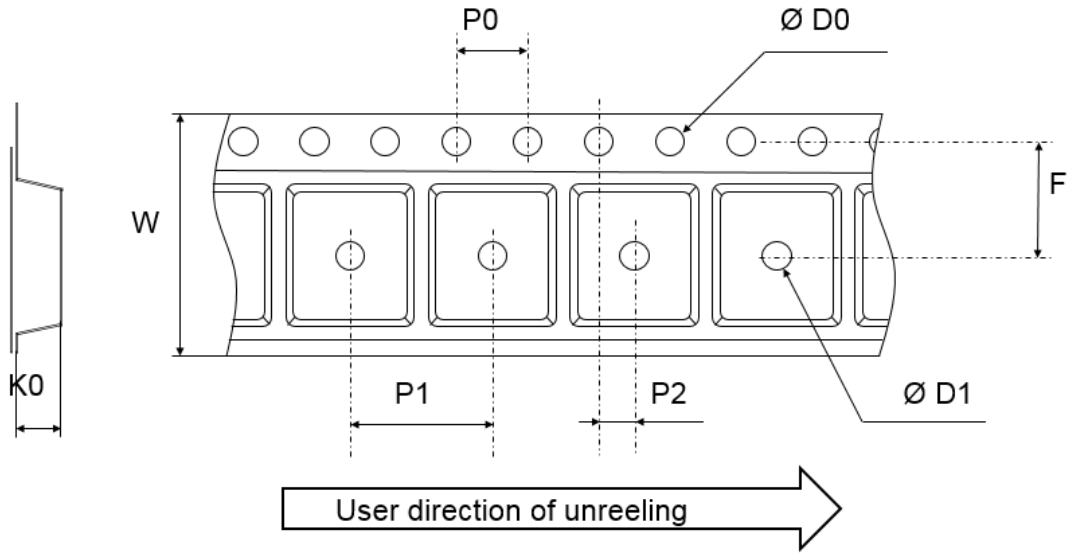


Figure 21. **Tape outline**



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 10. **Tape dimension values**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.45	1.5	1.6
D1	1.00		
F	3.45	3.50	3.55
K0	1.30	1.40	1.50
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

9.2 QFN-16L 4.0 x 2.0 package information

Figure 22. **QFN-16L 4.0 x 2.0 package outline**

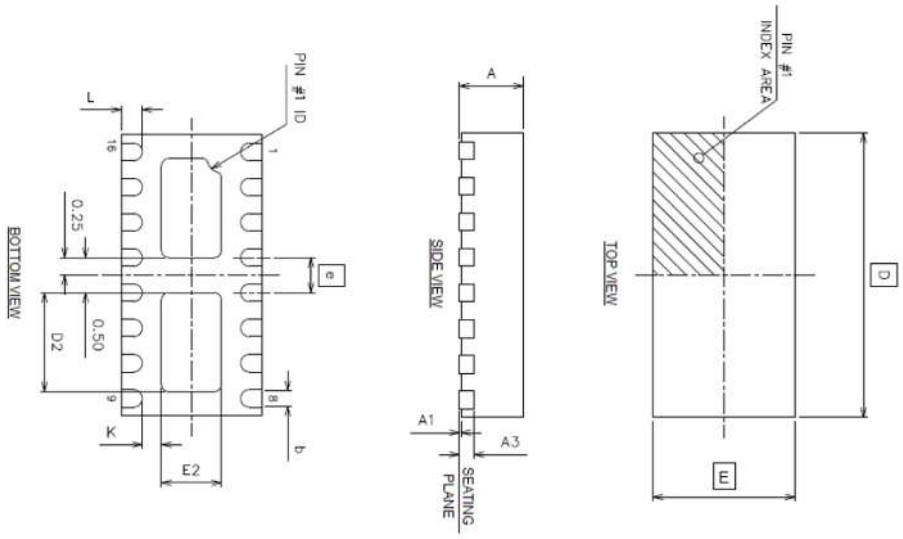


Table 11. **QFN-16L 4.0 x 2.0 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A3		0.20			0.008	
B	0.18	0.25	0.30	0.0071	0.0100	0.0118
D	3.95	4.00	4.05	0.1555	0.1574	0.1594
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D2	1.25	1.40	1.51	0.0492	0.0551	0.0594
E2	0.70	0.85	0.95	0.0276	0.0334	0.0374
e		0.50			0.0197	
K	0.15			0.0059		
L	0.20	0.30	0.40	0.0079	0.0118	0.0157

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 23. Footprint recommendations

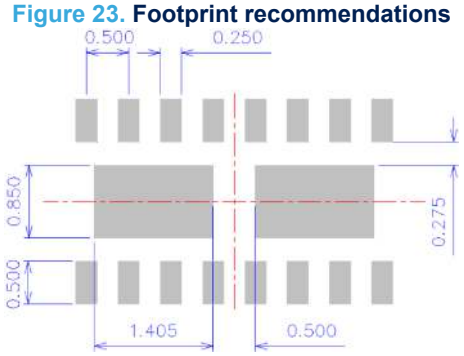
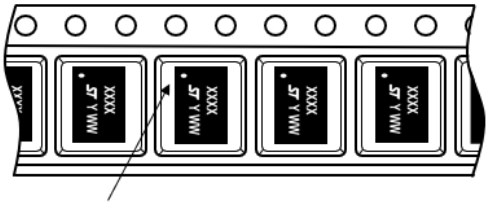


Figure 24. Marking

XXXX: marking
Y WW: date code

refer to ordering information table for marking value

Figure 25. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Figure 26. Tape and reel orientation

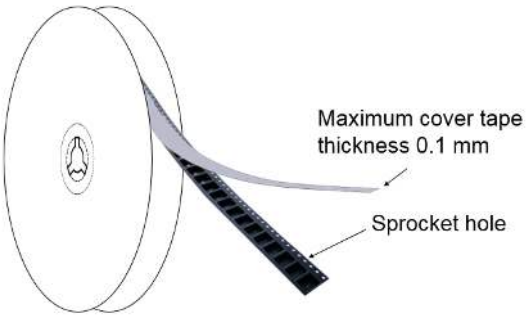


Figure 27. 7" reel dimension values

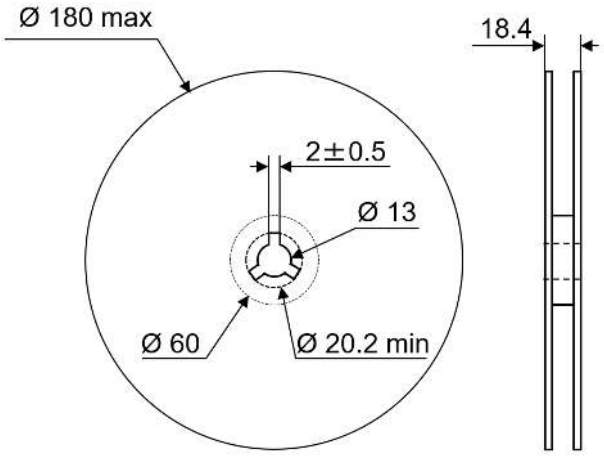


Figure 28. Inner box dimension values

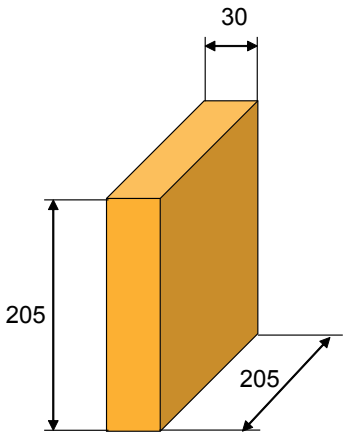
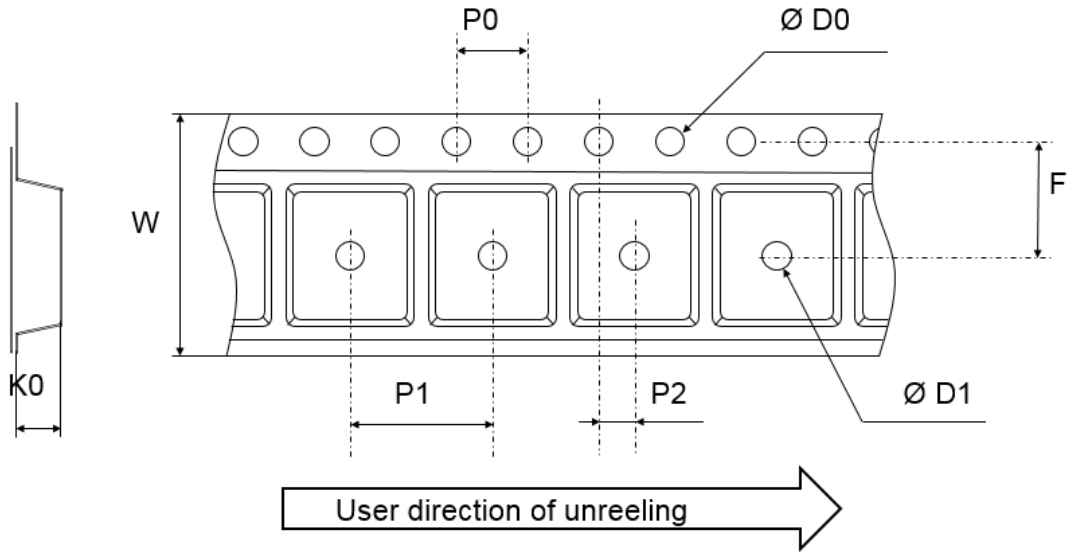


Figure 29. **Tape outline**



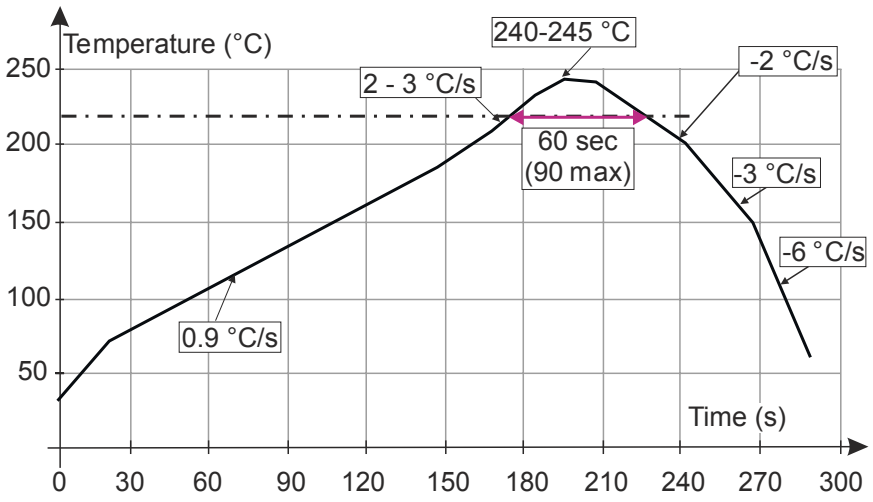
Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 12. **Tape dimension values**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.45	1.5	1.6
D1	1.00		
F	1.65	1.75	1.85
K0	1.10	1.15	1.20
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	11.90	12.00	12.30

10 Reflow profile

Figure 30. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: Maximum soldering profile corresponds to the latest IPC/JEDEC J-ST-020.

11 Ordering information

Figure 31. **Ordering information scheme**

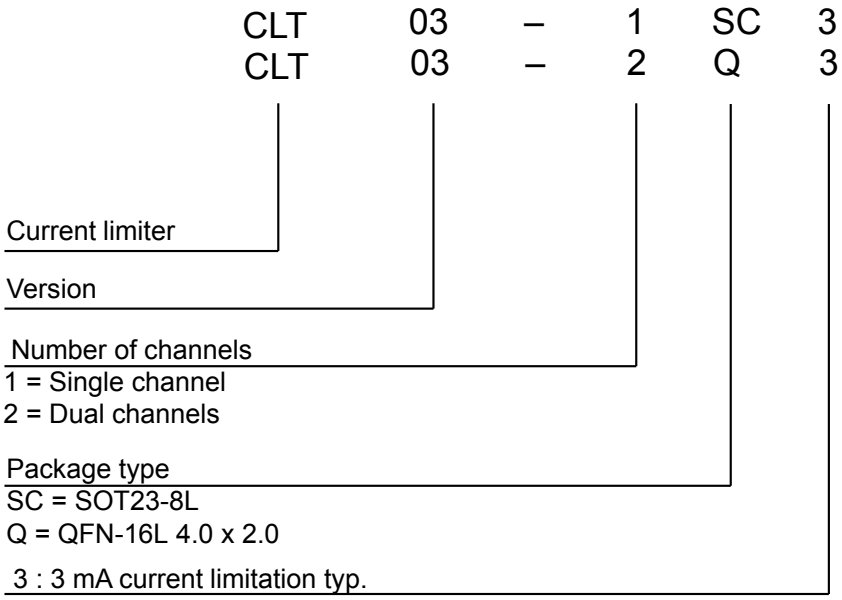


Table 13. **Ordering information**

Order code	Marking[1]	Package	Weight	Base qty.	Delivery mode
CLT03-1SC3	1SC3	SOT23-8L	18 mg	3000	Tape and reel
CLT03-2Q3	CLT03	QFN-16L 4.0 x 2.0	20 mg	3000	Tape and reel

1. *The marking can be rotated to differentiate assembly location*

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
18-Dec-2017	1	Initial release.
11-Dec-2018	2	Minor text change to improve readability.
23-Dec-2019	3	Updated Section Features, Table 4. Electrical characteristics (-30 °C < Tj < +125 °C, unless otherwise specified) (values), Section 8 Simplified application schematic and Figure 6. Test Pulse parameters description. Added Table 2. Thermal resistance parameter and Section 5 Deglitch filter.
06-Feb-2020	4	Updated Table 4. Electrical characteristics (-30 °C < Tj < +125 °C, unless otherwise specified) (values) and Figure 4. Output U-I operation..
04-Mar-2020	5	Updated Section Features, *Section 2.2 Absolute ratings* and *Section 2.3 Electrical characteristics*.
02-Dec-2020	6	Inserted SOT23-8L package information. Minor text change to improve readability.
18-Dec-2020	7	Updated Features and *Figure 24*.
12-Jan-2021	8	Updated Section 6 Test pulse feature description and SOT23-8L name.
06-Apr-2021	9	Updated Figure 7 and Figure 13.
19-Jul-2021	10	Updated Table 5 and Figure 4.
06-Oct-2021	11	Updated Figure 4 and added Table 6.
11-Oct-2021	12	Updated Product status link on cover page.
25-Nov-2022	13	Updated Table 4. Thermal resistance parameter.