19-2861; Rev 3; 2/07

EVALUATION KIT AVAILABLE

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

General Description

The MAX1540A/MAX1541 dual pulse-width modulation (PWM) controllers provide the high efficiency, excellent transient response, and high DC-output accuracy necessary for stepping down high-voltage batteries to generate low-voltage chipset and RAM power supplies in notebook computers.

The Maxim proprietary Quick-PWM™ controllers are free running, constant on-time with input feed forward. This configuration provides ultra-fast transient response, wide input-output (I/O) differential range, low supply current, and tight load-regulation characteristics. The controllers can accurately sense the inductor current across an external current-sense resistor in series with the output to ensure reliable overload and inductor saturation protection. Alternatively, the controllers can use the synchronous rectifier itself or lossless inductor current-sensing methods to provide overload protection with lower power dissipation.

For a single step-down PWM controller with inductor-saturation protection, external-reference input voltage, and dynamically selectable output voltages, refer to the MAX1992/MAX1993 data sheet.

Applications

Notebook Computers

Core/I/O Supplies as Low as 0.7V

0.7V to 5.5V Supply Rails

CPU/Chipset/GPU with Dynamic Voltage Core Supplies (MAX1541)

DDR Memory Termination (MAX1541)

Active Termination Buses (MAX1541)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX1540AETJ	-40°C to +85°C	32 Thin QFN 5mm x 5mm	T3255-4
MAX1540AETJ+	-40°C to +85°C	32 Thin QFN 5mm x 5mm	T3255-4
MAX1541ETL	-40°C to +85°C	40 Thin QFN 6mm x 6mm	T4066-5
MAX1541ETL+	-40°C to +85°C	40 Thin QFN 6mm x 6mm	T4066-5

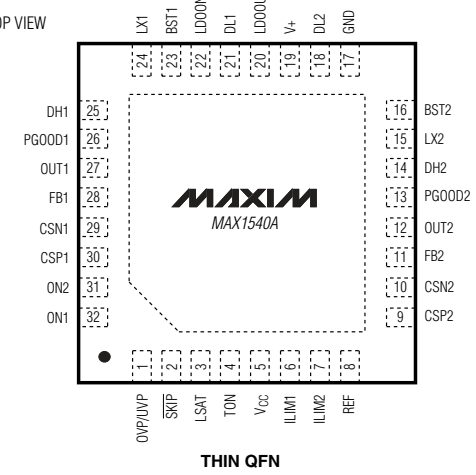
+Denotes a lead-free package.

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- **Inductor-Saturation Protection**
- **Accurate Differential Current-Sense Inputs**
- **Dual Ultra-High-Efficiency Quick-PWMs with 100ns Load-Step Response**
- **MAX1540A**
  - **1.8V/1.2V Fixed or 0.7V to 5.5V Adjustable Output (OUT1)**
  - **2.5V/1.5V Fixed or 0.7V to 5.5V Adjustable Output (OUT2)**
  - **Fixed 5V, 100mA Linear Regulator**
- **MAX1541**
  - **External Reference Input (REFIN1)**
  - **Dynamically Selectable Output Voltage—0.7V to 5.5V (OUT1)**
  - **2.5V/1.8V Fixed or 0.7V to 5.5V Adjustable Output (OUT2)**
  - **Optional Power-Good and Fault Blanking During Transitions**
  - **Fixed 5V or Adjustable 100mA Linear Regulator**
- **1% V_{OUT} Accuracy over Line and Load**
- **2V to 28V Battery Input Range**
- **170kHz to 620kHz Selectable Switching Frequency**
- **Overvoltage/Undervoltage-Protection Option**
- **1.7ms Digital Soft-Start**
- **Drives Large Synchronous-Rectifier FETs**
- **2V ±0.7% Reference Output**
- **Separate Power-Good Window Comparators**

Pin Configurations



Pin Configurations continued at end of data sheet.

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

ABSOLUTE MAXIMUM RATINGS

V+, LDOON to GND .....-0.3V to +28V
LDOOUT to GND (MAX1540A, Note 1).....-0.3V to +6V
LDOOUT to GND (MAX1541, Note 1) .....-0.3V to +28V
V_{DD} to GND (MAX1541, Note 1) .....-0.3V to +6V
V_{CC}, ON_ to GND.....-0.3V to +6V
$\overline{SKIP}$, PGOOD_ to GND.....-0.3V to +6V
FB_, CSP_, ILIM_ to GND.....-0.3V to +6V
TON, OVP/UVP, LSAT to GND .....-0.3V to (V_{CC} + 0.3V)
REF, OUT_ to GND.....-0.3V to (V_{CC} + 0.3V)
LDOIN to GND (MAX1541).....-0.3V to +28V
REFIN1, GATE, OD, FBLDO to GND (MAX1541).....-0.3V to +6V
FBLANK, CC1 to GND (MAX1541).....-0.3V to (V_{CC} + 0.3V)
DL_ to GND (Note 1) .....-0.3V to (V_{DD} + 0.3V)
CSN_ to GND .....-2V to +30V
DH_ to LX_.....-0.3V to (BST + 0.3V)
LX_ to GND.....-2V to +30V
BST_ to LX_ .....-0.3V to +6V
REF Short Circuit to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
32-Pin 5mm x 5mm Thin QFN (derated 21.3mW/°C above +70°C).....1702mW
40-Pin 6mm x 6mm Thin QFN (derated 26.3mW/°C above +70°C).....2105mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: For the MAX1540A, the gate-driver input supply (V_{DD}) is internally connected to the fixed 5V linear-regulator output (LDOOUT), and the linear-regulator input supply (LDOIN) is internally connected to the battery voltage input (V+).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES (Note 1)						
Input Voltage Range	V_{IN}	MAX1540A: battery voltage, V+ > V_{LDOOUT}	5.5		28	V
		MAX1541: battery voltage, V+ > V_{LDOOUT}	2		28	
	V_{BIAS}	V_{CC}, V_{DD} (MAX1541)	4.5		5.5	
	V_{LDOIN}	MAX1541: LDO input supply, V_{LDOIN} > V_{LDOOUT}	4.5		28	
Quiescent Supply Current (V_{CC})	I_{CC}	FB1 and FB2 forced above the regulation point, LSAT = GND		0.7	1.5	mA
		FB1 and FB2 forced above the regulation point, ON1 or ON2 = V_{CC}, V_{LSAT} > 0.5V			1.8	
Quiescent Supply Current (V_{DD}, MAX1541 Only)	I_{DD}	FB1 and FB2 forced above the regulation point, ON1 or ON2 = V_{CC}		<1	5	µA
Quiescent Supply Current (V+)	I_{V+}	MAX1540A: FB1 and FB2 forced above the regulation point, ON1 or ON2 = V_{CC}, V_{LDOON} = V+ = 28V			150	µA
		MAX1541: ON1 or ON2 = V_{CC}, V_{LDOON} = V+ = 28V		25	40	
Quiescent Supply Current (LDOIN, MAX1541 Only)	I_{LDOIN}	FB1 and FB2 forced above the regulation point, ON1 or ON2 = V_{CC}, V_{LDOON} = V+ = 28V			110	µA
Standby Supply Current (V_{CC})		ON1 = ON2 = GND, V_{LDOON} = V+ = 28V		<1	5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Standby Supply Current (V_{DD}, MAX1541 Only)		ON1 = ON2 = GND, V_{LDOON} = V+ = 28V			<1	5	µA
Standby Supply Current (V+)		MAX1540A: ON1 = ON2 = GND, LDOON = V+ = 28V, V_{CC} = 0 or 5V				105	µA
		MAX1541: ON1 = ON2 = GND, LDOON = V+ = 28V, V_{CC} = V_{DD} = 0 or 5V			<1	5	
Standby Supply Current (LDOIN, MAX1541 Only)		ON1 = ON2 = GND, V_{LDOON} = V+ = 28V				100	µA
Shutdown Supply Current (V_{CC})		ON1 = ON2 = LDOON = GND			<1	5	µA
Shutdown Supply Current (V_{DD}, MAX1541 Only)		ON1 = ON2 = LDOON = GND			<1	5	µA
Shutdown Supply Current (V+)		MAX1540A: ON1 = ON2 = LDOON = GND, V+ = 28V, V_{CC} = 0 or 5V			4	15	µA
		MAX1541: ON1 = ON2 = LDOON = GND, V+ = 28V, V_{CC} = V_{DD} = 0 or 5V			<1	5	
Shutdown Supply Current (LDOIN, MAX1541 Only)		LDOON = GND			4	10	µA
PWM CONTROLLERS							
MAX1540A Main Output-Voltage Accuracy (OUT1) (Note 2)	V_{OUT1}	Preset output, V+ = 5.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB1 = GND	1.782	1.80	1.818	V
			FB1 = V_{CC}	1.188	1.20	1.212	
	V_{FB1}	Adjustable output, V+ = 5.5V to 28V, $\overline{SKIP}$ = V_{CC}		0.693	0.70	0.707	
MAX1540A Secondary Output-Voltage Accuracy (OUT2) (Note 2)	V_{OUT2}	Preset output, V+ = 5.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB2 = GND	2.475	2.50	2.525	V
			FB2 = V_{CC}	1.485	1.50	1.515	
	V_{FB2}	Adjustable output, V+ = 5.5V to 28V, $\overline{SKIP}$ = V_{CC}		0.693	0.70	0.707	
MAX1541 Main Feedback-Voltage Accuracy (FB1)	V_{FB1}	V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}	REFIN1 = 0.35 x REF	0.693	0.70	0.707	V
MAX1541 Secondary Output-Voltage Accuracy (OUT2) (Note 2)	V_{OUT2}	Preset output, V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB2 = GND	2.475	2.50	2.525	V
			FB2 = V_{CC}	1.782	1.80	1.818	
	V_{FB2}	Adjustable output, V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}		0.693	0.70	0.707	
Load-Regulation Error		I_{LOAD} = 0 to 3A, $\overline{SKIP}$ = V_{CC}			0.1		%
Line-Regulation Error		V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			0.25		%
FB_ Input Bias Current	$I_{FB\_}$			-0.1		+0.1	µA
Output Adjust Range				0.7		5.5	V

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT_ Input Resistance	$R_{OUT\_}$	MAX1540A	FB_ = GND	70	145	350	kΩ
			FB_ = V_{CC} or adjustable	50	115	220	
		MAX1541	FB1 = OUT1	400	700	1500	
			FB2 = GND	90	170	350	
			FB2 = V_{CC} or adjustable	60	130	270	
OUT_ Discharge Mode On-Resistance	$R_{DISCHARGE}$				10	25	Ω
OUT_ Synchronous-Rectifier Discharge-Mode Turn-On Level				0.2	0.3	0.4	V
Soft-Start Ramp Time	t_{SS}	Rising edge on ON_ to full current limit			1.7		ms
DH1 On-Time	t_{ON1}	V+ = 15V, V_{OUT1} = 1.5V (Note 3)	TON = GND (620kHz)	149	169	190	ns
			TON = REF (485kHz)	191	216	242	
			TON = open (345kHz)	274	304	335	
			TON = V_{CC} (235kHz)	402	447	491	
DH2 On-Time	t_{ON2}	V+ = 15V, V_{OUT2} = 1.5V (Note 3)	TON = GND (460kHz)	201	228	256	ns
			TON = REF (355kHz)	260	296	331	
			TON = open (255kHz)	371	412	453	
			TON = V_{CC} (170kHz)	556	618	679	
On-Time Tracking		t_{ON2} with respect to t_{ON1} (Note 3)		120	135	150	%
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)			400	500	ns
LINEAR REGULATOR (LDO) (Note 1)							
MAX1540A LDO Output-Voltage Accuracy	V_{LDOOUT}	ON1 = ON2 = GND, V+ = 6V to 28V	0 < I_{LDOOUT} < 10mA	4.85	5.0	5.10	V
			0 < I_{LDOOUT} < 100mA	4.70		5.10	
MAX1541 LDO Output-Voltage Accuracy (Fixed V_{LDOOUT})	V_{LDOOUT}	FBLDO = ON1 = ON2 = GND, V_{LDOIN} = 6V to 28V	0 < I_{LDOOUT} < 10mA	4.85	5.0	5.10	V
			0 < I_{LDOOUT} < 100mA	4.70		5.10	
MAX1541 LDO Feedback Accuracy (Adjustable V_{LDOOUT})	V_{FBLDO}	FBLDO = LDOOUT, ON1 = ON2 = GND, V_{LDOIN} = 4.5V to 28V	0 < I_{LDOOUT} < 10mA	1.212	1.25	1.275	V
			0 < I_{LDOOUT} < 100mA	1.175		1.275	
MAX1541 LDO Output Adjust Range				1.175		24	V
LDOOUT Short-Circuit Current					130		mA
FBLDO Input Bias Current	I_{FBLDO}			-0.1		+0.1	µA
Dropout Voltage		MAX1540A: V+ - V_{LDOOUT}, I_{LDOOUT} = 50mA			500	800	mV
		MAX1541: V_{LDOIN} - V_{LDOOUT}, I_{LDOOUT} = 50mA			500	800	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE (REF)							
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0V	T_A = +25°C to +85°C	1.986	2.00	2.014	V
			T_A = 0°C to +85°C	1.983	2.00	2.017	
Reference Load Regulation	ΔV_{REF}	I_{REF} = -10µA to +50µA		-0.01		+0.01	V
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge, hysteresis = 350mV			1.95		V
REFIN1 (MAX1541) Voltage Range	V_{REFIN}			0.7		V_{REF}	V
REFIN1 (MAX1541) Input Bias Current	I_{REFIN1}				0.01	0.05	µA
FAULT DETECTION							
Overvoltage Trip Threshold		With respect to error-comparator threshold, OVP/UVP = V_{CC}		12	16	20	%
Overvoltage Fault-Propagation Delay	t_{OVP}	FB forced 2% above trip threshold			10		µs
Output Undervoltage-Protection Trip Threshold		With respect to error-comparator threshold, OVP/UVP = V_{CC}		65	70	75	%
Output Undervoltage-Protection Blanking Time	t_{BLANK}	From rising edge of ON_		10		35	ms
Output Undervoltage Fault-Propagation Delay	t_{UVP}				10		µs
PGOOD_ Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		-13	-10	-7	%
PGOOD_ Upper Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		+7	+10	+13	%
PGOOD_ Propagation Delay	$t_{PGOOD\_}$	FB forced 2% beyond PGOOD_ trip threshold			10		µs
PGOOD_ Output Low Voltage		I_{SINK} = 4mA				0.3	V
PGOOD_ Leakage Current	$I_{PGOOD\_}$	FB = REF (PGOOD high impedance), PGOOD forced to 5.5V				1	µA
Fault-Blanking Time (MAX1541 Only)	t_{FBLANK}	FBLANK = V_{CC}		120	220	320	µs
		FBLANK = open		80	140	205	
		FBLANK = REF		35	65	95	
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 10°C	LDOON = V_{CC}		+150		°C
			LDOON = GND		+160		
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level, hysteresis = 20mV		4.1	4.25	4.4	V
CURRENT LIMIT							
ILIM_ Adjustment Range				0.25		2	V
Current-Limit Input Range		CSP_		0		2.7	V
		CSN_		-0.3		+28	
CSP_/CSN_ Input Current						0.5	µA

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold (Fixed)	$V_{LIM\_ (VAL)}$	$V_{CSP\_}$ - $V_{CSN\_}$, ILIM_ = V_{CC}		45	50	55	mV
Valley Current-Limit Threshold (Adjustable)	$V_{LIM\_ (VAL)}$	$V_{CSP\_}$ - $V_{CSN\_}$	$V_{ILIM\_}$ = 250mV	15	25	35	mV
			$V_{ILIM\_}$ = 2.00V	170	200	230	
Current-Limit Threshold (Negative)	V_{NEG}	$V_{CSP\_}$ - $V_{CSN\_}$, $\overline{SKIP}$ = ILIM_ = V_{CC}, T_A = +25°C		-90	-65	-45	mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	With respect to valley current-limit threshold, $V_{CSP\_}$ - $V_{CSN\_}$, $\overline{SKIP}$ = GND, ILIM_ = V_{CC}			2.5		mV
Inductor-Saturation Current-Limit Threshold		With respect to valley current-limit threshold, ILIM_ = V_{CC}	LSAT = V_{CC}	180	200	220	%
			LSAT = open	157	175	193	
			LSAT = REF	135	150	165	
ILIM_ Saturation Fault Sink Current	$I_{ILIM\_ (LSAT)}$	V_{CSP} - V_{CSN} > inductor saturation current limit, 0.25V < $V_{ILIM\_}$ < 2.0V		4	6	8	µA
ILIM_ Leakage Current		$V_{CSP\_}$ - $V_{CSN\_}$ < inductor saturation current limit				0.1	µA
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	R_{DH}	BST_-LX_ forced to 5V			1.5	5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state			1.5	5	Ω
		DL_, low state			0.6	3	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_-LX_ forced to 5V			1		A
DL_ Gate-Driver Source Current	I_{DL} (SOURCE)	DL_ forced to 2.5V			1		A
DL_ Gate-Driver Sink Current	$I_{DL (SINK)}$	DL_ forced to 2.5V			3		A
Dead Time	t_{DEAD}	DL_ rising			35		ns
		DH_ rising			26		
INPUTS AND OUTPUTS							
OD On-Resistance	R_{OD}	GATE = V_{CC}			10	25	Ω
OD Leakage Current		GATE = GND, OD forced to 5.5V			1	200	nA
Logic Input Threshold		ON1, ON2, $\overline{SKIP}$, GATE rising edge, hysteresis = 225mV		1.2	1.7	2.2	V
LDOON Input Trip Level		Rising edge, hysteresis = 250mV		1.20	1.25	1.30	V
Logic Input Current		ON1, ON2, LDOON, $\overline{SKIP}$, GATE		-1		+1	µA
Dual Mode™ Threshold Voltage		FB1 (MAX1540A), FB2 (MAX1540A/MAX1541)	High	1.9	2.0	2.1	V
			Low	0.05	0.1	0.15	

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Four-Level Input Logic Levels		TON, OVP/UVP, LSAT, $\overline{SKIP}$, FBLANK	High	V_{CC} - 0.4V			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.5	
Four-Level Logic Input Current		TON, OVP/UVP, LSAT, $\overline{SKIP}$, FBLANK forced to GND or V_{CC}		-3		+3	µA

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
INPUT SUPPLIES (Note 1)					
Input Voltage Range	V_{IN}	MAX1540A: battery voltage, V+ > V_{LDOOUT}	5.5	28	V
		MAX1541: battery voltage, V+ > V_{LDOOUT}	2	28	
	V_{BIAS}	V_{CC}, V_{DD} (MAX1541)	4.5	5.5	
	V_{LDOIN}	MAX1541: LDO input supply, V_{LDOIN} > V_{LDOOUT}	4.5	28	
Quiescent Supply Current (V_{CC})	I_{CC}	FB1 and FB2 forced above the regulation point, LSAT = GND		1.5	mA
		FB1 and FB2 forced above the regulation point, ON1 or ON2 = V_{CC}, V_{LSAT} > 0.5V		1.8	
Quiescent Supply Current (V_{DD}, MAX1541 Only)	I_{DD}	FB1 and FB2 forced above the regulation point, ON1 or ON2 = V_{CC}		5	µA
Quiescent Supply Current (V+)	I_{V+}	MAX1540A: FB1 and FB2 forced above the regulation point, ON1 or ON2 = V_{CC}, V_{LDOON} = V+ = 28V		150	µA
		MAX1541: ON1 or ON2 = V_{CC}, V_{LDOON} = V+ = 28V		40	
Quiescent Supply Current (LDOIN, MAX1541 Only)	I_{LDOIN}	FB1 and FB2 forced above the regulation point, ON1 or ON2 = V_{CC}, V_{LDOON} = V+ = 28V		110	µA
Standby Supply Current (V_{DD})		ON1 = ON2 = GND, V_{LDOON} = V+ = 28V		5	µA
Standby Supply Current (V_{DD}, MAX1541 Only)		ON1 = ON2 = GND, V_{LDOON} = V+ = 28V		5	µA
Standby Supply Current (V+)		MAX1540A: ON1 = ON2 = GND, LDOON = V+ = 28V, V_{CC} = 0 or 5V		105	µA
		MAX1541: ON1 = ON2 = GND, LDOON = V+ = 28V, V_{CC} = V_{DD} = 0 or 5V		5	
Standby Supply Current (LDOIN, MAX1541 Only)		ON1 = ON2 = GND, V_{LDOON} = V+ = 28V		100	µA

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Shutdown Supply Current (V_{CC})		ON1 = ON2 = LDOON = GND			5	µA
Shutdown Supply Current (V_{DD}, MAX1541 Only)		ON1 = ON2 = LDOON = GND			5	µA
Shutdown Supply Current (V+)		MAX1540A: ON1 = ON2 = LDOON = GND, V+ = 28V, V_{CC} = 0 or 5V			15	µA
		MAX1541: ON1 = ON2 = LDOON = GND, V+ = 28V, V_{CC} = V_{DD} = 0 or 5V			5	
Shutdown Supply Current (LDOIN, MAX1541 Only)		LDOON = GND			10	µA
PWM CONTROLLERS						
MAX1540A Main Output-Voltage Accuracy (OUT1) (Note 2)	V_{OUT1}	Preset output, V+ = 5.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB1 = GND	1.773	1.827	V
			FB1 = V_{CC}	1.182	1.218	
	V_{FB1}	Adjustable output, V+ = 5.5V to 28V, $\overline{SKIP}$ = V_{CC}		0.689	0.711	
MAX1540A Secondary Output-Voltage Accuracy (OUT2) (Note 2)	V_{OUT2}	Preset output, V+ = 5.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB2 = GND	2.462	2.538	V
			FB2 = V_{CC}	1.477	1.523	
	V_{FB2}	Adjustable output, V+ = 5.5V to 28V, $\overline{SKIP}$ = V_{CC}		0.689	0.711	
MAX1541 Main Feedback Voltage Accuracy (FB1)	V_{FB1}	V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}	REFIN1 = 0.35 x REF	0.689	0.711	V
			REFIN1 = REF	1.97	2.03	
MAX1541 Secondary Output-Voltage Accuracy (OUT2) (Note 2)	V_{OUT2}	Preset output, V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB2 = GND	2.462	2.538	V
			FB2 = V_{CC}	1.773	1.827	
	V_{FB2}	Adjustable output, V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}		0.689	0.711	
DH1 On-Time (Note 3)	t_{ON1}	V+ = 15V, V_{OUT1} = 1.5V	TON = GND (620kHz)	149	190	ns
			TON = REF (485kHz)	191	242	
			TON = open (345kHz)	274	335	
			TON = V_{CC} (235kHz)	402	491	
DH2 On-Time (Note 3)	t_{ON2}	V+ = 15V, V_{OUT2} = 1.5V	TON = GND (460kHz)	201	256	ns
			TON = REF (355kHz)	260	331	
			TON = open (255kHz)	371	453	
			TON = V_{CC} (170kHz)	556	679	
On-Time Tracking		t_{ON2} with respect to t_{ON1} (Note 3)		118	152	%
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)			500	ns
LINEAR REGULATOR (LDO) (Note 1)						
MAX1540A LDO Output-Voltage Accuracy	V_{LDOOUT}	ON1 = ON2 = GND, V+ = 6V to 28V	0 < I_{LDOOUT} < 10mA	4.85	5.10	V
			0 < I_{LDOOUT} < 100mA	4.65	5.10	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
MAX1541 LDO Output-Voltage Accuracy (Fixed V_{LDOOUT})	V_{LDOOUT}	FBLDO = ON1 = ON2 = GND, V_{LDOIN} = 6V to 28V	0 < I_{LDOOUT} < 10mA	4.85	5.10	V
			0 < I_{LDOOUT} < 100mA	4.65	5.10	
MAX1541 LDO Feedback Accuracy (Adjustable V_{LDOOUT})	V_{FBLDO}	FBLDO = LDOOUT, ON1 = ON2 = GND, V_{LDOIN} = 4.5V to 28V	0 < I_{LDOOUT} < 10mA	1.212	1.275	V
			0 < I_{LDOOUT} < 100mA	1.175	1.275	
Dropout Voltage		MAX1540A: V+ - V_{LDOOUT}, I_{LDOOUT} = 50mA			800	mV
		MAX1541: V_{LDOIN} - V_{LDOOUT}, I_{LDOOUT} = 50mA			800	
REFERENCE (REF)						
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.98	2.02	V
REFIN1 Input Bias Current	I_{REFIN1}				0.05	µA
FAULT DETECTION						
Overvoltage Trip Threshold		With respect to error-comparator threshold, OVP/UVP = V_{CC}		10	21	%
Output Undervoltage-Protection Trip Threshold		With respect to error-comparator threshold, OVP/UVP = V_{CC}		64	76	%
PGOOD_ Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		-14	-5	%
PGOOD_ Upper Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		+5	+14	%
PGOOD_ Output Low Voltage		I_{SINK} = 4mA			0.3	V
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level, hysteresis = 20mV		4.1	4.4	V
CURRENT LIMIT						
Current-Limit Input Range		CSP_		0	2.7	V
		CSN_		-0.3	+28.0	
Valley Current-Limit Threshold (Fixed)	$V_{LIM\_(VAL)}$	$V_{CSP\_}$ - $V_{CSN\_}$, ILIM_ = V_{CC}		40	60	mV
Valley Current-Limit Threshold (Adjustable)	$V_{LIM\_(VAL)}$	$V_{CSP\_}$ - $V_{CSN\_}$, $V_{ILIM\_}$ = 2.00V		160	240	mV
INPUTS AND OUTPUTS						
Logic Input Threshold		ON1, ON2, $\overline{SKIP}$, GATE, rising edge, hysteresis = 225mV		1.2	2.2	V
LDOON Input Trip Level		Rising edge, hysteresis = 250mV		1.2	1.3	V
Dual Mode Threshold Voltage		FB1 (MAX1540A), FB2 (MAX1540A/MAX1541)	High	1.9	2.1	V
			Low	0.05	0.15	

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V_{CC} = V_{DD} = ON1 = ON2 = 5V, $\overline{SKIP}$ = GND, LDOIN (MAX1541) = V+, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Four-Level Input Logic Levels		TON, OVP/UVP, LSAT, $\overline{SKIP}$, FBLANK	High	V_{CC} - 0.4V		V
			Open	3.15	3.85	
			REF	1.65	2.35	
			Low		0.5	

Note 1: For the MAX1540A, the gate-driver input supply (V_{DD}) is internally connected to the fixed 5V linear-regulator output (LDOOUT),
and the linear-regulator input supply (LDOIN) is internally connected to the battery voltage input (V+).

Note 2: When the inductor is in continuous conduction, the output voltage has a DC regulation level higher than the error-comparator threshold by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light load), the output voltage has a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.

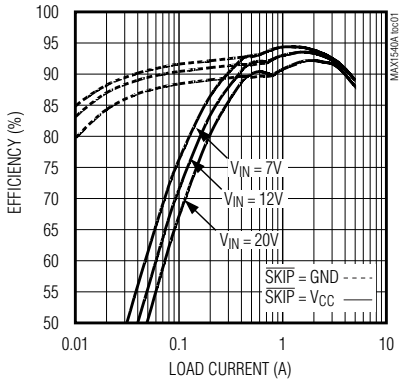
Note 3: On-time and off-time specifications are measured from 50% point to 50% point at the DH_ pin with LX_ = GND, VBST_ = 5V, and a 250pF capacitor connected from DH_ to LX_. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 4: Specifications to -40°C are guaranteed by design, not production tested.

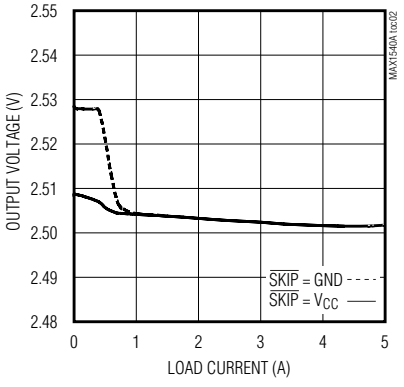
Typical Operating Characteristics

(MAX1541 circuit of Figure 12, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, TON = REF, T_A = +25°C, unless otherwise noted.)

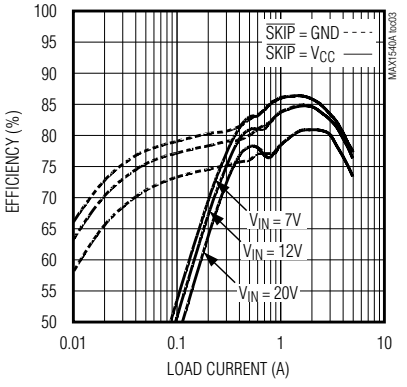
OUT2 EFFICIENCY vs. LOAD CURRENT (V_{OUT2} = 2.5V)



2.5V OUTPUT VOLTAGE (OUT2) vs. LOAD CURRENT



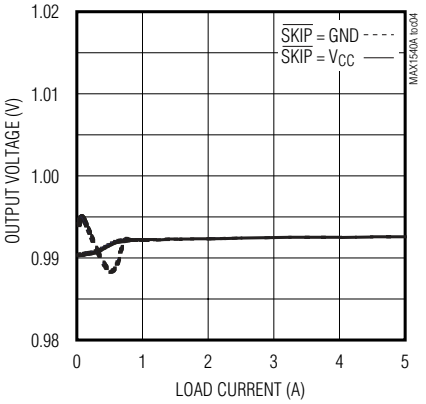
OUT1 EFFICIENCY vs. LOAD CURRENT (V_{OUT1} = 1.0V)



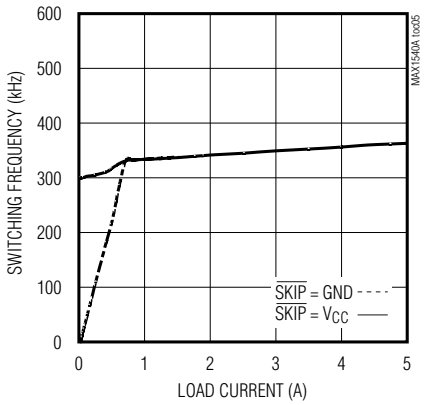
Typical Operating Characteristics (continued)

(MAX1541 circuit of Figure 12, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, TON = REF, T_A = +25°C, unless otherwise noted.)

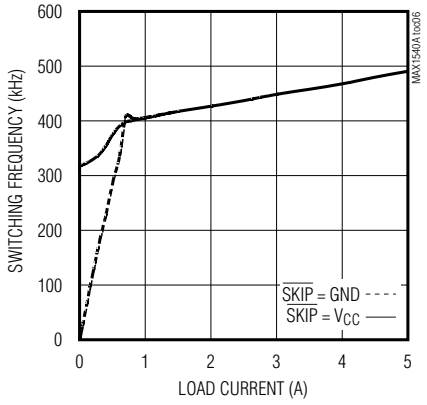
1.0V OUTPUT VOLTAGE (OUT1) vs. LOAD CURRENT



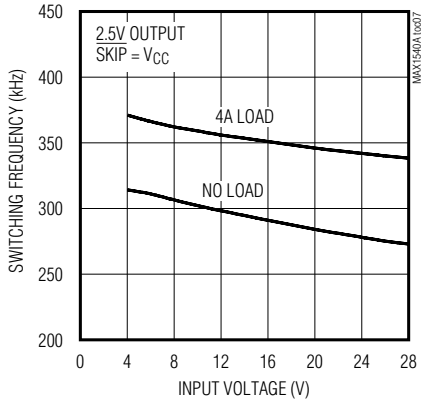
OUT2 SWITCHING FREQUENCY vs. LOAD CURRENT (V_{OUT2} = 2.5V)



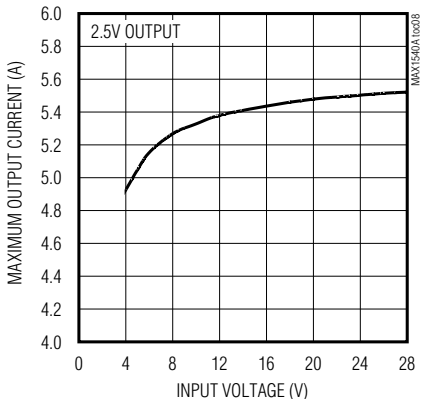
OUT1 SWITCHING FREQUENCY vs. LOAD CURRENT (V_{OUT1} = 1.0V)



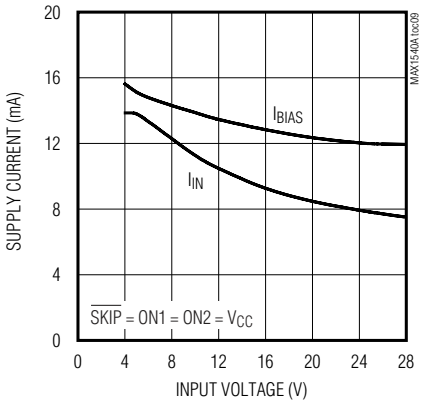
SWITCHING FREQUENCY vs. INPUT VOLTAGE



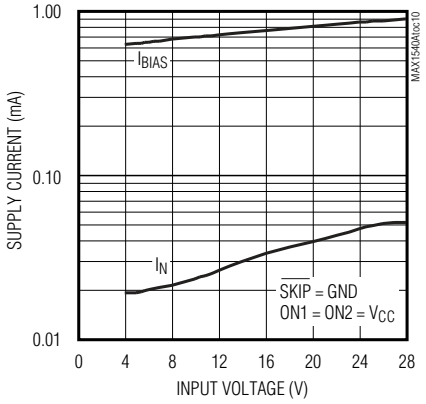
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



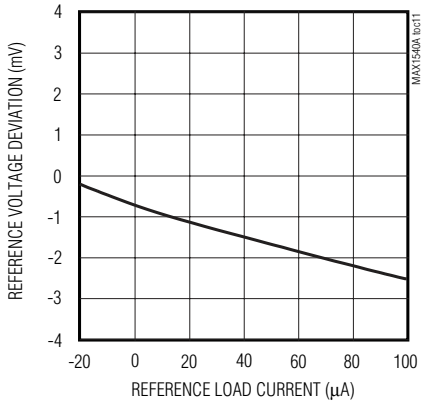
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (FORCED-PWM OPERATION)



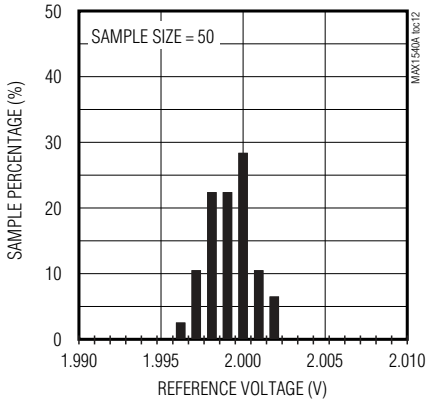
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PULSE-SKIPPING OPERATION)



2.0V REFERENCE LOAD REGULATION



REFERENCE DISTRIBUTION

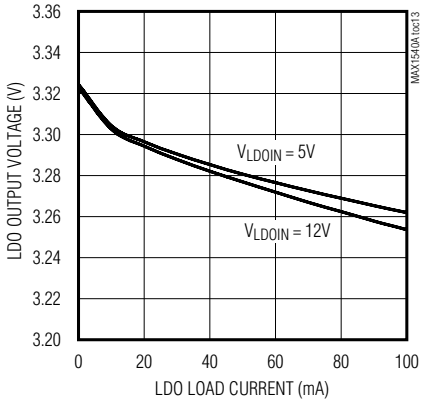


Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

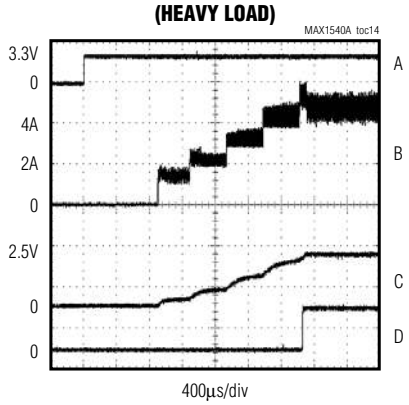
Typical Operating Characteristics (continued)

(MAX1541 circuit of Figure 12, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, TON = REF, T_A = +25°C, unless otherwise noted.)

LINEAR-REGULATOR OUTPUT (LDOOUT) vs. LOAD CURRENT



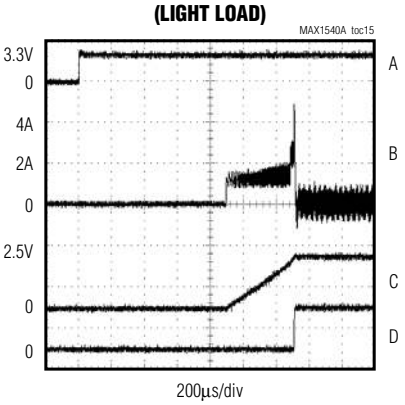
STARTUP WAVEFORM (HEAVY LOAD)



A. ON2, 5V/div
B. INDUCTOR CURRENT, 2A/div
C. OUT2, 2V/div
D. PGOOD2, 5V/div

0.5Ω LOAD

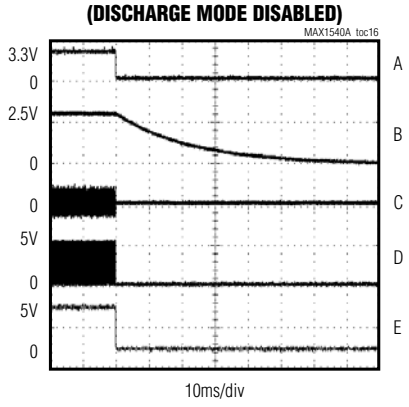
STARTUP WAVEFORM (LIGHT LOAD)



A. ON2, 5V/div
B. INDUCTOR CURRENT, 2A/div
C. OUT2, 2V/div
D. PGOOD2, 5V/div

100Ω LOAD

SHUTDOWN WAVEFORM (DISCHARGE MODE DISABLED)



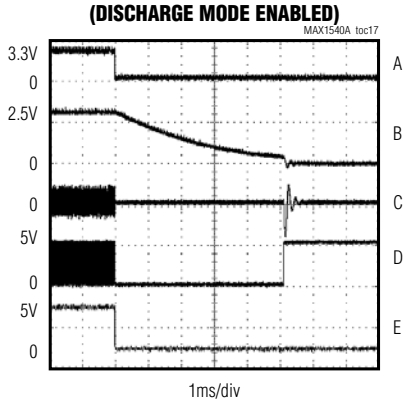
A. ON2, 5V/div
B. OUT2, 2V/div
C. INDUCTOR CURRENT, 2A/div
D. DL2, 5V/div
E. PGOOD2, 5V/div

100Ω LOAD, OVP/UVP = REF OR GND

Typical Operating Characteristics (continued)

(MAX1541 circuit of Figure 12, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, TON = REF, T_A = +25°C, unless otherwise noted.)

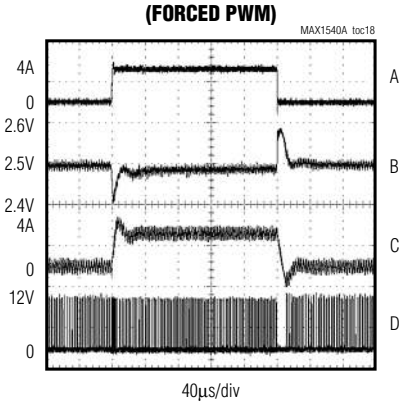
SHUTDOWN WAVEFORM (DISCHARGE MODE ENABLED)



A. ON2, 5V/div
B. OUT2, 2V/div
C. INDUCTOR CURRENT, 2A/div
D. DL2, 5V/div
E. PGOOD2, 5V/div

100Ω LOAD, OVP/UVP = V_{CC} OR OPEN

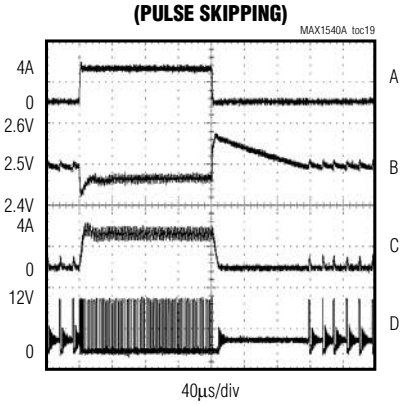
2.5V OUTPUT LOAD TRANSIENT (FORCED PWM)



A. I_{OUT2} = 0 TO 4A, 5A/div
B. V_{OUT2} = 2.5V, 100mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX2, 10V/div

$\overline{SKIP}$ = V_{CC}

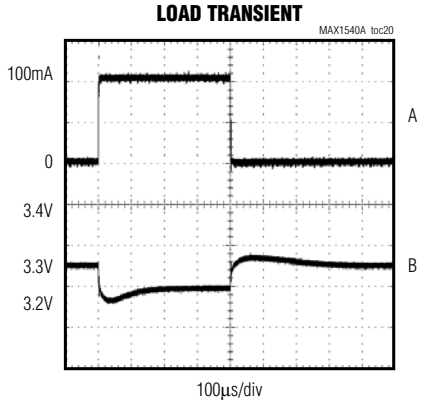
2.5V OUTPUT LOAD TRANSIENT (PULSE SKIPPING)



A. I_{OUT2} = 0.1A TO 4A, 5A/div
B. V_{OUT2} = 2.5V, 100mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX2, 10V/div

$\overline{SKIP}$ = GND

LINEAR-REGULATOR LOAD TRANSIENT



A. I_{LDOOUT} = 1mA TO 100mA, 50mA/div
B. V_{LDOOUT} = 3.3V, 100mV/div

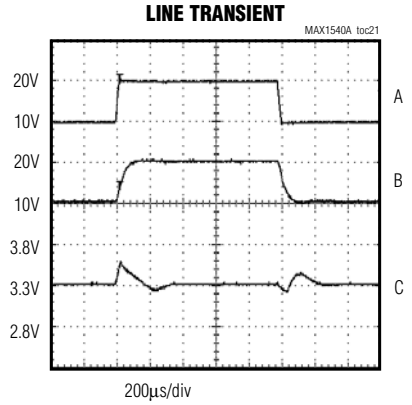
$\overline{SKIP}$ = GND

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Typical Operating Characteristics (continued)

(MAX1541 circuit of Figure 12, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, TON = REF, T_A = +25°C, unless otherwise noted.)

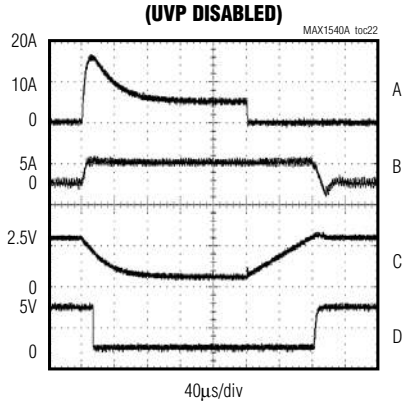
LINEAR-REGULATOR LINE TRANSIENT



A. INPUT (V_{IN}), 10V/div
B. LDOIN (10V TO 20V), 10V/div
C. LDOOUT (3.3V), 500mV/div

20mA LOAD

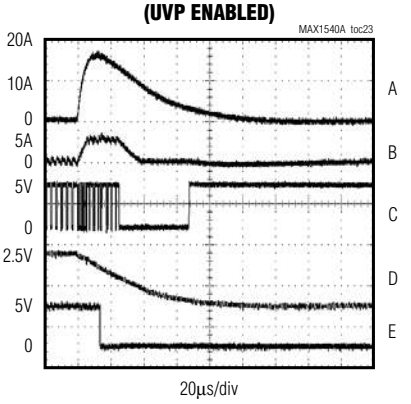
OUTPUT OVERLOAD (UVP DISABLED)



A. LOAD (0 TO 150mΩ), 10A/div
B. INDUCTOR CURRENT, 10A/div
C. 2.5V OUTPUT, 2V/div
D. PGOOD2, 5V/div

OVP/UVP = OPEN OR GND

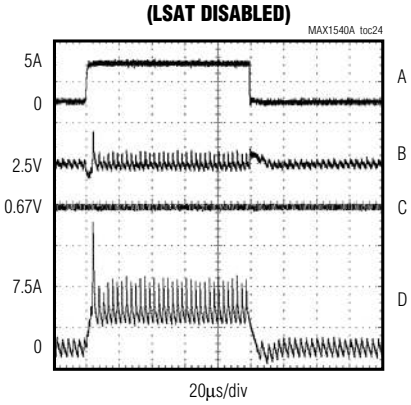
OUTPUT OVERLOAD (UVP ENABLED)



A. LOAD (0 TO 150mΩ), 10A/div
B. INDUCTOR CURRENT, 10A/div
C. DL2, 5V/div
D. 2.5V OUTPUT, 2V/div
E. PGOOD2, 5V/div

OVP/UVP = V_{CC} OR REF

INDUCTOR-SATURATION PROTECTION (LSAT DISABLED)



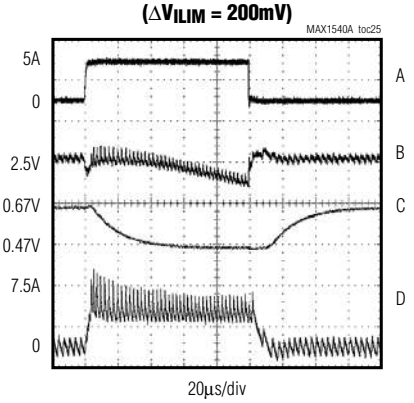
A. I_{OUT2} = 0 TO 5A, 5A/div
B. 2.5V OUTPUT, 200mV/div
C. ILIM, 100mV/div
D. INDUCTOR CURRENT, 5A/div

LSAT = GND, L = 3.3µH 3.5A

Typical Operating Characteristics (continued)

(MAX1541 circuit of Figure 12, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, TON = REF, T_A = +25°C, unless otherwise noted.)

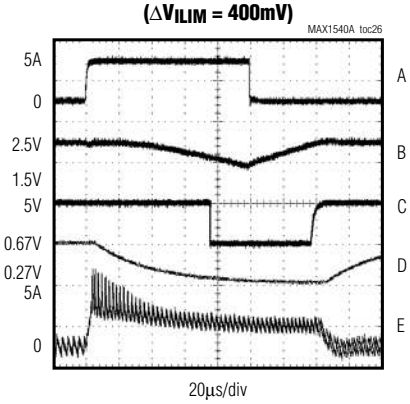
INDUCTOR-SATURATION PROTECTION (ΔV_{ILIM} = 200mV)



A. I_{OUT2} = 0 TO 5A, 5A/div
B. 2.5V OUTPUT, 200mV/div
C. ILIM, 200mV/div
D. INDUCTOR CURRENT, 5A/div

LSAT = REF, L = 3.3µH 3.5A

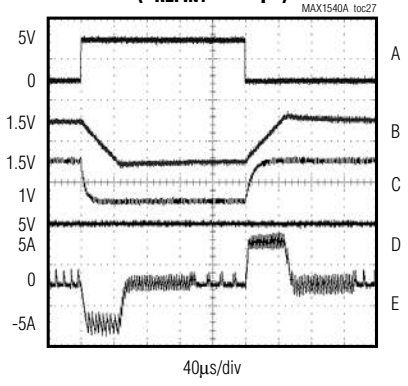
INDUCTOR-SATURATION PROTECTION (ΔV_{ILIM} = 400mV)



A. I_{OUT2} = 0 TO 5A, 5A/div
B. 2.5V OUTPUT, 1V/div
C. PGOOD, 5V/div
D. ILIM, 400mV/div
E. INDUCTOR CURRENT, 5A/div

LSAT = REF, L = 3.3µH 3.5A

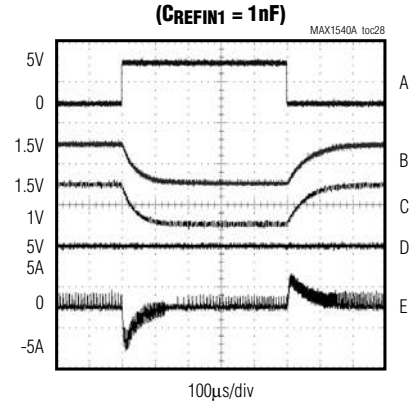
MAX1541 DYNAMIC OUTPUT-VOLTAGE TRANSITION (C_{REFIN1} = 100pF)



A. GATE, 5V/div
B. OUT1 (1.0V TO 1.5V), 0.5V/div
C. REFIN1, 0.5V/div
D. PGOOD1, 5V/div
E. INDUCTOR CURRENT, 5A/div

200mA LOAD, $\overline{SKIP}$ = GND

MAX1541 DYNAMIC OUTPUT-VOLTAGE TRANSITION (C_{REFIN1} = 1nF)



A. GATE, 5V/div
B. OUT1 (1.0V TO 1.5V), 0.5V/div
C. REFIN1, 0.5V/div
D. PGOOD1, 5V/div
E. INDUCTOR CURRENT, 5A/div

200mA LOAD, $\overline{SKIP}$ = GND

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Pin Description

PIN		NAME	FUNCTION
MAX1540A	MAX1541		
1	1	OVP/UVP	Overvoltage/Undervoltage Protection and Discharge-Mode Control Input. This four-level logic input selects between various output fault-protection options (Table 7) by selectively enabling OVP protection and UVP protection. When enabled, the OVP limit defaults at 116% of the nominal output voltage, and the UVP limit defaults at 70% of the nominal output voltage. Discharge mode is enabled when OVP protection is also enabled. Connect OVP/UVP to the following pins for the desired function: V_{CC} = enable OVP and discharge mode, enable UVP. Open = enable OVP and discharge mode, disable UVP. REF = disable OVP and discharge mode, enable UVP. GND = disable OVP and discharge mode, disable UVP. See the *Fault Protection* and *(ON_)* sections.
2	2	$\overline{SKIP}$	Pulse-Skipping Control Input. This four-level logic input enables or disables the light-load pulse-skipping operation of each output: V_{CC} = OUT1 and OUT2 in forced-PWM mode. Open = OUT1 in forced-PWM mode, OUT2 in pulse-skipping mode. REF = OUT1 in pulse-skipping mode, OUT2 in forced-PWM mode. GND = OUT1 and OUT2 in pulse-skipping mode.
3	3	LSAT	Inductor-Saturation Control Input. This four-level logic input sets the inductor-current saturation limit as a multiple of the valley current-limit threshold set by ILIM, or disables the function if not required. Connect LSAT to the following pins to set the saturation current limit: V_{CC} = 2 x $I_{LIM(VAL)}$ Open = 1.75 x $I_{LIM(VAL)}$ REF = 1.5 x $I_{LIM(VAL)}$ GND = disable LSAT protection See the *Inductor Saturation Limit* and *Setting the Current Limit* sections.
4	4	TON	On-Time Selection Control Input. This four-level logic input sets the K-factor value used to determine the DH_ on-time (see the *On-Time One-Shot (TON)* section). Connect to analog ground (GND), REF, or V_{CC}; or leave TON unconnected to select the following nominal switching frequencies: V_{CC} = 235kHz (OUT1) / 170kHz (OUT2) Open = 345kHz (OUT1) / 255kHz (OUT2) REF = 485kHz (OUT1) / 355kHz (OUT2) GND = 620kHz (OUT1) / 460kHz (OUT2)
5	5	V_{CC}	Analog Supply Input. Connect to the system supply voltage (+4.5V to +5.5V) through a series 20Ω resistor. Bypass V_{CC} to analog ground with a 1µF or greater ceramic capacitor.
—	6	GATE	Buffered N-Channel MOSFET Gate Input. A logic low on GATE turns off the internal MOSFET so OD appears as high impedance. A logic high on GATE turns on the internal MOSFET, pulling OD to ground.
—	7	CC1	Integrator Capacitor Connection for Controller 1. Connect a 47pF to 470pF (47pF typ) capacitor from CC1 to analog ground (GND) to set the integration time constant for the main MAX1541 controller (OUT1).

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1540A	MAX1541		
6	8	ILIM1	Valley Current-Limit Threshold Adjustment for Controller 1. The valley current-limit threshold defaults to 50mV if ILIM1 is tied to V_{CC}. In adjustable mode, the valley current-limit threshold across CSP1 and CSN1 is precisely 1/10 the voltage seen at ILIM1 over a 250mV to 2.5V range. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V. When the inductor-saturation protection threshold is exceeded, ILIM1 sinks 6µA. See the *Current-Limit Protection* section.
7	9	ILIM2	Valley Current-Limit Threshold Adjustment for Controller 2. The valley current-limit threshold defaults to 50mV if ILIM2 is tied to V_{CC}. In adjustable mode, the valley current-limit threshold across CSP2 and CSN2 is precisely 1/10th the voltage seen at ILIM2 over a 250mV to 2.5V range. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V. When the inductor-saturation protection threshold is exceeded, ILIM2 sinks 6µA. See the *Current-Limit Protection* section.
8	10	REF	2.0V Reference Voltage Output. Bypass REF to analog ground with a 0.1µF or greater ceramic capacitor. The reference can source up to 50µA for external loads. Loading REF degrades output voltage accuracy according to the REF load-regulation error. The reference is disabled when the MAX1540A/MAX1541 are shut down.
—	11	REFIN1	External Reference Input for Controller 1. REFIN1 sets the main feedback regulation voltage ($V_{FB1} = V_{REFIN1}$) of the MAX1541.
—	12	OD	Open-Drain Output. Controlled by GATE.
9	13	CSP2	Positive Current-Sense Input for Controller 2. Connect to the positive terminal of the current-sense element. Figure 14 and Table 9 describe several current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the valley current-limit threshold programmed at ILIM2.
10	14	CSN2	Negative Current-Sense Input for Controller 2. Connect to the negative terminal of the current-sense element. Figure 14 and Table 9 describe several current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the valley current-limit threshold programmed at ILIM2.
11	15	FB2	Feedback Input for Controller 2: MAX1540A: Connect to V_{CC} for a +1.5V fixed output or to analog ground (GND) for a +2.5V fixed output. For an adjustable output (0.7V to 5.5V), connect FB2 to a resistive divider from OUT2. The FB2 regulation level is +0.7V. MAX1541: Connect to V_{CC} for a +1.8V fixed output or to analog ground (GND) for a +2.5V fixed output. For an adjustable output (0.7V to 5.5V), connect FB2 to a resistive divider from OUT2. The FB2 regulation level is +0.7V.
12	16	OUT2	Output Voltage-Sense Connection for Controller 2. Connect directly to the positive terminal of the output capacitors as shown in the standard application circuits (Figures 1 and 12). OUT2 senses the output voltage to determine the on-time for the high-side switching MOSFET. OUT2 also serves as the feedback input when using the preset internal output voltages as shown in Figure 10. When discharge mode is enabled by OVP/UVP, the output capacitor is discharged through an internal 10Ω resistor connected between OUT2 and ground.

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1540A	MAX1541		
13	17	PGOOD2	Open-Drain Power-Good Output. PGOOD2 is low when the output voltage is more than 10% (typ) above or below the normal regulation point, during soft-start, and in shutdown. After the soft-start circuit has terminated, PGOOD2 becomes high impedance if the output is in regulation.
14	18	DH2	High-Side Gate-Driver Output for Controller 2. DH2 swings from LX2 to BST2.
15	19	LX2	Inductor Connection for Controller 2. Connect to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
16	20	BST2	Boost Flying-Capacitor Connection for Controller 2. Connect to an external capacitor and diode as shown in Figure 8. An optional resistor in series with BST2 allows the DH2 pullup current to be adjusted.
17	21	GND	Analog and Power Ground. Connect backside pad to GND.
18	22	DL2	Low-Side Gate-Driver Output for Controller 2. DL2 swings from GND to LDOOUT (MAX1540A) or GND to V_{DD} (MAX1541).
19	23	V+	Battery Voltage Input. The controller uses V+ to set the on-time one-shot timing. The DH on-time is inversely proportional to input voltage over a range of 2V to 28V. For the MAX1540A, V+ also serves as the linear-regulator input supply.
—	24	LDOIN	Internal Linear-Regulator Input Supply. Power LDOIN from a 4.5V to 28V voltage source. Bypass LDOIN to GND with a 4.7µF or greater capacitor. For the MAX1540A, LDOIN is internally connected to V+. For the MAX1541, LDOIN must be connected to V_{DD} when LDO is not used.
—	25	V_{DD}	MAX1541 Supply Voltage Input for the DL_ Gate Driver. Connect to the system supply voltage (+4.5V to +5.5V). Bypass V_{DD} to power ground with a 1µF or greater ceramic capacitor. For the MAX1540A, LDOOUT supplies the DL_ gate drivers (V_{DD} = LDOOUT).
20	26	LDOOUT	Linear Regulator Output. Bypass LDOOUT with a 1µF or greater capacitor per 5mA of load (internal and external), with a minimum of 4.7µF. For the MAX1540A, LDOOUT powers the DL_ gate drivers (V_{DD} internally connected to LDOOUT).
—	27	FBLDO	Feedback Input for the Linear Regulator. Connect to GND for a fixed 5V output. For an adjustable output (1.25V to V_{LDOIN} - 0.6V), connect FBLDO to a resistive voltage-divider from LDOOUT to analog ground (GND). The FBLDO regulation voltage is +1.25V. For the MAX1540A, FBLDO is internally connected to GND for a fixed 5V output.
21	28	DL1	Low-Side Gate-Driver Output for Controller 1. DL1 swings from GND to LDOOUT (MAX1540A) or GND to V_{DD} (MAX1541).
22	29	LDOON	Linear-Regulator Enable Input. For automatic startup, connect to V+ or LDOIN (MAX1541). Connect to GND to shut down the linear regulator.
23	30	BST1	Boost Flying-Capacitor Connection for Controller 1. Connect to an external capacitor and diode as shown in Figure 8. An optional resistor in series with BST1 allows the DH1 pullup current to be adjusted.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1540A	MAX1541		
24	31	LX1	Inductor Connection for Controller 1. Connect to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
25	32	DH1	High-Side Gate-Driver Output for Controller 1. DH1 swings from LX1 to BST1.
26	33	PGOOD1	Open-Drain Power-Good Output. PGOOD1 is low when the output voltage is more than 10% (typ) above or below the normal regulation point, during soft-start, and in shutdown. After the soft-start circuit has terminated, PGOOD1 becomes high impedance if the output is in regulation. For the MAX1541, PGOOD1 is blanked—forced high-impedance state—when FBLANK is enabled and the controller detects a transition on GATE.
27	34	OUT1	Output Voltage-Sense Connection for Controller 1. Connect directly to the positive terminal of the output capacitors as shown in the standard application circuits (Figures 1 and 12). OUT1 senses the output voltage to determine the on-time for the high-side switching MOSFET. For the MAX1540A, OUT1 also serves as the feedback input when using the preset internal output voltages as shown in Figure 10. When discharge mode is enabled by OVP/UVP, the output capacitor is discharged through
28	35	FB1	Feedback Input for Controller 1: MAX1540A: Connect to V_{CC} for a +1.2V fixed output or to analog ground (GND) for a +1.8V fixed output. For an adjustable output (0.7V to 5.5V), connect FB1 to a resistive divider from OUT1. The FB1 regulation level is +0.7V. MAX1541: The FB1 regulation level is set by the voltage at REFIN1.
29	36	CSN1	Negative Current-Sense Input for Controller 1. Connect to the negative terminal of the current-sense element. Figure 14 and Table 9 describe several current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the valley current-limit threshold programmed at ILIM1.
30	37	CSP1	Positive Current-Sense Input for Controller 1. Connect to the positive terminal of the current-sense element. Figure 14 and Table 9 describe several current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the valley current-limit threshold programmed at ILIM1.
—	38	FBLANK	Fault-Blanking Control Input. This four-level logic input enables or disables fault blanking, and sets the forced-PWM operation time (t_{FBLANK}). When fault blanking is enabled, PGOOD1 and the OVP/UVP protection for controller 1 are blanked for the selected time period after the MAX1541 detects a transition on GATE. Additionally, controller 1 enters forced-PWM mode for the duration of t_{FBLANK} anytime GATE changes states. Connect FBLANK as follows: V_{CC} = 220µs t_{FBLANK}, fault blanking enabled. Open = 140µs t_{FBLANK}, fault blanking enabled. REF = 65µs t_{FBLANK}, fault blanking enabled. GND = 140µs t_{FBLANK}, fault blanking disabled. See the *Electrical Characteristics* table for the t_{FBLANK} limits.

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1540A	MAX1541		
31	39	ON2	OUT2 Enable Input. Pull ON2 to GND to shut down controller 2 (OUT2). Connect to V_{CC} for normal operation. When discharge mode is enabled by OVP/UVP, the output is discharged through a 10Ω resistor between OUT2 and GND, and DL2 is forced high after V_{OUT2} drops below 0.3V. When discharge mode is disabled by OVP/UVP, OUT2 remains a high-impedance input and DL2 is forced low so LX2 also appears as a high impedance. A rising edge on ON1 or ON2 clears the fault-protection latch.
32	40	ON1	OUT1 Enable Input. Pull ON1 to GND to shut down controller 1 (OUT1). Connect to V_{CC} for normal operation. When discharge mode is enabled by OVP/UVP, the output is discharged through a 10Ω resistor between OUT1 and GND, and DL1 is forced high after V_{OUT1} drops below 0.3V. When discharge mode is disabled by OVP/UVP, OUT1 remains a high-impedance input and DL1 is forced low so LX1 also appears as high impedance. A rising edge on ON1 or ON2 clears the fault-protection latch.
—	—	EP	Exposed Backside Pad. Connect the exposed backside pad to analog ground.

Table 1. Component Selection for Standard Applications

COMPONENT	MAX1540A		MAX1541	
	PWM1	PWM2	PWM1	PWM2
Input Voltage (V_{IN})	7V to 24V	7V to 24V	7V to 24V	7V to 24V
Output Voltage ($V_{OUT\_}$)	1.8V	2.5V	1.0V/1.5V	2.5V
Load Current ($I_{OUT\_}$)	4A	8A	4A	4A
Switching Frequency ($f_{SW\_}$)	TON = REF (485kHz)	TON = REF (355kHz)	TON = REF (485kHz)	TON = REF (355kHz)
Input Capacitor (C_{IN})	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM		(2) 4.7µF, 25V Taiyo Yuden TMK325BJ475KM	
Output Capacitor ($C_{OUT\_}$)	220µF, 6.3V, 12mΩ Sanyo POSCAP 6TPD220M	330µF, 4V, 12mΩ Sanyo POSCAP 4TPD330M	470µF, 4V, 10mΩ Sanyo POSCAP 4TPD470M	220µF, 6.3V, 12mΩ Sanyo POSCAP 6TPD220M
High-Side MOSFET ($N_{H\_}$)	35mΩ, 30V Fairchild 1/2 FDS6982S	20mΩ, 30V Fairchild FDS6690	35mΩ, 30V Fairchild 1/2 FDS6982S	35mΩ, 30V Fairchild 1/2 FDS6982S
Low-Side MOSFET ($N_{L\_}$)	22mΩ, 30V Fairchild 1/2 FDS6982S	12.5mΩ, 30V Fairchild FDS6670S	22mΩ, 30V Fairchild 1/2 FDS6982S	22mΩ, 30V Fairchild 1/2 FDS6982S
Low-Side Schottky ($D_{L\_}$) (if needed)	1A, 30V Schottky Nihon EP10QS03L	1A, 30V Schottky Nihon EP10QS03L	1A, 30V Schottky Nihon EP10QS03L	1A, 30V Schottky Nihon EP10QS03L
Inductor (L_)	2.5µH, 6.2A, 15mΩ Sumida CDEP105(H)-2R5	2.2µH, 10A, 4.4mΩ Sumida CDEP105(L)-2R2	1.8µH, 9.0A, 6.2mΩ Sumida CDEP105(S)-1R8	4.3µH, 6.8A, 8.7mΩ Sumida CDEP105(L)-4R3
$R_{SENSE\_}$	15mΩ ±1%, 0.5W IRC LR2010-01-R015F or Dale WSL-2010-R015F	5mΩ ±1%, 0.5W IRC LR2010-01-R005F or Dale WSL-2010-R005F	15mΩ ±1%, 0.5W IRC LR2010-01-R015F or Dale WSL-2010-R015F	15mΩ ±1%, 0.5W IRC LR2010-01-R015F or Dale WSL-2010-R015F

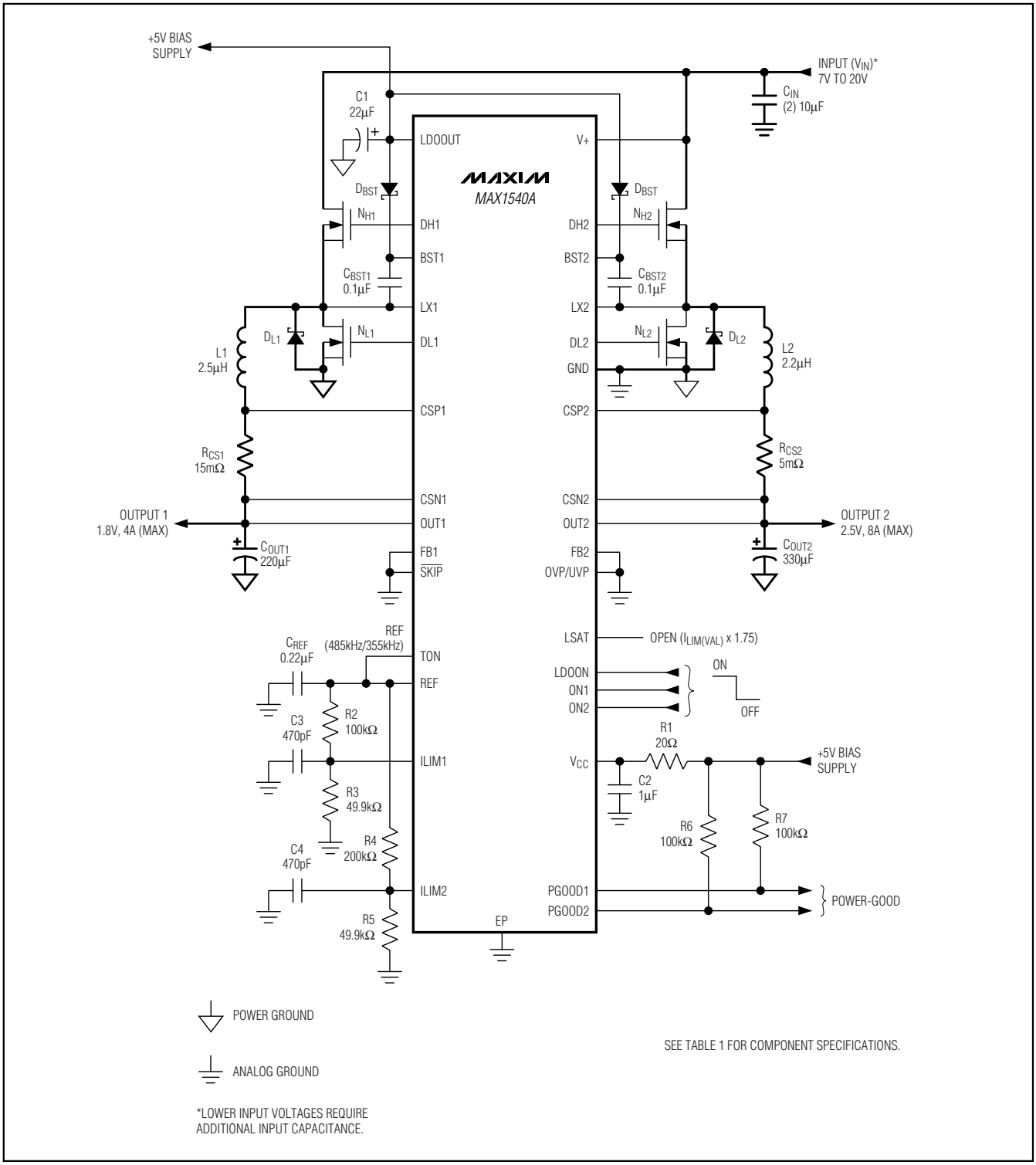


Figure 1. MAX1540A Standard Application Circuit

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Central Semiconductor	631-435-1110 (USA)	www.centralsemi.com
Coilcraft	800-322-2645 (USA)	www.coilcraft.com
Fairchild Semiconductor	888-522-5372 (USA)	www.fairchildsemi.com
International Rectifier	310-322-3331 (USA)	www.irf.com
Kemet	408-986-0424 (USA)	www.kemet.com
Panasonic	65-6231-3226 (Singapore), 408-749-9714 (USA)	www.panasonic.com
Sanyo	619-661-6835 (USA)	www.sanyovideo.com
Siliconix (Vishay)	203-268-6261 (USA)	www.vishay.com
Sumida	408-982-9660 (USA)	www.sumida.com
Taiyo Yuden	03-3667-3408 (Japan), 408-573-4150 (USA)	www.t-yuden.com
TDK	847-803-6100 (USA), 81-3-5201-7241 (Japan)	www.component.tdk.com
TOKO	858-675-8013 (USA)	www.tokoam.com

Standard Application Circuits

The MAX1540A standard application circuit (Figure 1) generates a 1.8V and 2.5V rail for general-purpose use in a notebook computer. The MAX1541 Standard Application Circuit (Figure 12) generates a dynamically adjustable output voltage (OUT1), typical of a graphics-processor core requirement, and a fixed 2.5V output (OUT2).

See Table 1 for component selections. Table 2 lists the component manufacturers.

Detailed Description

The MAX1540A/MAX1541 provide three independent outputs with independent enable controls. They contain two Quick-PWM step-down controllers ideal for low-voltage power supplies for notebook computers, and a 100mA linear regulator. Maxim's proprietary Quick-PWM pulse-width modulators in the MAX1540A/ MAX1541 are specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs, while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes.

The MAX1540A linear regulator draws power from the battery voltage and generates a preset 5V, which can be used to bootstrap the buck controllers for automatic startup. The MAX1541's linear regulator can be connected to any input source from 4.5V to 28V to generate an adjustable output voltage as low as 1.25V, or as high as the input source with 800mV of dropout at 50mA load.

Single-stage buck conversion allows the MAX1540A/ MAX1541 to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down from another system supply rail instead of the battery at a higher switching frequency) allows the minimum possible physical size.

The MAX1540A generates chipset, dynamic random-access memory (DRAM), CPU I/O, or other low-voltage supplies down to 0.7V. The MAX1541 powers chipsets and graphics processor cores that require dynamically adjustable output voltages, or generates the active termination bus that must track the input reference. The MAX1540A is available in a 32-pin thin QFN package with optional inductor-saturation protection and overvoltage/undervoltage protection. The MAX1541 is available in a 40-pin thin QFN package with optional inductor-saturation protection and overvoltage/undervoltage protection.

+5V Bias Supply (V_{CC} and V_{DD})

The MAX1540A/MAX1541 require a 5V bias supply in addition to the battery. This 5V bias supply is either the MAX1540A/MAX1541s' internal linear regulator or the notebook's 95%-efficient 5V system supply. Keeping the bias supply external to the IC can improve efficiency and allows the fixed 5V or adjustable linear regulator (MAX1541) to be used for other applications. For the MAX1540A, the gate-driver input supply (V_{DD}) is con-

nected internally to the fixed 5V linear-regulator output (LDOOUT).

The 5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$
$$= 4mA \text{ to } 50mA \text{ (typ)}$$

where I_{CC} is 1.1mA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

The V+ battery input and 5V bias inputs (V_{CC} and V_{DD}) can be connected together if the input source is a fixed 4.5V to 5.5V supply. If the 5V bias supply powers up prior to the battery supply, the enable signals (ON1 and ON2 going from low to high) must be delayed until the battery voltage is present in order to ensure startup.

Free-Running, Constant On-Time, PWM Controller with Input Feed Forward

The Quick-PWM control architecture is a pseudofixed-frequency, constant on-time, current-mode regulator with voltage feed forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The Quick-PWM algorithm is simple: the high-side switch on-time relies solely on an adjustable one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a fixed minimum off-time (400ns typ). The controller triggers the on-time one-shot when the error comparator is low, the inductor current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to the battery and output voltages. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input (V_{IN} = V+), and proportional to the output voltage as measured by the OUT_ input:

$$On\text{-}Time = K \left(\frac{V_{OUT}}{V_{IN}} \right)$$

where K (switching period) is set by the TON pin-strap connection (Table 3). This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: 1) the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band and 2) the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The on-time for the main controller (DH1) is set 15% higher than the nominal frequency setting (200kHz, 300kHz, 420kHz, or 540kHz), while the on-time for the secondary controller (DH2) is set 15% lower than the nominal setting. This prevents audio-frequency "beating" between the two asynchronous regulators.

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* (approximately ±12.5% at 540kHz and 420kHz nominal settings, and ±10% with the 300kHz and 200kHz settings). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* can vary over a wider range.

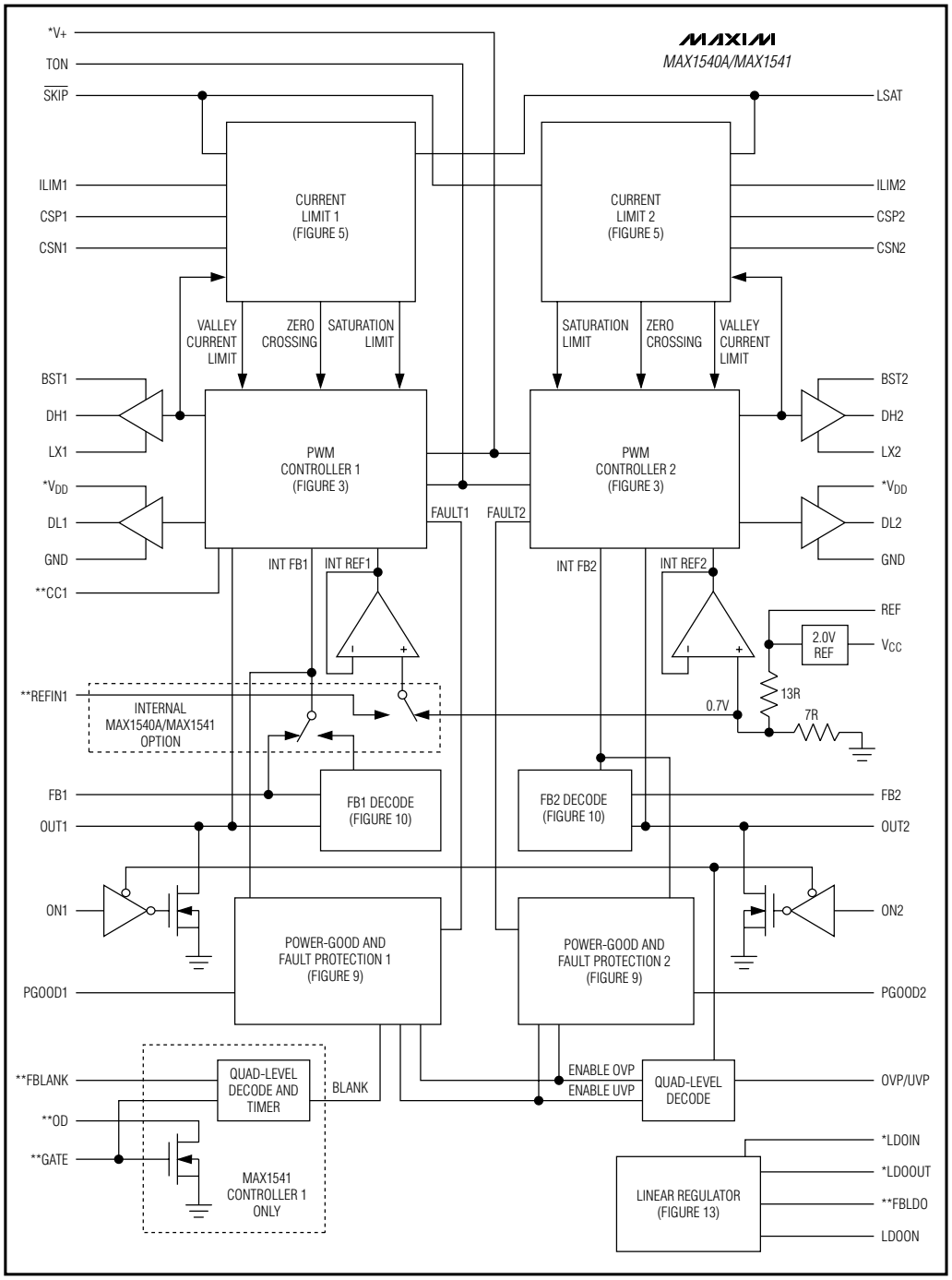
The constant on-time translates only roughly to a constant switching frequency. The on-times guaranteed in the *Electrical Characteristics* are influenced by resistive losses and by switching delays in the high-side MOSFET. Resistive losses—including the inductor, both MOSFETs, and PC board copper losses in the output and ground—tend to raise the switching frequency as the load increases. The dead-time effect increases the effective on-time, reducing the switching frequency as one or both dead times add to the effective on-time. It occurs only in PWM mode ($\overline{SKIP}$ = V_{CC}) and during dynamic output-voltage transitions when the inductor current reverses at light- or negative-load currents. With reversed inductor current, the inductor's EMF causes LX_ to go high earlier than normal, extending the on-time by a period equal to the driver dead time.

For loads above the critical conduction point, where the dead-time effect no longer occurs, the actual switching frequency is:

$$f_{SW} = \frac{V_{OUT\_} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, includ-

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator



*FOR THE MAX1540A:
LDOIN IS CONNECTED TO V+.
LDOOUT IS CONNECTED TO V_{DD}.
**MAX1541 CONTROLLER ONLY.

Figure 2. MAX1540A/MAX1541 Functional Diagram

Table 3. Approximate K-Factor Errors

NOMINAL TON SETTING (kHz)	K-FACTOR ERROR (%)	CONTROLLER 1 (OUT1)		CONTROLLER 2 (OUT2)	
		TYPICAL K-FACTOR (µs)	MINIMUM V_{IN} AT V_{OUT1} = 1.8V* (V)	TYPICAL K-FACTOR (µs)	MINIMUM V_{IN} AT V_{OUT2} = 2.5V* (V)
200kHz (TON = V_{CC})	±10	4.5 (235kHz)	2.28	6.2 (170kHz)	2.96
300kHz (TON = open)	±10	3.0 (345kHz)	2.52	4.1 (255kHz)	3.18
420kHz (TON = REF)	±12.5	2.2 (485kHz)	2.91	3.0 (355kHz)	3.48
540kHz (TON = GND)	±12.5	1.7 (620kHz)	3.42	2.3 (460kHz)	3.87

**See the Step-Down Converter Dropout Performance section (h = 1.5 and worst-case K-factor value used).*

Table 4. $\overline{SKIP}$ Configuration Table

$\overline{SKIP}$	OUT1 MODE	OUT2 MODE
V_{CC}	Forced PWM	Forced PWM
Open	Forced PWM	Pulse skipping
REF	Pulse skipping	Forced PWM
GND	Pulse skipping	Pulse skipping

ing the high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time calculated by the MAX1540A/MAX1541.

Light-Load Operation ($\overline{SKIP}$)

The four-level $\overline{SKIP}$ input selects light-load, pulse-skipping operation by independently enabling or disabling the zero-crossing comparator for each controller (Table 4). When the zero-crossing comparator is enabled, the controller forces DL_ low when the current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output. When the zero-crossing comparator is disabled, the controller maintains PWM operation under light-load conditions (see the *Forced-PWM Mode* section).

Automatic Pulse-Skipping Mode

In skip mode, an inherent automatic switchover to PFM takes place at light loads (Figure 3). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator differentially senses the inductor current across the current-sense inputs (CSP_ to CSN_). Once $V_{CSP\_}$ - $V_{CSN\_}$ drops below 5% of the current-limit threshold (2.5mV for the default 50mV current-limit threshold), the comparator forces DL_ low (Figure 3). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical-conduction" point). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to half the peak-to-peak ripple current, which is a function of the inductor value (Figure 4). This threshold is relatively constant, with only a minor dependence on battery voltage:

$$I_{LOAD(SKIP)} \approx \left(\frac{V_{OUT}K}{2L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

where K is the on-time scale factor (Table 3). For example, in the MAX1541 Standard Application Circuit (Figure 12) (K = 3.0µs, V_{OUT2} = 2.5V, V_{IN} = 12V, and L = 4.3µH), the pulse-skipping switchover occurs at:

$$\left(\frac{2.5V \times 3.0\mu s}{2 \times 4.3\mu H}\right)\left(\frac{12V - 2.5V}{12V}\right) = 0.69A$$

The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used. The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

DC-output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX1540A/MAX1541 regulate the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

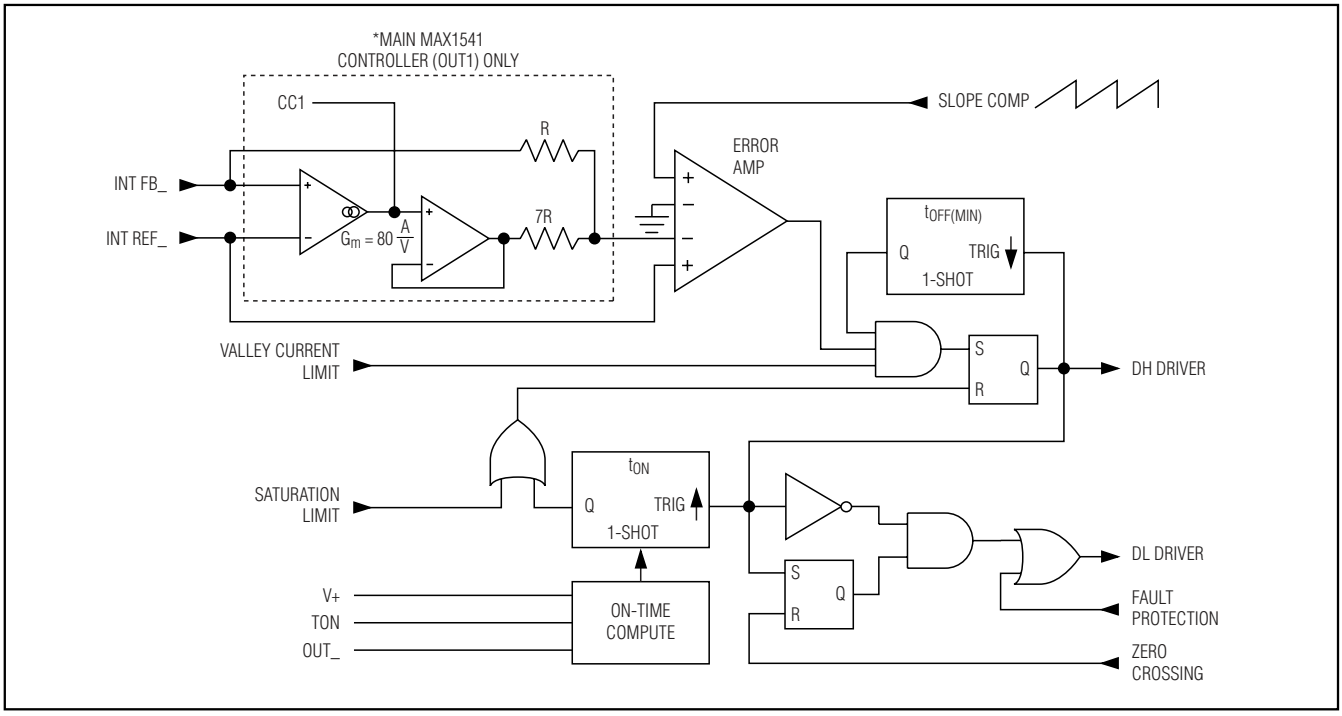


Figure 3. MAX1540A/MAX1541 PWM-Controller Functional Diagram

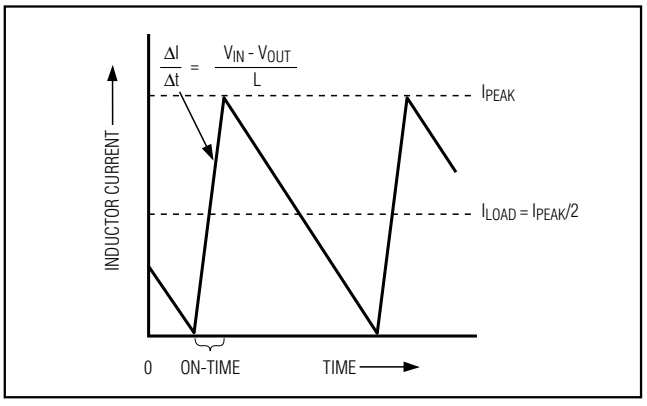


Figure 4. Pulse-Skipping/Discontinuous Crossover Point

(I_{OUT} < $I_{LOAD(SKIP)}$), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

Forced-PWM Mode

The low-noise forced-PWM mode disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to be constantly the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH_ maintains a duty factor of $V_{OUT\_}$ / V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 4mA to 40mA, depending on the external MOSFETs and switching frequency.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, and providing sink-current capability for dynamic output-voltage adjustment. The MAX1541 uses forced-PWM operation during all dynamic output-voltage transitions (GATE transition detected) in order to ensure fast, accurate transitions. Since forced-PWM operation disables the zero-crossing comparator, the inductor current reverses under light loads, quickly discharging the output capacitors. FBLANK determines how long the MAX1541 maintains forced-PWM operation—typically 220µs (FBLANK = V_{CC}), 140µs (FBLANK = open or GND), or 65µs (FBLANK = REF).

Current-Limit Protection (ILIM_)

Valley Current Limit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses a current-sense resistor between CSP_ and CSN_ as the current-sensing ele-

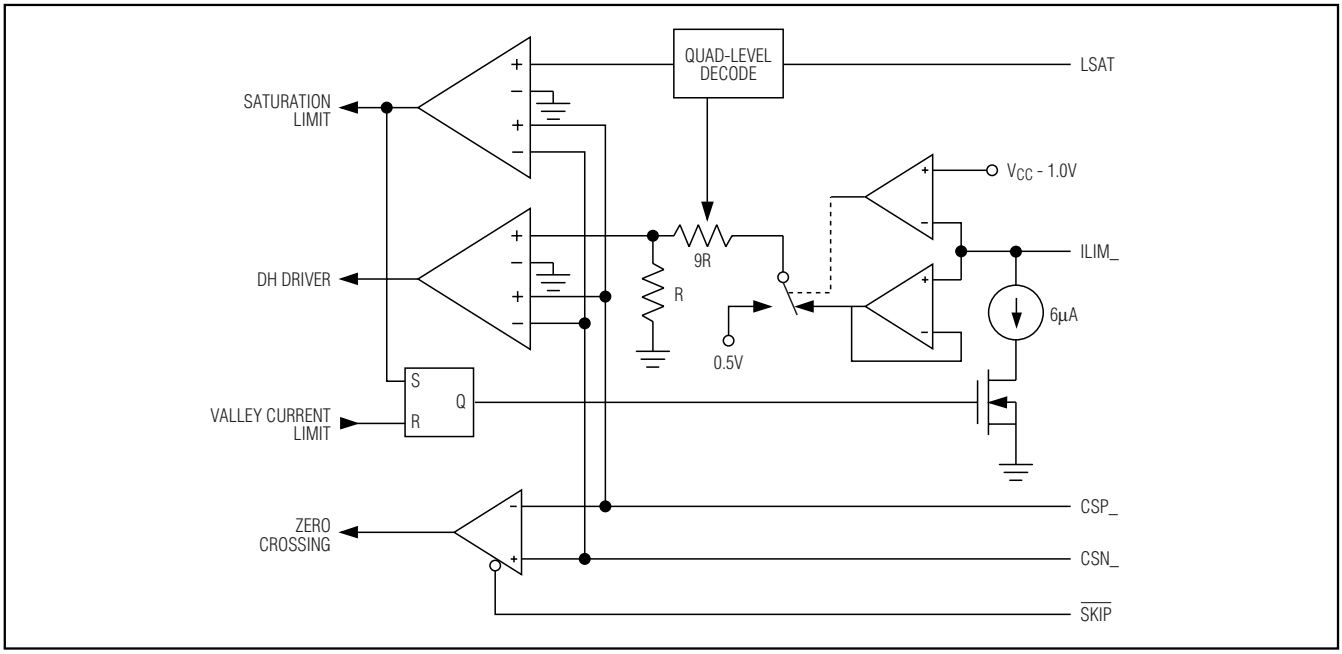


Figure 5. MAX1540A/MAX1541 Current-Limit Functional Diagram

ment (Figure 1). If the magnitude of the current-sense signal is above the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle (Figures 3 and 5). The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance. Figure 6 shows the valley current-limit threshold point.

In forced-PWM mode, the MAX1540A/MAX1541 also implement a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and tracks the positive current limit when ILIM is adjusted.

The current-limit threshold is adjusted with an external resistor-divider at ILIM_. A 2µA to 20µA divider current is recommended for accuracy and noise immunity. The current-limit threshold adjustment range is from 25mV to 200mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage seen at ILIM_. The threshold defaults to 50mV when ILIM_ is

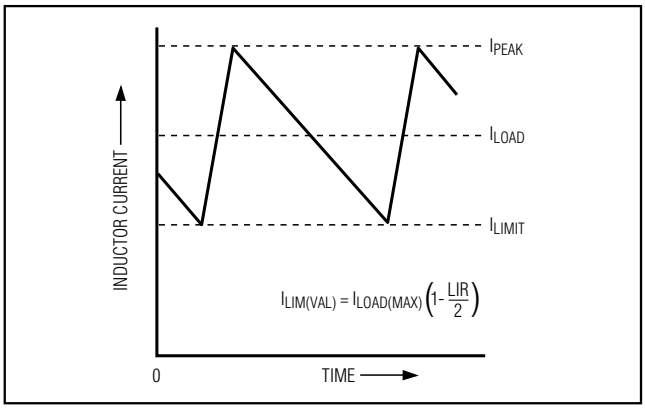


Figure 6. Valley Current-Limit Threshold Point

connected to V_{CC}. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen by CSP_ and CSN_. Place the IC close to the sense resistor with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Inductor-Saturation Limit

The LSAT connection selects an upper current-sense limit as the inductor-saturation threshold, or disables the inductor-saturation protection feature altogether (LSAT = GND). When enabled, the inductor-saturation threshold is a multiple of the positive valley current-limit threshold (Table 5) and tracks the valley current limit when ILIM is adjusted. The selected inductor-saturation threshold should give sufficient headroom above the peak inductor current so switching noise does not accidentally trip the saturation protection. Selecting an excessively high threshold may allow inductor saturation to go undetected. For an inductor with a low LIR (the ratio of the inductor ripple current to the designed maximum load current) near 20%, select the lowest saturation threshold of 1.5 x $I_{LIM(VAL)}$ (LSAT = REF). When using an inductor with a higher LIR, increase the inductor-saturation threshold accordingly.

When inductor-saturation protection is enabled, the MAX1540A/MAX1541 continuously monitor the inductor current through the voltage across the current-sense resistor. When the inductor-saturation threshold is exceeded, the MAX1540A/MAX1541 immediately turn off the high-side gate driver and enable a 6µA discharge current on ILIM_ (Figure 7) at the beginning of the next DH_ on-time. This reduces the voltage on ILIM_ by ΔV_{ILIM} where:

$$\Delta V_{ILIM} = -\left(\frac{R_A R_B}{R_A + R_B}\right) I_{ILIM(LSAT)}$$

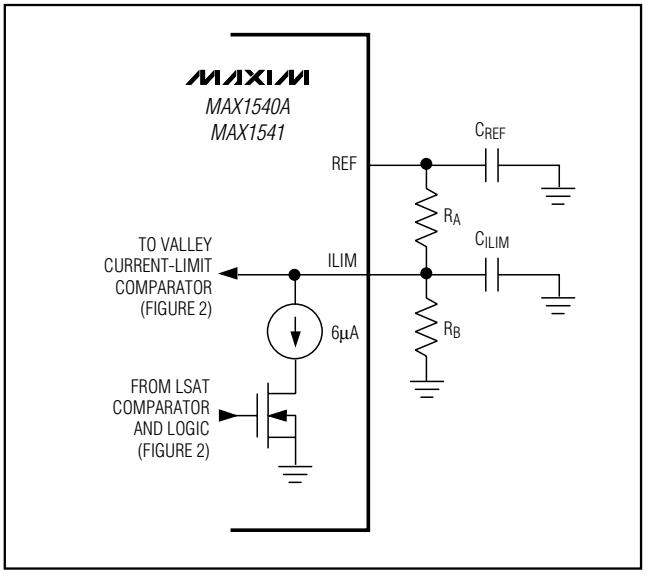


Figure 7. Adjustable Current-Limit Threshold

where the ILIM saturation fault sink current ($I_{ILIM(LSAT)}$) is typically 6µA (see the *Electrical Characteristics* table). When using the default 50mV valley current-limit threshold (ILIM_ = V_{CC}), the ILIM_ saturation fault sink current does not lower the current-limit threshold (Figure 5).

If the inductor current remains below the saturation threshold during the next cycle, the controller disables the ILIM_ discharge current, allowing the ILIM_ voltage to return to its nominal set point. The inductor should not remain in saturation once the controller reduces the valley current limit. If the inductor remains saturated, the output voltage may drop low enough to trip the undervoltage fault protection (UVP enabled), causing the MAX1540A/MAX1541 to set the fault latch and shut down both outputs. Adding a capacitor from ILIM_ to GND slows the ILIM_ voltage change by the time constant $\tau = (R_A \parallel R_B) \times C_{ILIM}$, where τ is between 5 to 10 switching periods. If the inductor saturation occurs only during a short load transient, the time constant allows the power supply to recover before the output voltage drops below the output undervoltage threshold.

Set ΔV_{ILIM} to be at least 30% of the ILIM_ set voltage. Calculate R_A and R_B using the equations below:

$$R_A = \frac{V_{REF}}{I_{ILIM(LSAT)}}\left(\frac{\Delta V_{ILIM}}{V_{ILIM(SET)}}\right) \text{ with } \left(\frac{\Delta V_{ILIM}}{V_{ILIM(SET)}}\right) \text{ set at 30\%}$$

$$R_B = \frac{R_A}{\left(\frac{V_{REF}}{V_{ILIM(SET)}} - 1\right)}$$

Inductor-saturation sensing works best when using a current-sense resistor in series with the inductor. See the *Setting the Current Limit* section for various current-sense configurations (Figure 14) and LSAT recommendations.

Table 5. LSAT Configuration Table

LSAT	INDUCTOR-SATURATION THRESHOLD
V_{CC}	2.00 x $I_{LIM(VAL)}$
Open	1.75 x $I_{LIM(VAL)}$
REF	1.50 x $I_{LIM(VAL)}$
GND	Disabled

MOSFET Gate Drivers (DH_, DL_)

The DH_ and DL_ drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL_ output and prevents the high-side MOSFET from turning on until DL_ is off. A similar adaptive dead-time circuit monitors the DH_ output, preventing the low-side MOSFET from turning on until DH_ is off. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX1540A/MAX1541 interprets the MOSFET gates as "off" while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL_ low is robust, with a 0.6Ω (typ) on-resistance. This helps prevent DL_ from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX_) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces may require additional gate-to-source capacitance to ensure fast-rising LX_ edges do not pull up the low-side MOSFETs gate, causing shoot-through currents. The capacitive coupling between LX_ and DL_ created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS}-C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage can cause problems in marginal designs. Alternatively, adding a resistor less than 10Ω in series with BST_ can remedy the problem by increasing the turn-on time of the high-side MOSFET without degrading the turn-off time (Figure 8).

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and soft-start counter, powering-up the reference, and preparing the PWM for operation. Until V_{CC} reaches 4.25V (typ), V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching. The controller inhibits switching by pulling DH_ low, and holding DL_ low when OVP and shutdown discharge are disabled or forcing DL_ high when OVP and shutdown discharge are enabled (Table 7). When V_{CC} rises above 4.25V and ON_ is driven high, the controller activates the PWM controller and initializes soft-start.

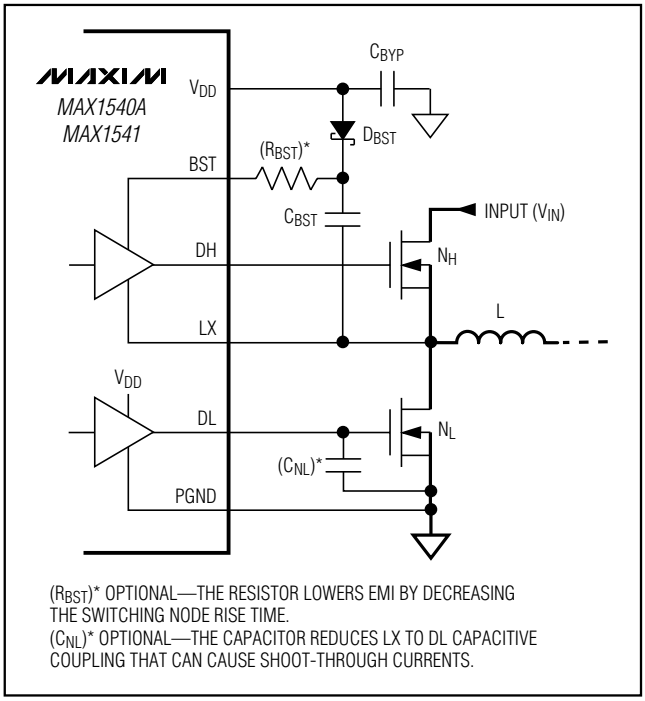


Figure 8. Optional Gate-Driver Circuitry

Soft-start allows a gradual increase of the internal current-limit level during startup to reduce the input surge currents. The MAX1540A/MAX1541 divide the soft-start period into five phases. During the first phase, the controller limits the current limit to only 20% of the full current limit. If the output does not reach regulation within 425µs, soft-start enters the second phase, and the current limit is increased by another 20%. This process is repeated until the maximum current limit is reached after 1.7ms or when the output reaches the nominal regulation voltage, whichever occurs first (see the soft-start waveforms in the *Typical Operating Characteristics*).

Power-Good Output (PGOOD_)

PGOOD_ is the open-drain output for a window comparator that continuously monitors the output. PGOOD_ is actively held low in shutdown and during soft-start. After the digital soft-start terminates, PGOOD_ becomes high impedance as long as the respective output voltage is within ±10% of the nominal regulation voltage set by FB_. When the output voltage drops 10% below or rises 10% above the nominal regulation voltage, the MAX1540A/MAX1541 pull the respective power-good output (PGOOD_) low by turning on the MOSFET (Figure 9). Any fault condition forces both PGOOD1 and PGOOD2 low until the fault latch is cleared by toggling

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

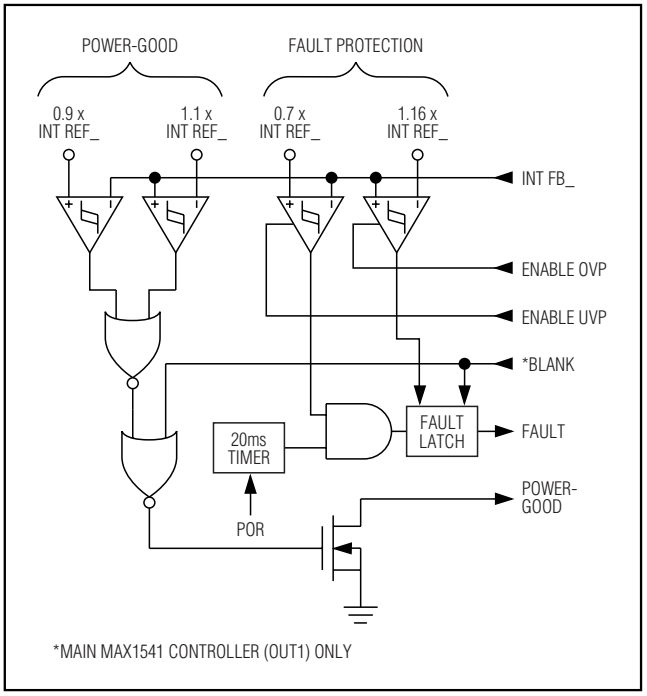


Figure 9. Power-Good and Fault Protection

ON1 or ON2, or cycling V_{CC} power below 1V. For logic-level output voltages, connect an external pullup resistor between PGOOD_ and V_{CC}. A 100kΩ resistor works well in most applications.

Note that the power-good window detectors are completely independent of the overvoltage and undervoltage-protection fault detectors.

Fault Blanking (MAX1541 FBLANK)

The main MAX1541 controller (OUT1) automatically enters forced-PWM operation during all dynamic output-voltage transitions (GATE transition detected) in order to ensure fast, accurate transitions. FBLANK determines how long the main MAX1541 controller maintains forced-PWM operation (Table 6—typically 220µs (FBLANK = V_{CC}), 140µs (FBLANK = open or GND), or 65µs (FBLANK = REF).

When fault blanking is enabled (FBLANK = V_{CC}, open, or REF), the MAX1541 also disables the overvoltage and undervoltage fault protection for OUT1, and forces PGOOD1 to a high-impedance state during the transition period selected by FBLANK (Table 6). This prevents fault protection from latching off the MAX1541 and the PGOOD1 signal from going low when the output voltage change (ΔV_{OUT1}) cannot occur as fast as the REFIN1 voltage change (ΔV_{REFIN1}).

Table 6. FBLANK Configuration Table

FBLANK	OUT1 FAULT BLANKING	FORCED-PWM DURATION (MIN/TYP) (µs)
V_{CC}	Enabled	120/220
Open	Enabled	80/140
REF	Enabled	35/65
GND	Disabled	80/140

Shutdown and Output Discharge (ON_)

When the output discharge mode is enabled (OVP/UVP connected to V_{CC} or left open), and either ON_ is pulled low or an OVP fault or thermal fault sets the fault latch (Table 7), the controller discharges each output through an internal 10Ω switch connected between OUT_ and ground. While the output discharges, DL_ is forced low and the PWM controller is disabled. Once the output voltage drops below 0.3V, the low-side driver pulls DL_ high, effectively clamping the output and LX_ switching node to ground. The reference remains active until both output voltages are below 0.3V to provide an accurate 0.3V discharge threshold.

When OVP/UVP is connected to REF or GND, the controller does not actively discharge either output, and the DL_ driver remains low until the system reenables the controller. Under these conditions, the output discharge rate is determined by the load current and output capacitance.

The controller detects and latches the discharge-mode state set by OVP/UVP on startup.

Fault Protection

The MAX1540A/MAX1541 provide over/undervoltage fault protection (Figure 9). Drive OVP/UVP to enable and disable fault protection as shown in Table 7. Once activated, the controller continuously monitors the output for undervoltage and overvoltage fault conditions.

Overvoltage Protection (OVP)

When the output voltage rises above 116% of the nominal regulation voltage and OVP is enabled (OVP/UVP = V_{CC} or open), the OVP circuit sets the fault latch, shuts down both the Quick-PWM controllers, immediately pulls DH1 and DH2 low, and forces DL1 and DL2 high. This turns on the synchronous-rectifier MOSFETs with 100% duty, rapidly discharging the output capacitors and clamping both outputs to ground. Note that immediately latching DL_ high can cause the output voltages to go slightly negative due to energy stored in the output LC at the instant the OV fault occurs. If the load

cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the input fuse blows. The MAX1541 ignores OVP faults on OUT1 when it detects a transition on GATE (FBLANK enabled). Toggle ON1 or ON2, or cycle V_{CC} power below 1V to clear the fault latch and restart the controller.

OVP is disabled when OVP/UVP is connected to REF or GND (Table 7).

Undervoltage Protection (UVP)

When the output voltage drops below 70% of the nominal regulation voltage and UVP is enabled (OVP/UVP = V_{CC} or REF), the controller sets the fault latch and activates the output discharge sequence (see the *Shutdown and Output Discharge (ON_)* section) of both outputs. When the output voltage drops to 0.3V, the driver pulls DL high so the synchronous rectifier turns on, clamping the output to GND. UVP is ignored for at least 10ms (min) after startup (ON_ rising edge), and when transitions are detected on GATE (MAX1541 only, FBLANK enabled). Toggle ON1 or ON2, or cycle V_{CC} power below 1V to clear the fault latch and restart the controller.

UVP is disabled when OVP/UVP is left open or connected to GND (Table 7).

Thermal Fault Protection

The MAX1540A/MAX1541 feature a thermal fault-protection circuit. When the linear regulator is disabled (LDOON = GND), the controller sets the thermal limit at +160°C. When the linear regulator is enabled (LDOON = V_{CC}), the controller sets the thermal limit at +150°C to protect the internal linear regulator from continuous short-circuit conditions. Once the junction temperature exceeds the thermal limit, the thermal-protection circuit activates the fault latch, pulls PGOOD1 and PGOOD2 low, disables the linear regulator, and activates the output discharge sequence of both outputs regardless of the OVP/UVP setting. Toggle ON1 or ON2, or cycle V_{CC} power below 1V to reactivate the controller after the junction temperature cools by 10°C.

Output Voltage

Preset Output Voltages

The MAX1540A/MAX1541s' Dual Mode operation allows the selection of common voltages without requiring external components (Figure 10). For the main controller (OUT1) of the MAX1540A, connect FB1 to GND for a fixed 1.8V output, to V_{CC} for a fixed 1.2V output, or connect FB1 directly to OUT1 for a fixed 0.7V output. For the secondary controller (OUT2) of the MAX1540A, connect FB2 to GND for a fixed 2.5V output, to V_{CC} for a fixed 1.5V output, or connect FB2 directly to OUT2 for a fixed 0.7V output. The main controller (OUT1) of the MAX1541 regulates to the voltage set at REFIN1 (V_{FB1} = V_{REFIN1}) and does not support Dual Mode operation. For the secondary controller (OUT2) of the MAX1541, connect FB2 to GND for a fixed 2.5V output, to V_{CC} for a fixed 1.8V output, or connect FB2 directly to OUT2 for a fixed 0.7V output. Table 8 shows the output voltage configuration.

Table 7. Fault Protection and Shutdown Setting Truth Table

OVP/UVP	ON_ DISCHARGE*	UVP PROTECTION	OVP PROTECTION	THERMAL PROTECTION
V_{CC}	Yes. Output discharged through a 10Ω resistor, and DL forced high when output drops below 0.3V.	Yes. UVP fault activates the discharge sequence.	Yes. DH pulled low and DL forced high immediately.	Yes. Thermal fault activates the discharge sequence.
Open	Yes. Output discharged through a 10Ω resistor, and DL forced high when output drops below 0.3V.	No. UVP disabled.	Yes. DH pulled low and DL forced high immediately.	Yes. Thermal fault activates the discharge sequence.
REF	No. DL forced low when shut down.	Yes. UVP fault activates the discharge sequence.	No. OVP disabled.	Yes. Thermal fault activates the discharge sequence.
GND	No. DL forced low when shut down.	No. UVP disabled.	No. OVP disabled.	Yes. Thermal fault activates the discharge sequence.

**Discharge-mode state latched on power-up.*

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

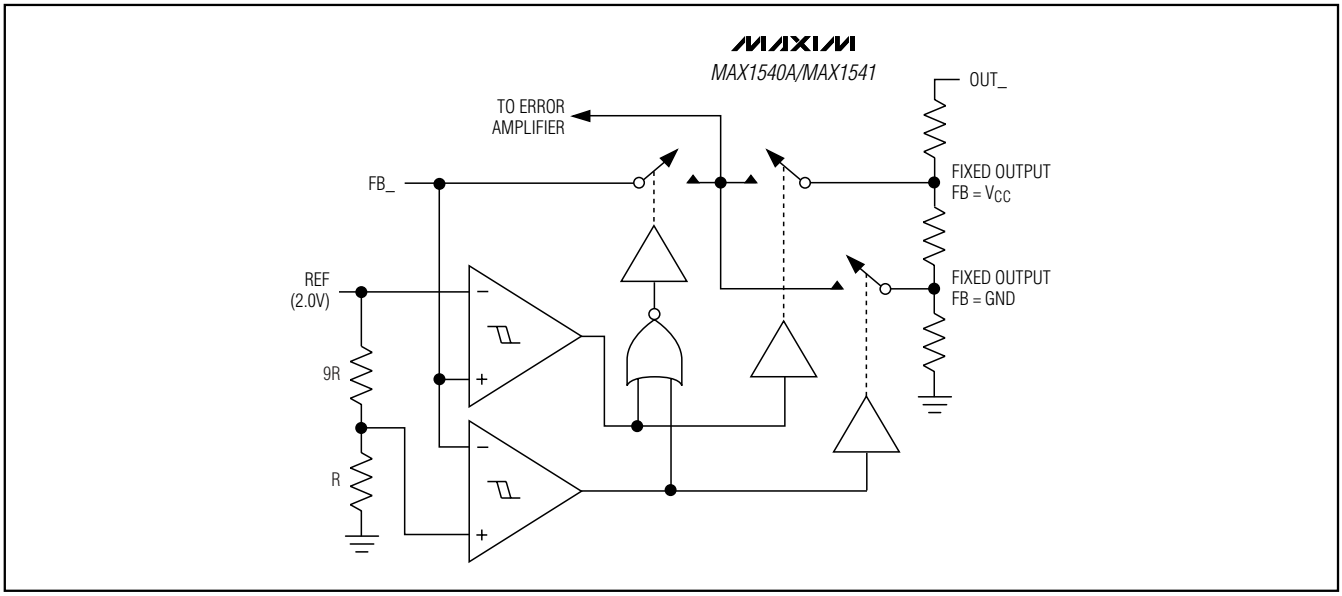


Figure 10. MAX1540A/MAX1541 Dual Mode Feedback Decoder

Table 8. Output Voltage Configuration

	OUT1		OUT2	
	MAX1540A	**MAX1541**	**MAX1540A**	**MAX1541**
FB_ = V_{CC}	Fixed 1.2V	Not allowed	Fixed 1.5V	Fixed 1.8V
FB_ = GND	Fixed 1.8V	Not allowed	Fixed 2.5V	Fixed 2.5V
FB_ = OUT_ or adjustable	0.7V	V_{REFIN1}	0.7V	0.7V

*Setting V_{OUT} with a Resistive Voltage-Divider at FB_*

The output voltage can be adjusted from 0.7V to 5.5V using a resistive voltage-divider (Figure 11). The MAX1540A regulates FB1 and FB2 to a fixed 0.7V reference voltage. The MAX1541 regulates FB1 to the voltage set at REFIN1 and regulates FB2 to a fixed 0.7V reference voltage. This makes the main MAX1541 controller (OUT1) ideal for memory applications where the termination supply must track the supply voltage. The adjusted output voltage is:

$$V_{OUT\_} = V_{FB\_}\left(1+\frac{R_C}{R_D}\right)$$

where $V_{FB\_}$ = 0.7V for the MAX1540A, and V_{FB1} = V_{REFIN1} and V_{FB2} = 0.7V for the MAX1541.

Dynamic Output Voltages (MAX1541 OUT1 Only)

The MAX1541 regulates FB1 to the voltage set at REFIN1. By changing the voltage at REFIN1, the MAX1541 can be used in applications that require dynamic output-voltage changes between two set points. Figure 12 shows a dynamically adjustable resistive voltage-divider network at REFIN1. Using the GATE signal and open-drain output (OD), a resistor can be switched in and out of the REFIN1 resistor-divider, changing the voltage at REFIN1. A logic high on GATE turns on the internal N-channel MOSFET, forcing OD to a low-impedance state. A logic low on GATE disables the N-channel MOSFET, so OD is high impedance. The two output voltages (FB1 = OUT1) are determined by the following equations:

$$V_{OUT1(LOW)} = V_{REF}\left(\frac{R9}{R8+R9}\right)$$

$$V_{OUT1(HIGH)} = V_{REF}\left[\frac{(R9+R10)}{R8+(R9+R10)}\right]$$

The main MAX1541 controller (OUT1) automatically enters forced-PWM operation on the rising and falling edges of GATE, and remains in forced-PWM mode for a minimum time selected by FBLANK (Table 6). Forced-PWM operation is required to ensure fast, accurate negative voltage transitions when REFIN1 is lowered. Since forced-PWM operation disables the zero-crossing comparator, the inductor current may reverse under

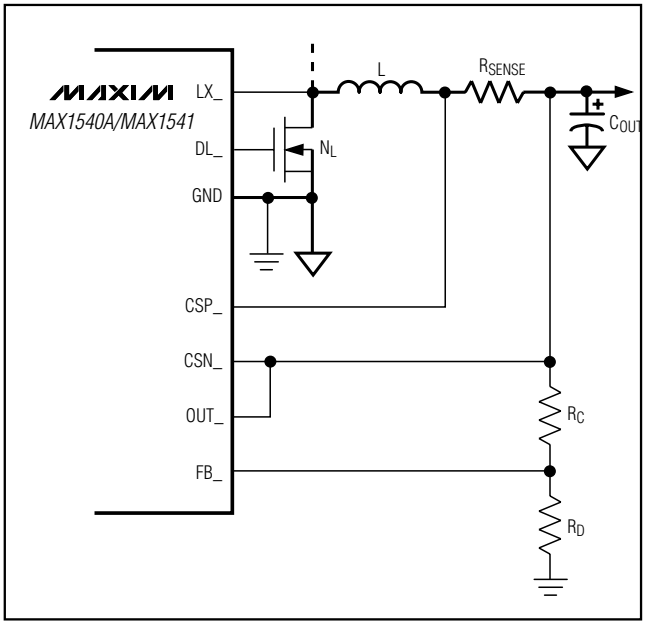


*Figure 11. Setting V_{OUT} with a Resistive Voltage-Divider at FB_*

light loads, quickly discharging the output capacitors. If fault blanking is enabled, the MAX1541 also disables the main controller's (OUT1) overvoltage and undervoltage fault protection, and forces PGOOD1 to a high-impedance state for the period selected by FBLANK (Table 6).

For a step-voltage change at REFIN1, the rate of change of the output voltage is limited by the inductor current ramp, the total output capacitance, the current limit, and the load during the transition. The inductor current ramp is limited by the voltage across the inductor and the inductance. The total output capacitance determines how much current is needed to change the output voltage. Additional load current slows down the output-voltage change during a positive REFIN1 voltage change, and speeds up the output-voltage change during a negative REFIN1 voltage change. For fast positive output-voltage transitions, the current limit must be greater than the load current plus the transition current:

$$I_{LIMIT} > I_{LOAD} + C_{OUT}\frac{dV}{d_t}$$

Adding a capacitor across REFIN1 and GND filters noise and controls the rate of change of the REFIN1 voltage during dynamic transitions. With the additional capacitance, the REFIN1 voltage slews between the two set points with a time constant given by R_{EQ} x C_{REFIN1}, where R_{EQ} is the equivalent parallel resistance seen by the slew capacitor. Looking at Figure 12, the time constant for a positive REFIN1 voltage transition is:

$$\tau_{POS} = \left[\frac{R8\times(R9+R10)}{R8+(R9+R10)}\right]C_{REFIN1}$$

and the time constant for a negative REFIN1 voltage transition is:

$$\tau_{NEG} = \left(\frac{R8\times R9}{R8+R9}\right)C_{REFIN1}$$

Linear Regulator (LDO)

The maximum input voltage for the linear regulator is 28V, while the minimum input voltage is determined by the 800mV (max) dropout voltage ($V_{LDOIN(MIN)}$ = V_{LDOOUT} + $V_{DROPOUT}$) at 50mA load. Bypass the linear regulator's output (LDOOUT) with a 4.7µF or greater capacitor, providing at least 1µF per 5mA of internal and external load on the linear regulator. The LDO can source up to 100mA for powering the controller or supplying a small external load.

For the MAX1540A, the linear regulator provides the 5V bias supply that powers the gate drivers and analog controller (Figure 1), providing stand-alone capability. The linear regulator's input is internally connected to the battery voltage input (LDOIN = V+), and the gate-driver input supply is internally connected to the linear regulator's output (V_{DD} = LDOOUT). Figure 13 is the internal linear-regulator functional diagram.

For the MAX1541, the linear regulator supports Dual Mode operation to allow the selection of a 5V output voltage without requiring external components (Figure 1). Connect FBLDO to GND for a fixed 5.0V output. The linear regulator's output voltage can be adjusted from 1.25V to 5.5V using a resistive voltage-divider (Figure 12). The MAX1541 regulates FBLDO to a 1.25V feedback voltage. The adjusted output voltage is:

$$V_{LDOOUT} = V_{FBLDO}\left(1+\frac{R11}{R12}\right)$$

where V_{FBLDO} = 1.25V. If unused, disable the MAX1541 linear regulator by connecting LDOON to GND.

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

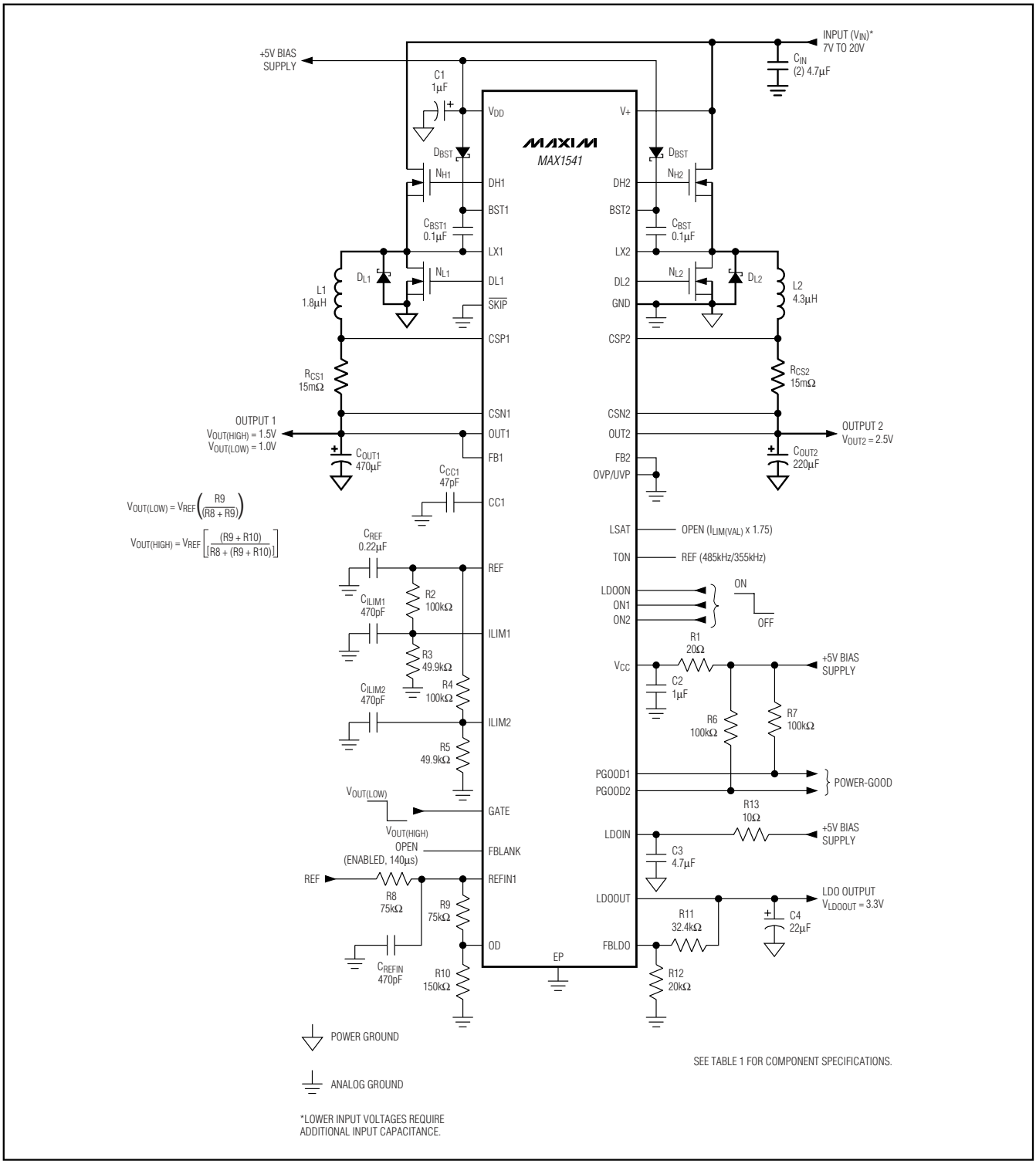


Figure 12. MAX1541 Standard Application Circuit

MAXIM

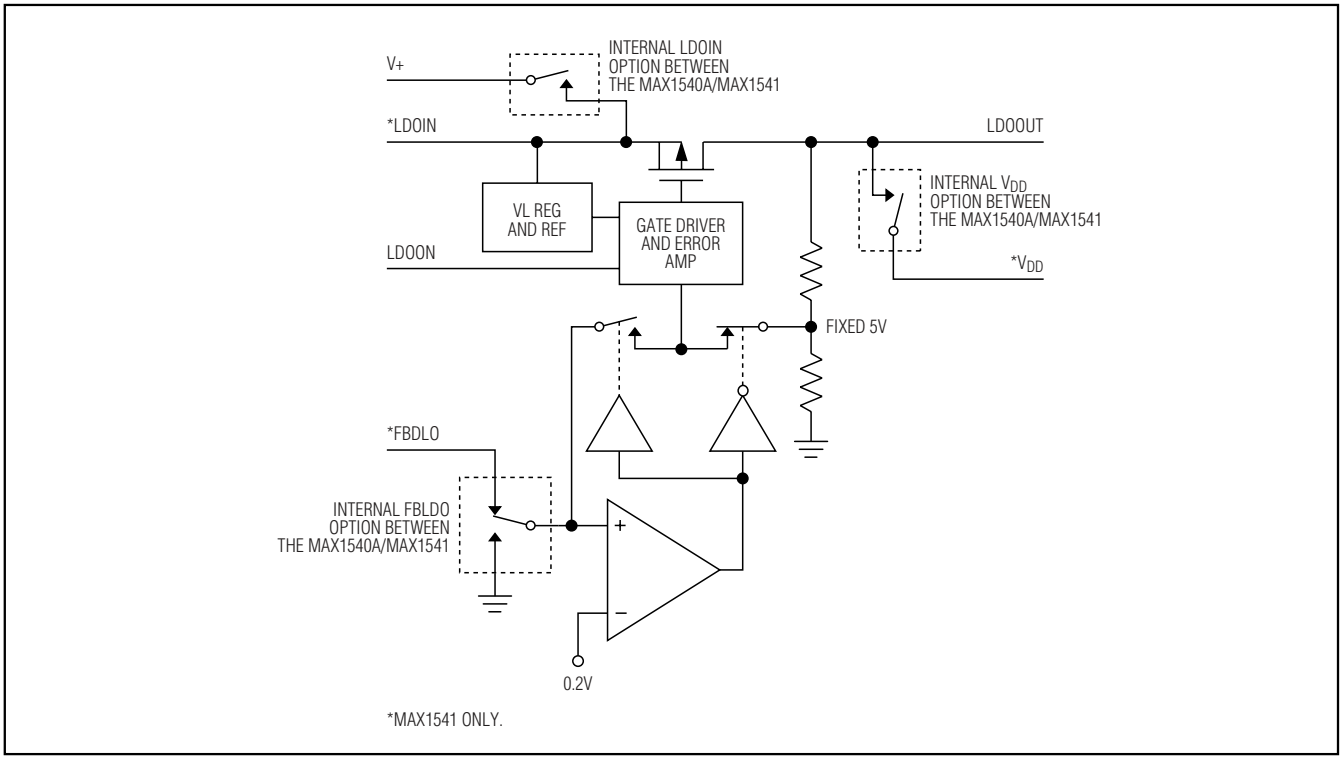


Figure 13. Internal Linear-Regulator Functional Diagram

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN2}. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping ($\overline{SKIP}$ low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

For example: $I_{LOAD(MAX)}$ = 4A, V_{IN} = 12V, V_{OUT2} = 2.5V, f_{SW} = 355kHz, 30% ripple current or LIR = 0.3:

$$L = \frac{2.5V \times (12V - 2.5V)}{12V \times 355kHz \times 4A \times 0.3} = 4.65\mu H$$

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)}\left(1 + \frac{LIR}{2}\right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2\left[\left(\frac{V_{OUT} \times K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT} \times V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT}) \times K}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics*) and K is from Table 3.

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT} \times V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{LIM(VAL)} > I_{LOAD(MAX)} - \left(\frac{V_{OUT}(V_{IN(MIN)} - V_{OUT})}{2V_{IN(MIN)} \ f_{SW} \ L}\right)$$

where $I_{LIM(VAL)}$ equals the minimum valley current-limit threshold voltage divided by the current-sense resistance (R_{SENSE}). For the 50mV default setting, the minimum valley current-limit threshold is 40mV.

Connect ILIM_ to V_{CC} for a default 50mV valley current-limit threshold. In adjustable mode, the valley current-limit threshold is precisely 1/10th the voltage seen at ILIM_. For an adjustable threshold, connect a resistive divider from REF to analog ground (GND) with ILIM_ connected to the center tap. The external 250mV to 2V adjustment range corresponds to a 25mV to 200mV valley current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately 10µA to prevent significant inaccuracy in the valley current-limit tolerance.

The current-sense method (Figure 14) and magnitude determine the achievable current-limit accuracy and power loss (Table 9). Typically, higher current-sense voltage limits provide tighter accuracy, but also dissipate more power. Most applications employ a valley current-sense voltage ($V_{LIM(VAL)}$) of 50mV to 100mV, so the sense resistor may be determined by:

$$R_{SENSE} = V_{LIM(VAL)} / I_{LIM(VAL)}$$

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 14a. This configuration constantly monitors the inductor current, allowing accurate valley current-limiting and inductor-saturation protection.

For low-output-voltage applications that require higher efficiency, the current-sense resistor can be connected between the source of the low-side MOSFET ($N_{L\_}$) and power ground (Figure 14b) with CSN_ connected to the drain of $N_{L\_}$ and CSP_ connected to power ground. In this configuration, the additional current-sense resistance only dissipates power when $N_{L\_}$ is conducting current. Inductor-saturation protection must be disabled with this configuration (LSAT = GND) since the inductor current is only properly sensed when the low-side MOSFET is turned on.

For high-power applications that do not require high-accuracy current sensing or inductor-saturation protection, the MAX1540A/MAX1541 can use the low-side MOSFET's on-resistance as the current-sense element ($R_{SENSE} = R_{DS(ON)}$) by connecting CSN_ to the drain of $N_{L\_}$ and CSP_ to the source of $N_{L\_}$ (Figure 14c). Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise. Inductor-saturation protection must be disabled with this configuration (LSAT = GND) since the inductor current is only properly sensed when the low-side MOSFET is turned on.

Alternatively, high-power applications that require inductor saturation can constantly detect the inductor current by connecting a series RC circuit across the inductor (Figure 14d) with an equivalent time constant:

$$\frac{L}{R_L} = C_{EQ} \times R_{EQ}$$

where R_L is the inductor's series DC resistance. In this configuration, the current-sense resistance is equivalent to the inductor's DC resistance ($R_{SENSE} = R_L$). Use the worst-case inductance and R_L values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

In all cases, ensure an acceptable valley current-limit threshold voltage and inductor-saturation configurations despite inaccuracies in sense-resistance values.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For processor-core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. Therefore, the maximum ESR required to meet ripple specifications is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\Delta I_{LOAD(MAX)} \times LIR}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high-ESR zeros that may affect the overall stability (see the *Output-Capacitor Stability Considerations* section).

Table 9. Current-Sense Configurations

METHOD	CURRENT-SENSE ACCURACY	INDUCTOR-SATURATION PROTECTION	CURRENT-SENSE POWER LOSS (EFFICIENCY)
a) Output current-sense resistor	High	Allowed (highest accuracy)	$R_{SENSE} \times I_{OUT}^2$
b) Low-side current-sense resistor	High	Not allowed (LSAT = GND)	$\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{SENSE} \times I_{OUT}^2$
c) Low-side MOSFET on-resistance	Low	Not allowed (LSAT = GND)	No additional loss
d) Equivalent inductor DC resistance	Low	Allowed	No additional loss

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

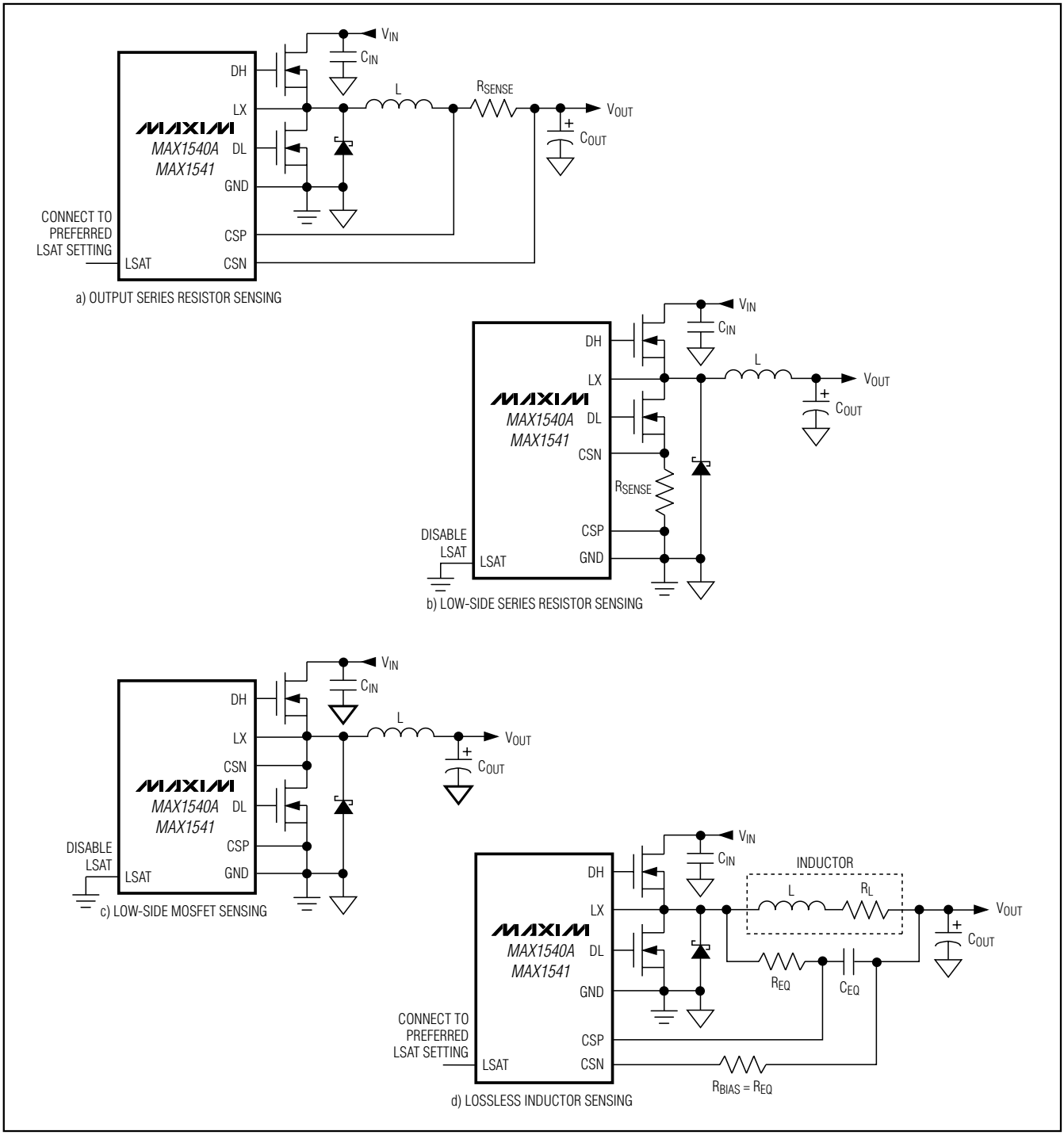


Figure 14. Current-Sense Configurations

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Output-Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \leq \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support 25mV$_{P-P}$ ripple is 25mV/1.2A = 20.8mΩ. One 220µF/4V Sanyo polymer (TPE) capacitor provides 15mΩ (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and fast-feedback loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to monitor simultaneously the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input-Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents:

$$I_{RMS} = \frac{\sqrt{\sum_{X=1}^{2} I^2_{OUTX} \, V_{OUTX} \, (V_{IN} - V_{OUTX})}}{V_{IN}}$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX1540A/MAX1541 are operated as the second stage of a two-stage power conversion system, tantalum input capacitors are acceptable. In either configuration, choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H.

Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D^{2}PAK), and is reasonably priced. Ensure that the MAX1540A/MAX1541 DL_ gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Power-MOSFET Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD\,(N_H\ Resistance) = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{LOAD})^2 \times R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often restricts how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\,(N_H\ Switching) = \frac{(V_{IN(MAX)})^2 C_{RSS} \times f_{SW} \times I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of N_H, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied due to the squared term in the switching-loss equation ($C \times V_{IN}^2 \times f_{SW}$). If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low-battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD\,(N_L\ Resistance) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right](I_{LOAD})^2 \times R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than $I_{LOAD(MAX)}$ but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{VALLEY(MAX)} + \left(\frac{V_{OUT}(V_{IN} - V_{OUT})}{2V_{IN}\ f_{SW}\ L}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward-voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 the load current. This diode is optional and can be removed if efficiency is not critical.

Applications Information

Step-Down Converter Dropout Performance

The output-voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time setting. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 3). Also, keep in mind that transient-response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ indicates the controller's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle, and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{DROP1}}{1-\left(\frac{h \times t_{OFF(MIN)}}{K}\right)}$$

where V_{DROP1} is the parasitic voltage drop in the charge path (see the *On-Time One-Shot (TON)* section), $t_{OFF(MIN)}$ is from the *Electrical Characteristics*, and K is taken from Table 3. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example

- V_{OUT2} = 2.5V
- f_{SW} = 355kHz
- K = 3.0µs, worst-case K_{MIN} = 3.3µs
- $t_{OFF(MIN)}$ = 500ns
- V_{DROP1} = 100mV
- h = 1.5

$$V_{IN(MIN)} = \frac{2.5V + 0.1V}{1-\left(\frac{1.5 \times 500ns}{3.0\mu s}\right)} = 3.47V$$

Calculating again with h = 1 and the typical K-factor value (K = 3.3µs) gives the absolute limit of dropout:

$$V_{IN(MIN)} = \frac{2.5V + 0.1V}{1-\left(\frac{1 \times 500ns}{3.3\mu s}\right)} = 3.06V$$

Therefore, V_{IN} must be greater than 3.06V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 3.47V.

Multi-Output Voltage Settings (MAX1541 OUT1 Only)

While the main MAX1541 controller (OUT1) is optimized to work with applications that require two dynamic output voltages, it can produce three or more output voltages if required by using discrete logic or a DAC.

Figure 15 shows an application circuit providing four voltage levels using discrete logic. Switching resistors in and out of the resistor network changes the voltage at REFIN1. An edge-detection circuit is added to generate a 1µs pulse on GATE to trigger the fault blanking and forced-PWM operation. When using PWM mode ($\overline{SKIP}$ = V_{CC} or open) on the main controller, the edge-detection circuit is only required if fault blanking is enabled. Otherwise, leave OD unconnected.

Active Bus Termination (MAX1541 OUT1 Only)

Active-bus-termination power supplies generate a voltage rail that tracks a set reference. They are required to source and sink current. DDR memory architecture requires active bus termination. In DDR memory architecture, the termination voltage is set at exactly half the memory supply voltage. Configure the main MAX1541 controller (OUT1) to generate the termination voltage using a resistive voltage-divider at REFIN1. In such an application, the main MAX1541 controller (OUT1) must be kept in PWM mode ($\overline{SKIP}$ = V_{CC} or open) in order for it to source and sink current. Figure 16 shows the main MAX1541 controller configured as a DDR termination regulator. Connect GATE and FBLANK to GND when unused.

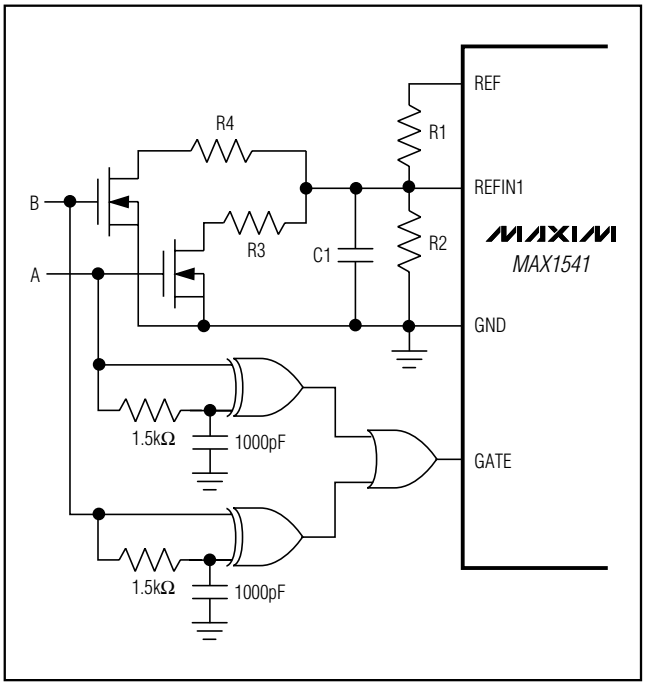


Figure 15. Multi-Output Voltage Settings

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

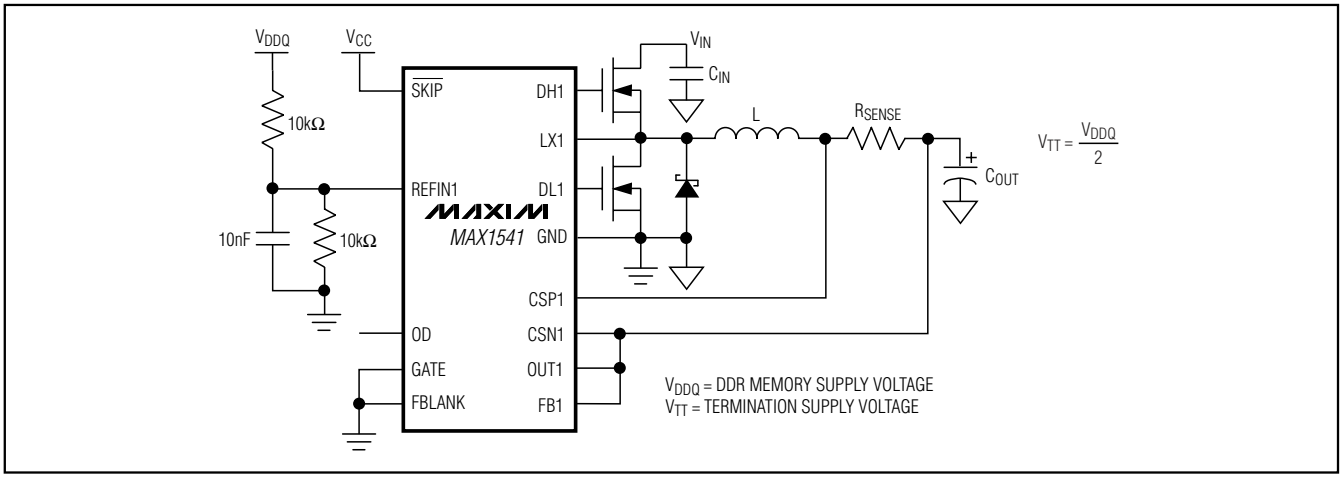


Figure 16. Active Bus Termination

Voltage Positioning

In applications where fast load transients occur, the output voltage changes instantly by $ESR_{COUT} \times \Delta I_{LOAD}$. Voltage positioning allows the use of fewer output capacitors for such applications, and maximizes the output voltage AC and DC tolerance window in tight-tolerance applications.

Figure 17 shows the connection of OUT_ and FB_ in voltage-positioned and nonvoltage-positioned circuits. In nonvoltage-positioned circuits, the MAX1540A/MAX1541 regulate at the output capacitor. In voltage-positioned circuits, the MAX1540A/MAX1541 regulate on the inductor side of the current-sense resistor. $V_{OUT\_}$ is reduced to:

$$V_{OUT(VPS)} = V_{OUT(NO\ LOAD)} - R_{SENSE} \times I_{LOAD}$$

Figure 18 shows the voltage-positioning transient response.

PC Board Layout Guidelines

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 19). If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting CSP_ and CSN_ directly across the current-sense resistor ($R_{SENSE\_}$).
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (REF, FB_, CSP_, CSN_).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (N_{L} _ source, C_{IN}, $C_{OUT\_}$, and D_{L} _ anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite N_{L} _ and $N_{H\_}$ in order to keep LX_, GND, DH_, and the DL_ gate-drive lines short and wide. The DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.

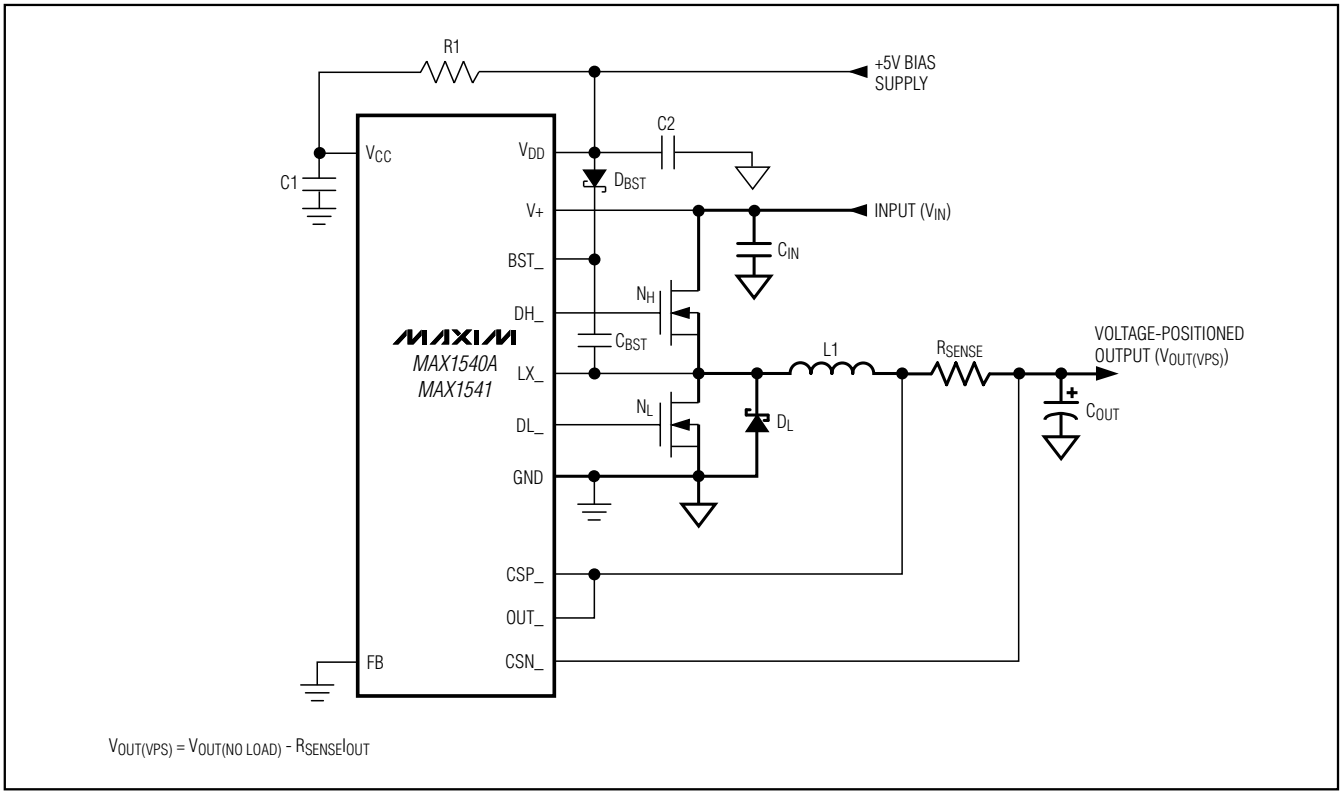


Figure 17. Voltage Positioning

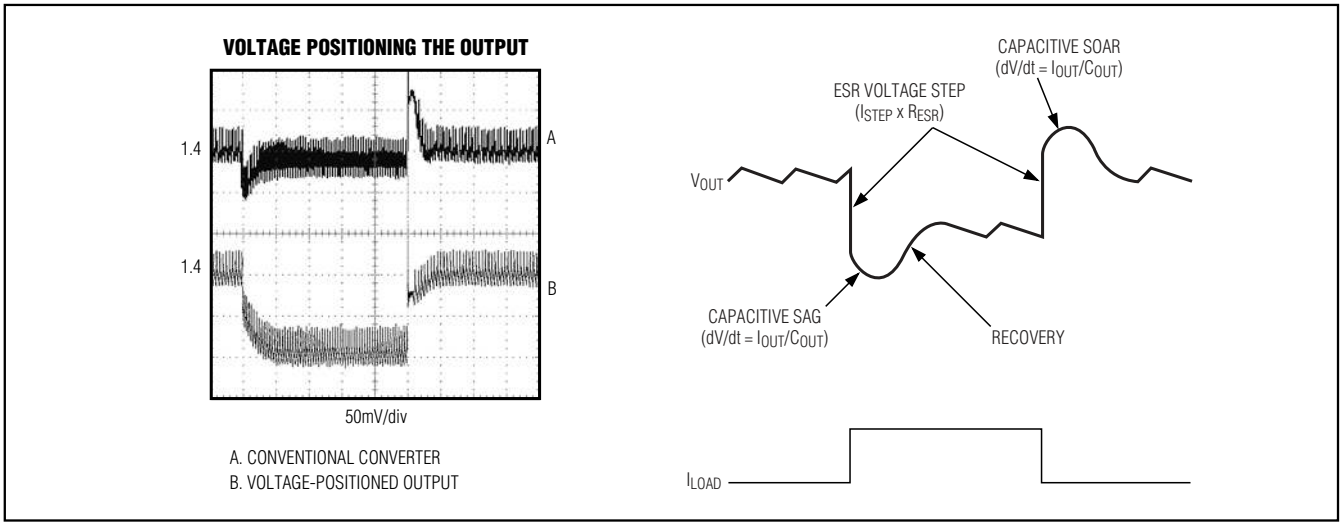


Figure 18. Voltage-Positioning Transient Response

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

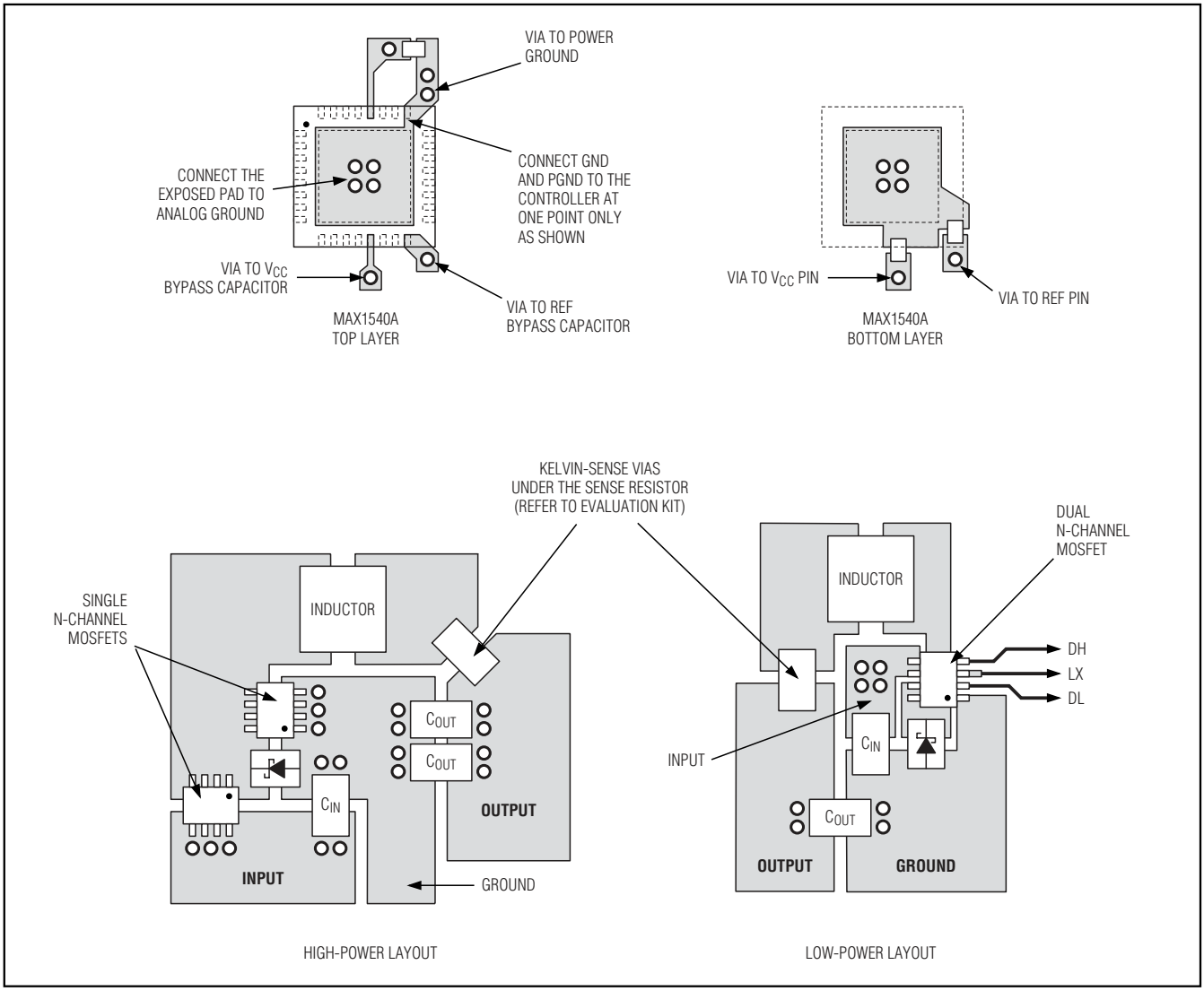


Figure 19. PC Board Layout

3) Group the gate-drive components (BST_ diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.

4) Make the DC-DC controller ground connections as shown in Figures 1 and 12. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go, and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.

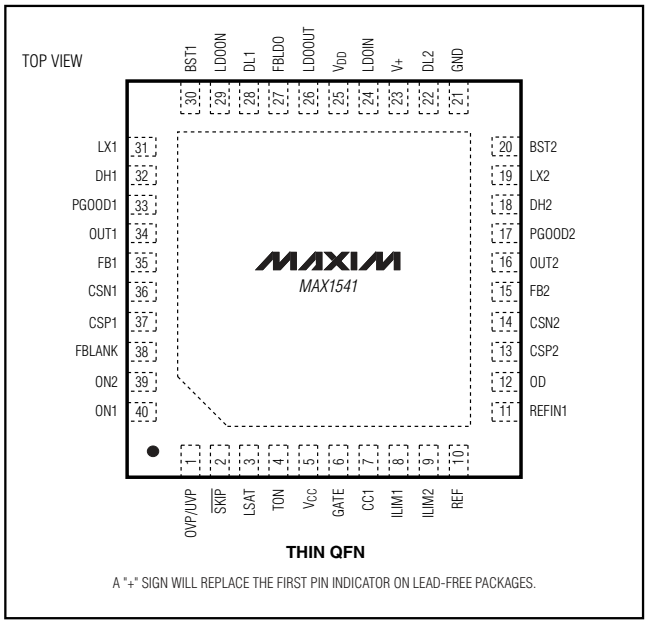
5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

Chip Information

TRANSISTOR COUNT: 8612

PROCESS: BiCMOS

Pin Configurations (continued)



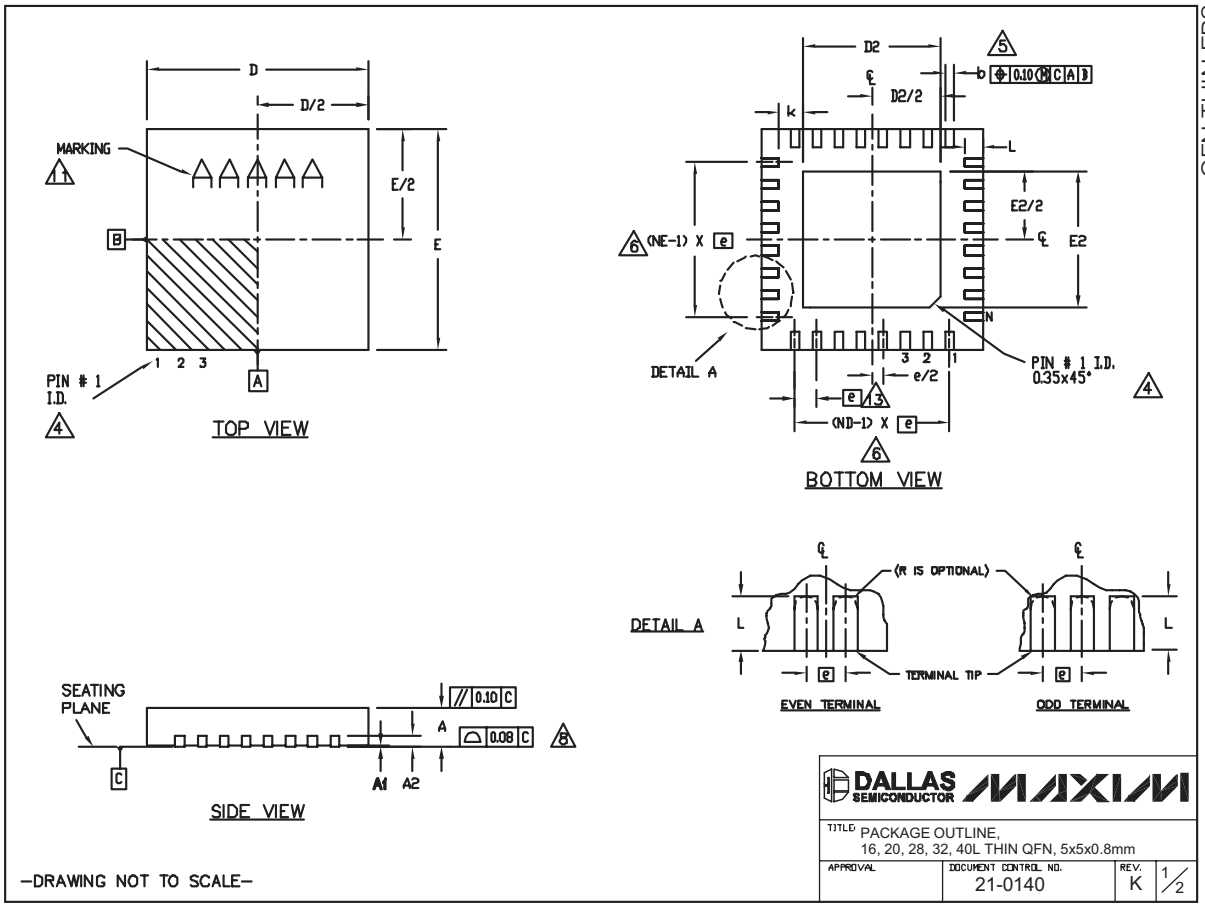
THIN QFN

A "+" SIGN WILL REPLACE THE FIRST PIN INDICATOR ON LEAD-FREE PACKAGES.

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

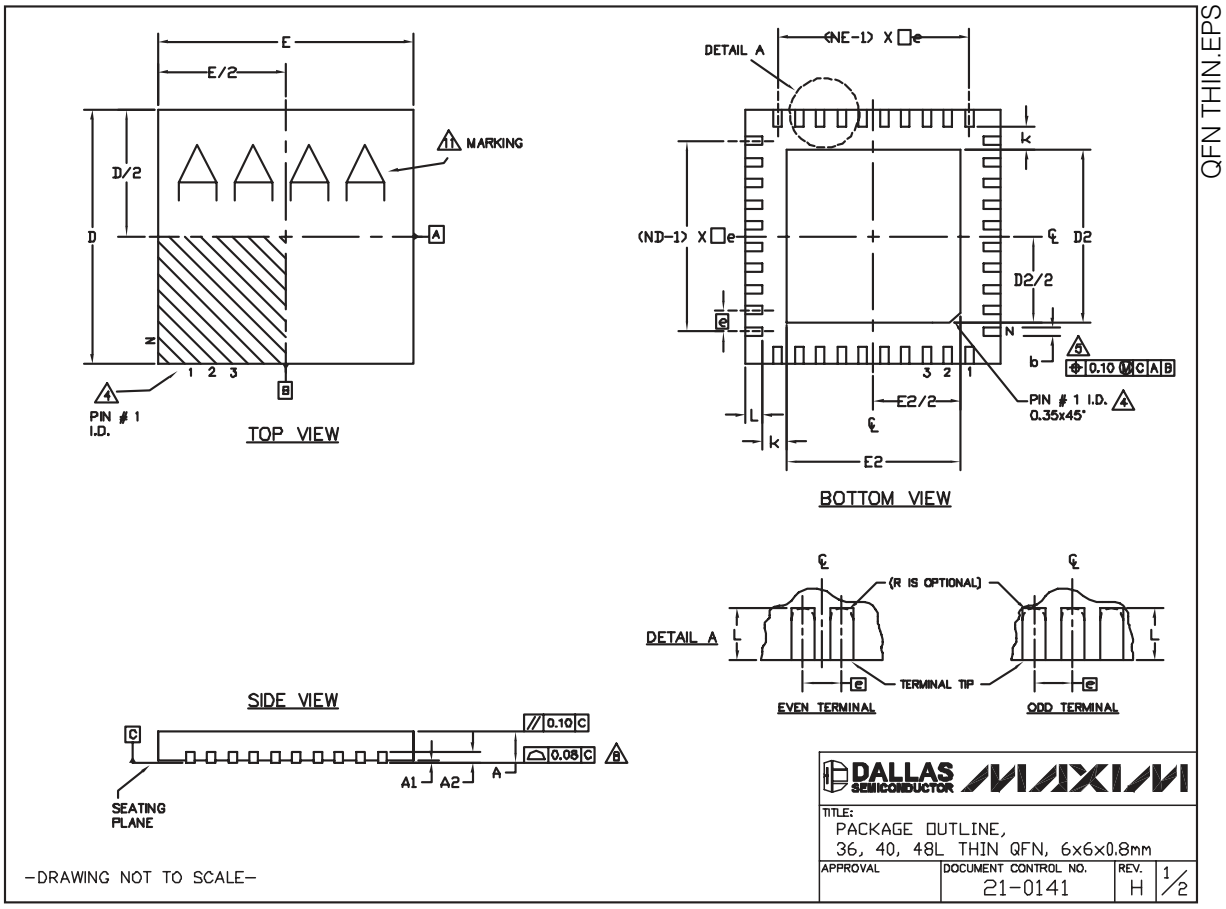
TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	K	2/2

Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Dual Step-Down Controllers with Saturation Protection, Dynamic Output, and Linear Regulator

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	H	2/2

Revision History

Pages changed at Rev 3: 1, 10–15, 18, 20, 21, 22, 24, 34, 46–49