![Integrated Device Technology, Inc. logo]

512K x 8
CMOS STATIC RAM MODULE

IDT7M4048

FEATURES:
- High-density 4 megabit CMOS Static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 StaticRAMs
- Fast access time: 25ns (max.)
- Surface mounted LCCs (leadless chip carriers) on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
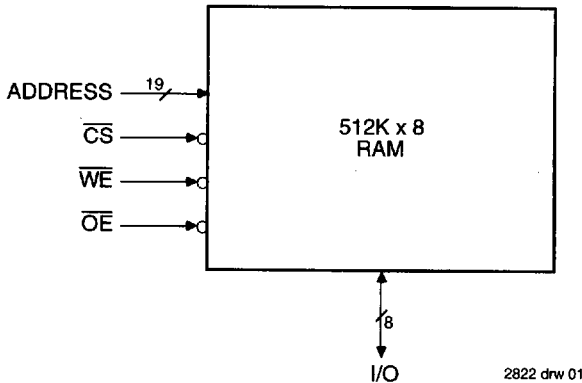- Inputs/outputs directly TTL-compatible

DESCRIPTION:
The IDT7M4048 is a 4 megabit (512K x 8) CMOS Static RAM module constructed on a co-fired ceramic substrate using four 1 Megabit StaticRAMs and a decoder. The IDT7M4048 is available with access times as fast as 25ns.

The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 4 megabits into the JEDEC DIP footprint.

All inputs and outputs of the IDT7M4048 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

ADDRESS — 19 →
$\overline{CS}$ →
$\overline{WE}$ →
$\overline{OE}$ →

512K x 8
RAM

8
I/O   2822 drw 01

7

MILITARY TEMPERATURE RANGE

DSC-2822/4

4825771 0021255 632

PIN CONFIGURATION

```
        A18 ┌ 1      32 ┐ Vcc
        A16 ┌ 2      31 ┐ A15
        A14 ┌ 3      30 ┐ A17
        A12 ┌ 4      29 ┐ WE
         A7 ┌ 5      28 ┐ A13
         A6 ┌ 6      27 ┐ A8
         A5 ┌ 7      26 ┐ A9
         A4 ┌ 8      25 ┐ A11
         A3 ┌ 9      24 ┐ OE
         A2 ┌ 10     23 ┐ A10
         A1 ┌ 11     22 ┐ CS
         A0 ┌ 12     21 ┐ I/O7
       I/O0 ┌ 13     20 ┐ I/O6
       I/O1 ┌ 14     19 ┐ I/O5
       I/O2 ┌ 15     18 ┐ I/O4
        GND ┌ 16     17 ┐ I/O3
```

2822 drw 02

DIP
TOP VIEW

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2822 tbl 01

CAPACITANCE[1] ($T_A = +25°C$, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	50	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	$V_{IN} = 0V$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	40	pF

NOTE: 2822 tbl 02
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	$-0.5^{(1)}$	—	0.8	V

NOTE: 2822 tbl 03
1. $V_{IL} = -1.5V$ for pulse width less than 10ns.

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2822 tbl 04

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +160	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2822 tbl 05
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for ex-tended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%

2822 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Test Conditions	7M4048SxxCB		Unit
			Min.	Max.	
I_{ILI}	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
I_{ILOI}	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ ≤ V_{IL}; f = f_{MAX}, Outputs Open	—	300	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	160	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V, V_{CC} = Max., f = 0, Outputs Open	—	85	mA

2822 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2822 tbl 08
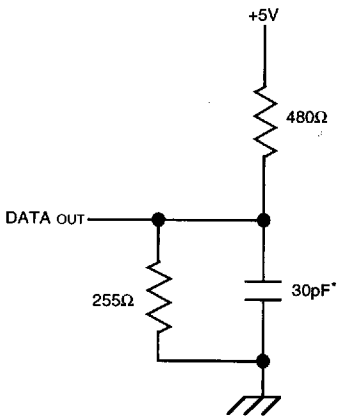
Figure 1. Output Load
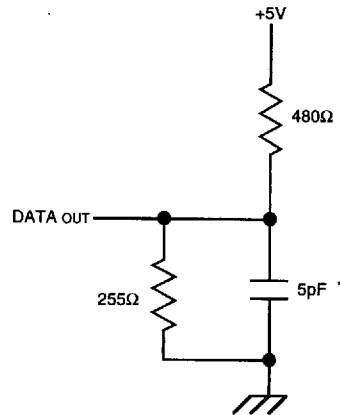
Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, tow and t_{CLZ})

* Including scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

| Symbol	Parameter	7M4048SxxCB						Unit
		-25[3]		-30		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	12	—	12	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	·3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	17	—	20	—	25	—	ns
t_{AS}[2]	Address Set-up Time	3	—	3	—	3	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End-of-Write	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	20	—	ns
t_{DH}[2]	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}[2]	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	15	—	15	—	15	ns
t_{OW}[1]	Output Active from End-of-Write	3	—	3	—	3	—	ns

NOTES:
2822 tbl 09
1. This parameter is guaranteed by design, but not tested.
2. t_{AS} = 0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR} = 3ns for $\overline{CS}$ controlled write cycles.
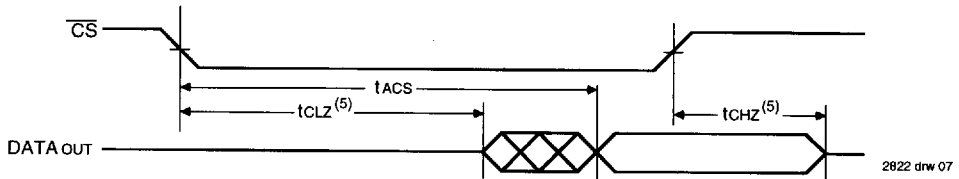3. Preliminary specifications only.

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TIMING WAVEFORM OF READ CYCLE NO. 1[1]

2822 drw 05
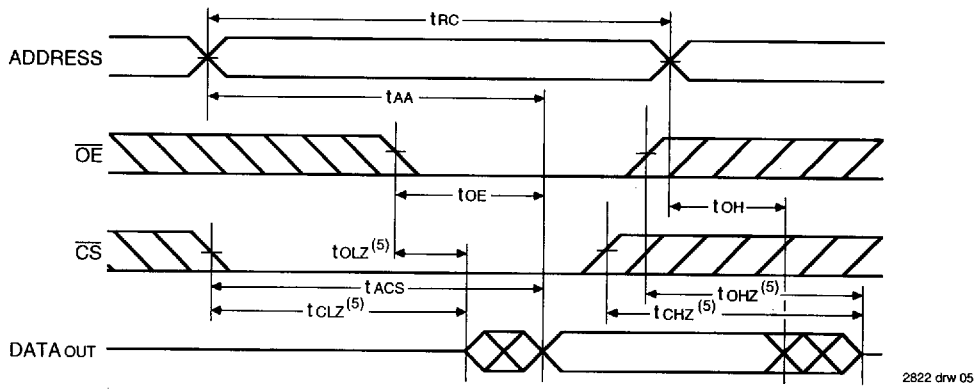
TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]

2822 drw 06
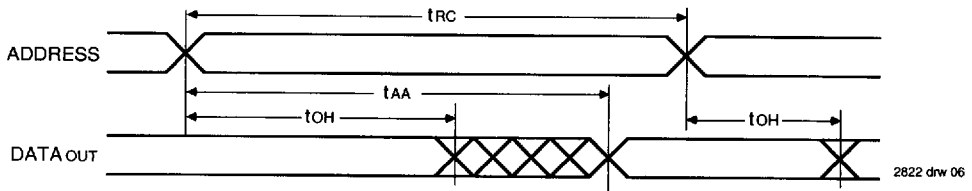
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]
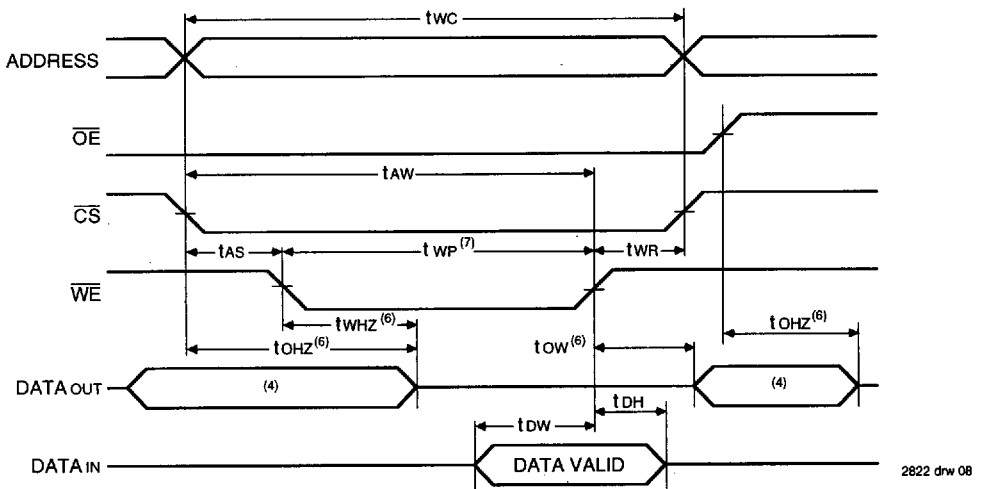

2822 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
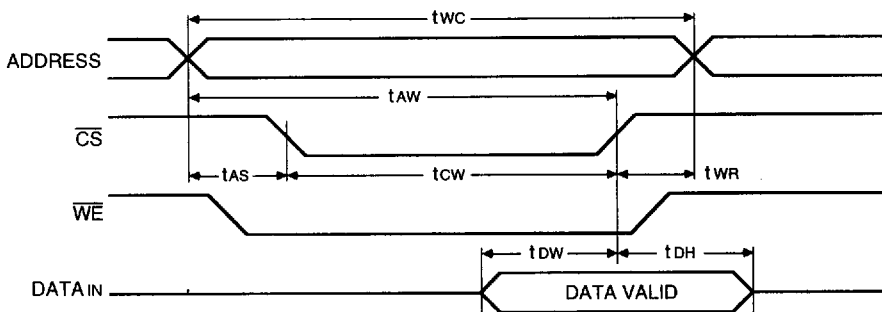5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]

2822 drw 08

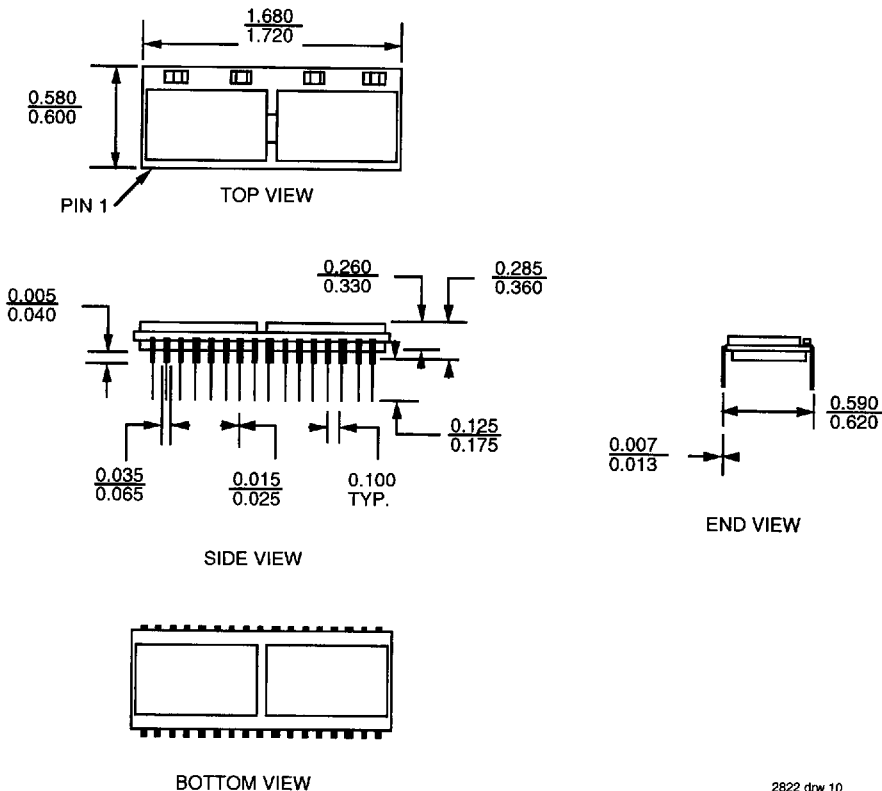## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]
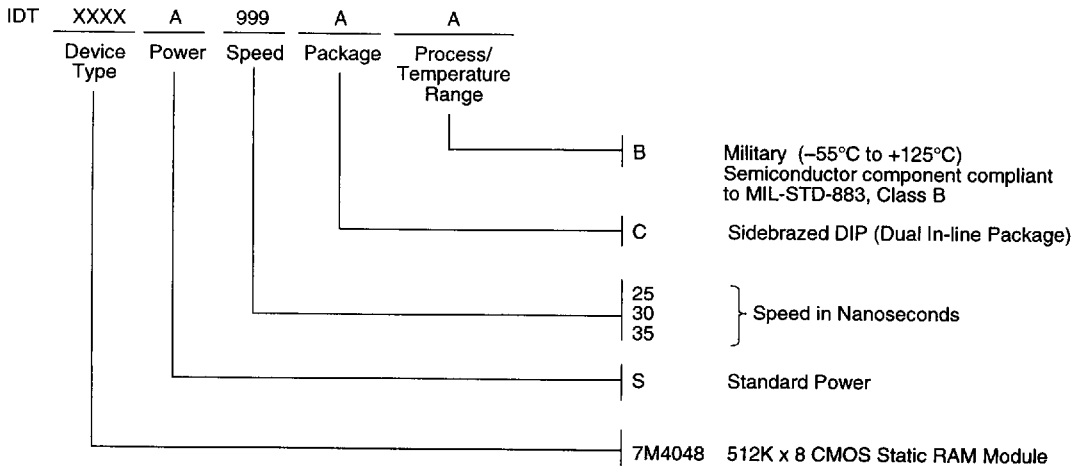

2822 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

PACKAGE DIMENSIONS

$$\frac{1.680}{1.720}$$

$$\frac{0.580}{0.600}$$

PIN 1

TOP VIEW

$$\frac{0.005}{0.040}$$

$$\frac{0.260}{0.330}$$

$$\frac{0.285}{0.360}$$

$$\frac{0.125}{0.175}$$

$$\frac{0.035}{0.065}$$

$$\frac{0.015}{0.025}$$

0.100
TYP.

SIDE VIEW

$$\frac{0.590}{0.620}$$

$$\frac{0.007}{0.013}$$

END VIEW

BOTTOM VIEW

2822 drw 10

ORDERING INFORMATION

```
IDT    XXXX    A    999    A        A
       Device  Power Speed Package  Process/
       Type                         Temperature
                                    Range
```

B	Military (–55°C to +125°C) Semiconductor component compliant to MIL-STD-883, Class B
C	Sidebrazed DIP (Dual In-line Package)
25 30 35	Speed in Nanoseconds
S	Standard Power
7M4048	512K x 8 CMOS Static RAM Module

2822 drw 11