ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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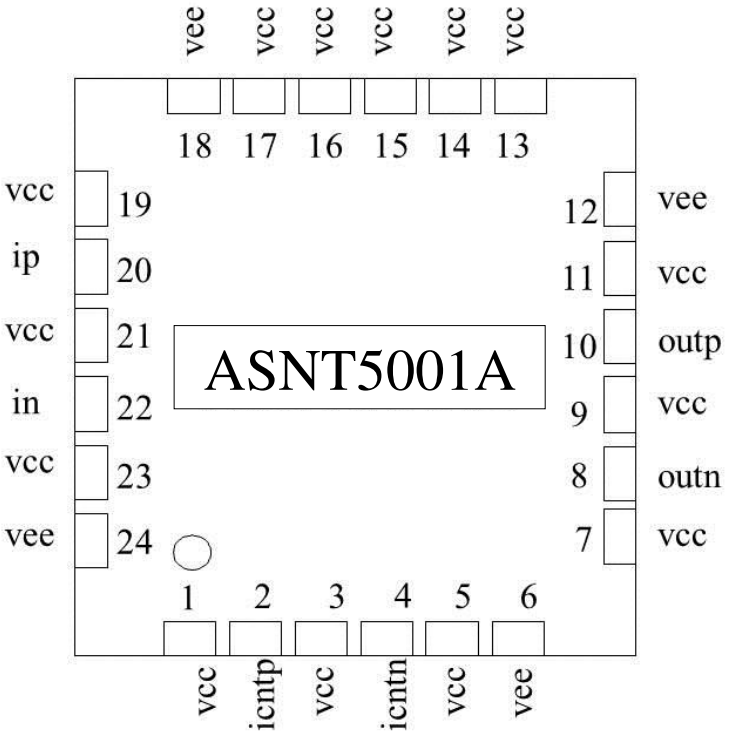
ASNT5001A-PQC

DC-32*Gbps*/17*GHz* Signal Phase Shifter with Linearized OB

- Broadband (DC-32*Gbps* / 17*GHz*) tunable data/clock phase shifter
- Delay adjustment range of 265*ps*
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 1*GHz* of bandwidth for the phase adjustment tuning port
- Fully differential CML input interface
- Fully differential CML output interface with 600*mV* single-ended swing
- Linearized data output for minimized undershoot/overshoot.
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.17*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 24-pin package



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DESCRIPTION

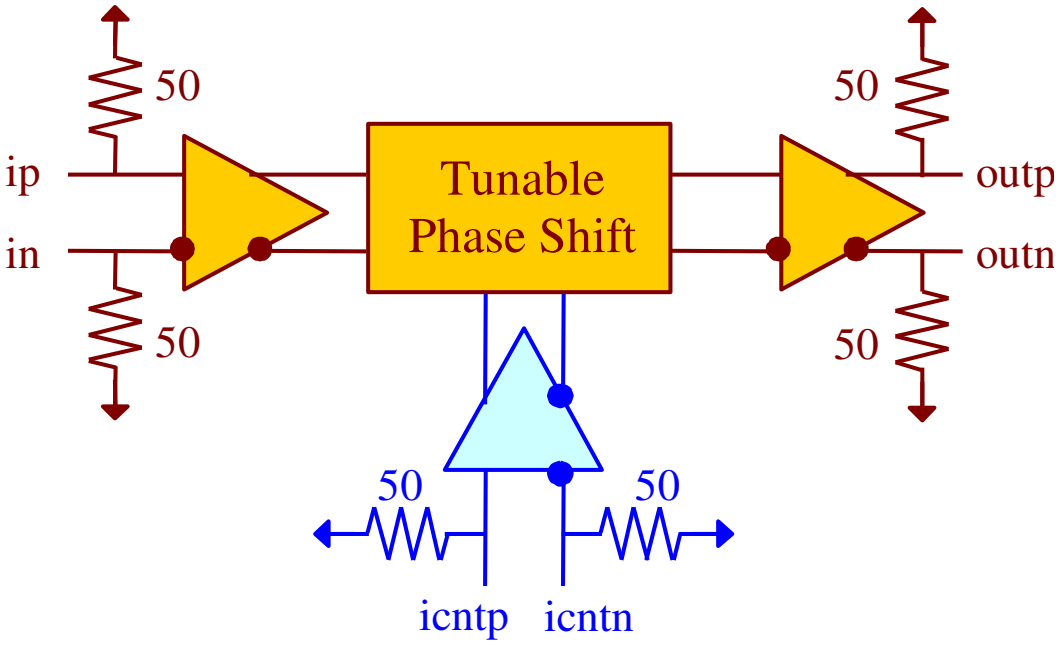

Fig. 1. Functional Block Diagram

ASNT5001A-PQC is a data / clock variable delay line fabricated in a SiGe technology. The IC shown in Fig. 1 provides an adjustable delay of its differential output signal outp/outn in relation to its broadband input signal ip/in. The delay adjustment range is temperature-stabilized. The delay is controlled through a wide-band differential tuning port icntp/icntn.

The part's I/Os support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

The output buffer is linearized for reduction of undershoot and overshoot on the output waveforms. Due to an extremely low jitter, the part is suitable for use in high-speed measurement / test equipment.

Delay Control Port

The delay is controlled through a wide-band differential tuning port icntp/icntn. The delay control diagram is shown in Fig. 2.

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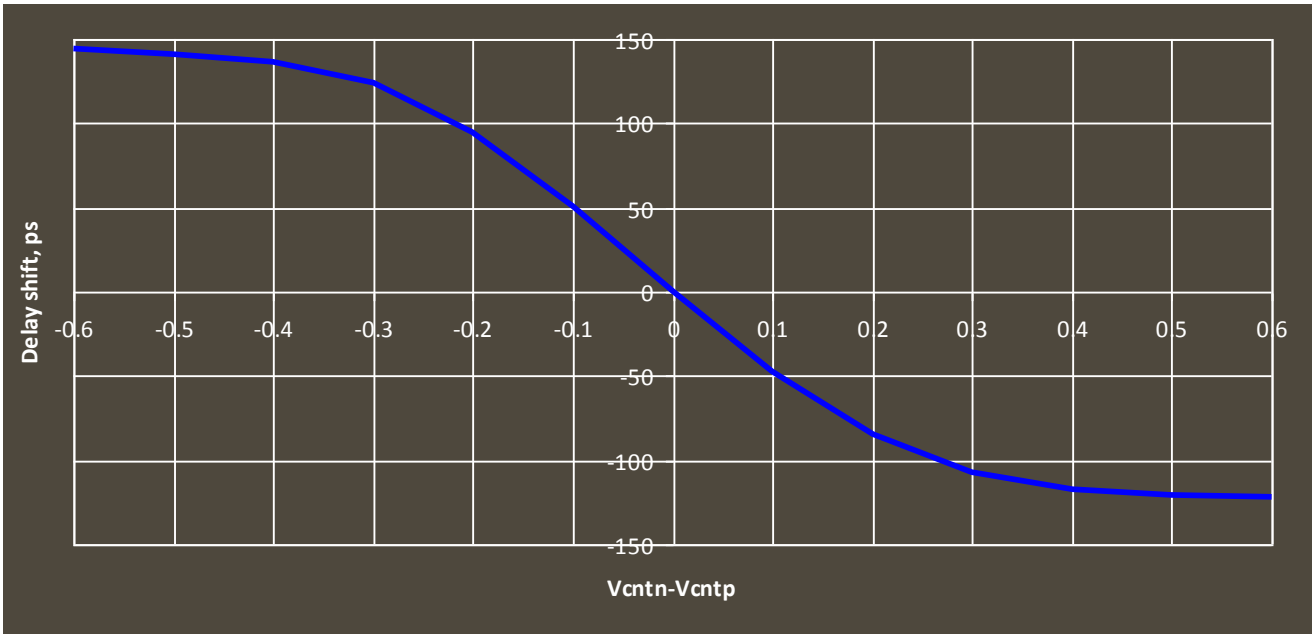

Fig. 2. Delay Control Diagram

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V*=ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V*=ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.3	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
ip	20	CML input	Differential high-speed signal inputs with internal SE 50*Ohm* termination to vcc
in	22		
icntp	2	CML input	Differential low-speed control inputs with internal SE 50*Ohm* termination to vcc
icntn	4		
outp	10	CML output	Differential high-speed signal outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
outn	8		

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	1, 3, 5, 7, 9, 11, 13, 14, 15, 16, 17, 19, 21,23
vee	Negative power supply (0*V* or -3.3*V*)	6, 12, 18, 24

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		355		*mA*	
Power consumption		1.17		*W*	
Junction temperature	-25	50	125	*°C*	
HS Input Data/Clock (ip/in)					
Data Rate	DC		32	*Gbps*	
Frequency	DC		17	*GHz*	For clock signals
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Data/Clock (outp/outn)					
Data Rate	DC		32	*Gbps*	
Frequency	DC		17	*GHz*	For clock signals
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.6		*V*	With external 50*Ohm* DC termination
Rise/Fall times	14		18	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	For clock signal
Output-to-Input Delay					
Adjustment range		265		*ps*	For the full range of icntp/icntn control signals
Absolute delay stability	-28		28	*ps*	0-125°C
Tuning port (icntp/icntn)					
Bandwidth	DC		1000	*MHz*	
SE voltage level	vcc-600		vcc	*mV*	Half control range when the opposite pin is at vcc
SE voltage level	vcc-1200		vcc	*mV*	Full control range when the opposite pin is at vcc-0.6*V*
Differential swing	0		1200	*mV*	Peak-peak, full control range
CM Level	vcc-(Diff. swing)/4			*V*	In differential mode

PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 3. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain, which is ground for the positive supply or power for the negative supply. It will help dissipate heat generated by the chip during operation.

The part's identification label is ASNT5001A-PQC. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

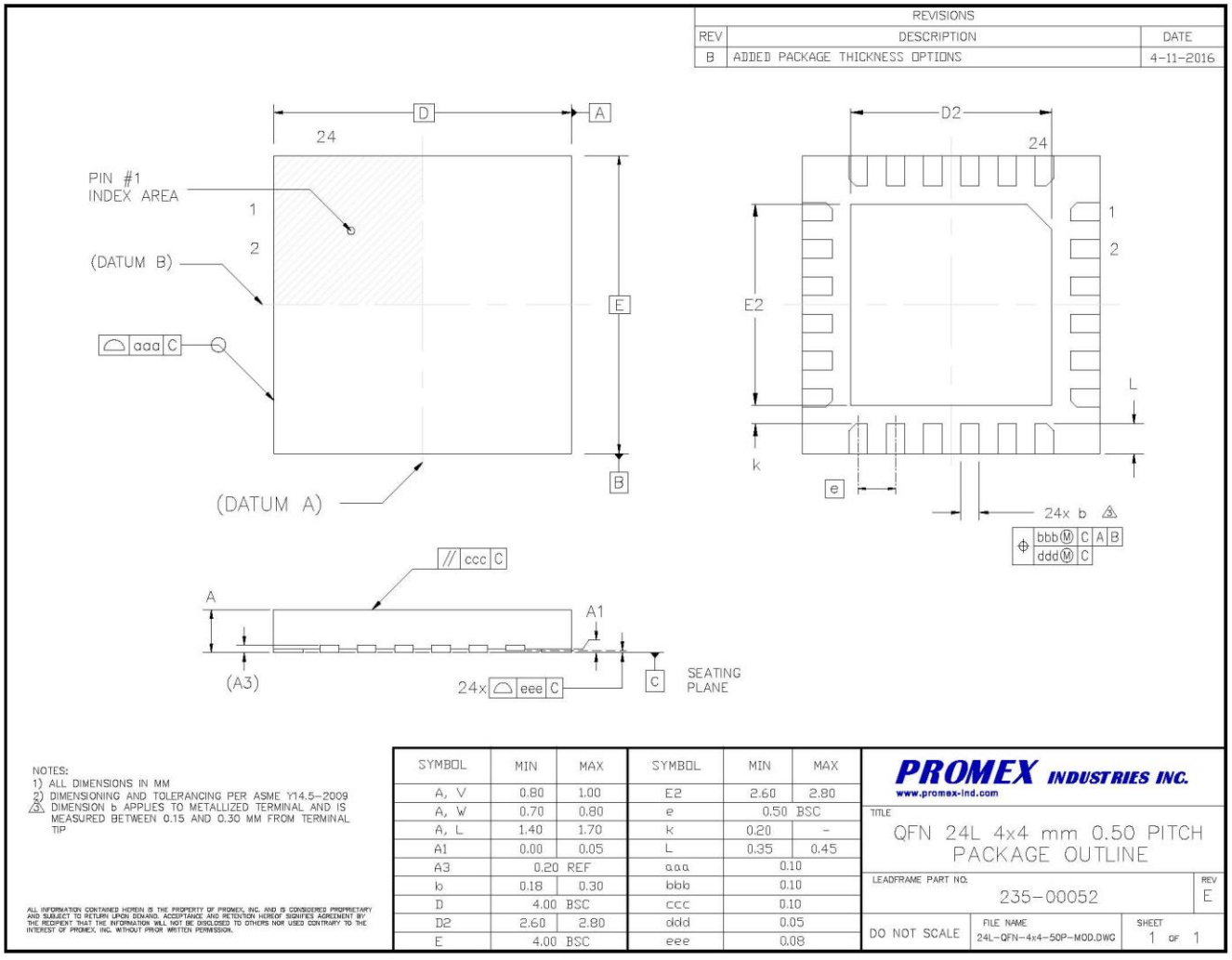

Fig. 3. QFN 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.1.2	01-2020	Updated Package Information
1.0.2	07-2019	Updated Letterhead
1.0.1	03-2017	Initial release