µPA672CT

N-CHANNEL MOSFET FOR SWITCHING

R07DS1289EJ0200
Rev.2.00
Jul 24, 2015

Description

The UPA672CT, N-channel vertical type MOSFET designed for general-purpose switch, is a device which can be driven directly by a 4.5 V power source.

Features

- Two MOSFET circuits
- Directly driven by a 4.5 V power source.
- Low on-state resistance
  $R_{DS(on)1}$ = 2.7 Ω MAX. (V_{GS} = 10 V, I_D = 100 mA)
  $R_{DS(on)2}$ = 3.2 Ω MAX. (V_{GS} = 4.5 V, I_D = 50 mA)

Ordering Information

Part Number	Lead Plating	Packing	Package
UPA672CT-T1-A/AT	-A:Sn-Bi , -AT:Pure Sn	3000p/Reel	SC-88 (6pSSP)

Remark "-AT" indicates Pb-free. This product does not contain Pb in external electrode and other parts.

Marking UA

Absolute Maximum Ratings (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±100	mA
Drain Current (pulse) **Note**	$I_{D(pulse)}$	±200	mA
Total Power Dissipation	P_T	200 (Total)	mW
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

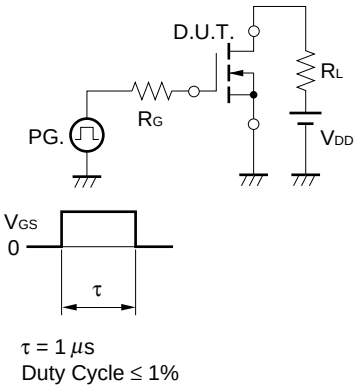
Note PW ≤ 10 µs, Duty Cycle ≤ 1%

Electrical Characteristics (T_A = 25°C)

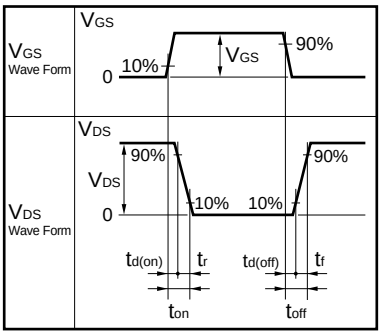
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0		2.5	V
Forward Transfer Admittance **Note**	$\lvert y_{fs} \rvert$	V_{DS} = 10 V, I_D = 100 mA	150			mS
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 100 mA		2.1	2.7	Ω
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 50 mA		2.4	3.2	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V,		20		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		9		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		2		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 10 V,		16		ns
Rise Time	t_r	I_D = 200 mA,		6.5		ns
Turn-off Delay Time	$t_{d(off)}$	V_{GS} = 10 V,		82		ns
Fall Time	t_f	R_G = 10 Ω		32		ns
Total Gate Charge	Q_G	I_D = 200 mA, V_{DD} = 25 V, V_{GS} = 10 V		2		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = 200 mA, V_{GS} = 0 V		0.86		V

Note Pulsed

Test Circuit Switching Time

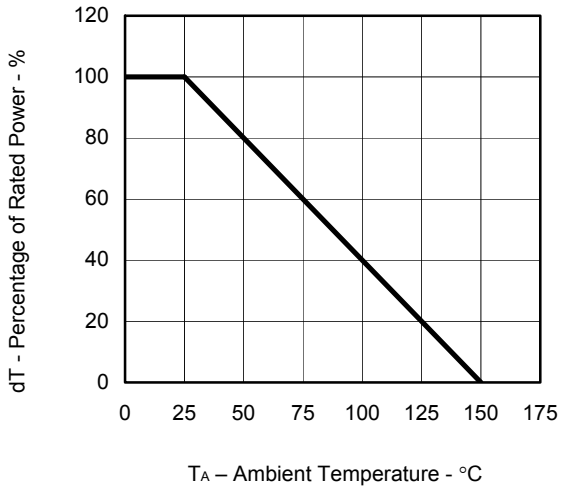


τ = 1 µs
Duty Cycle ≤ 1%

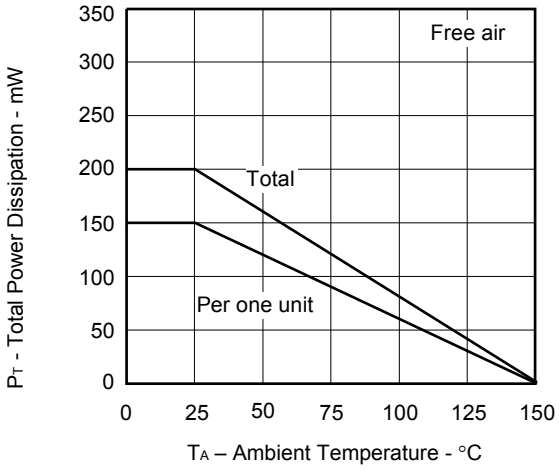


Typical Characteristics (T_A = 25°C)

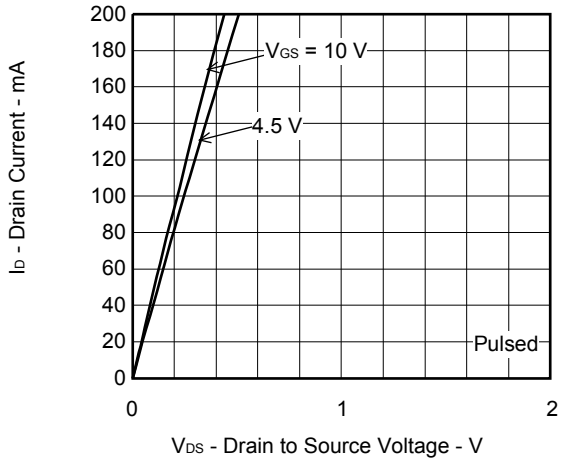
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



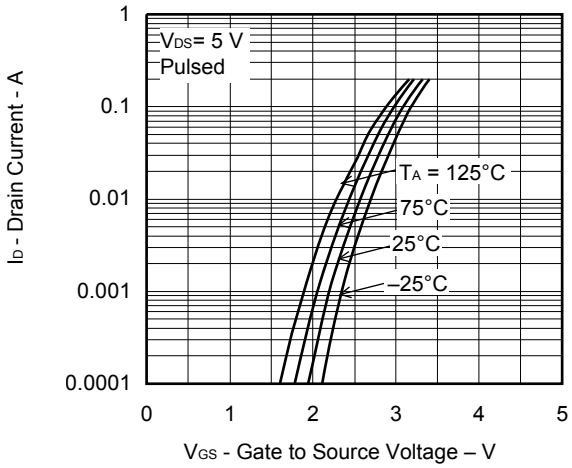
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



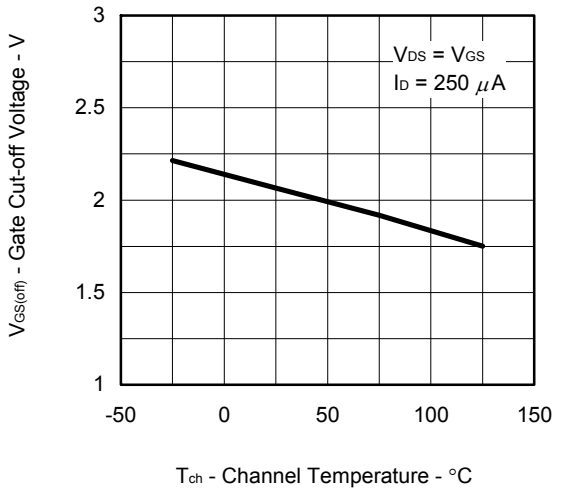
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



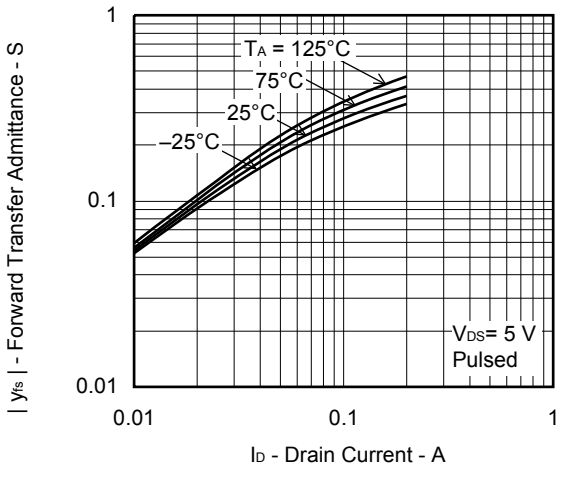
FORWARD TRANSFER CHARACTERISTICS



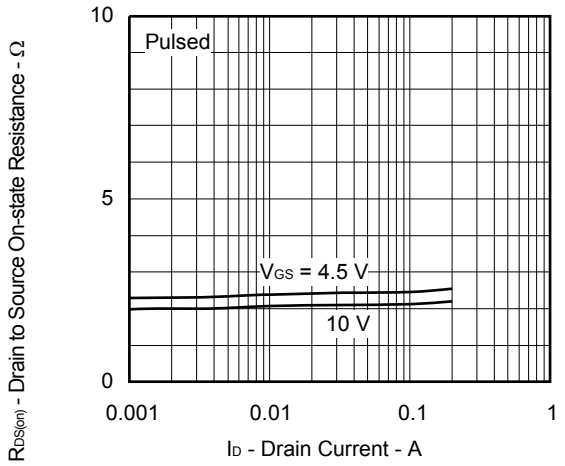
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



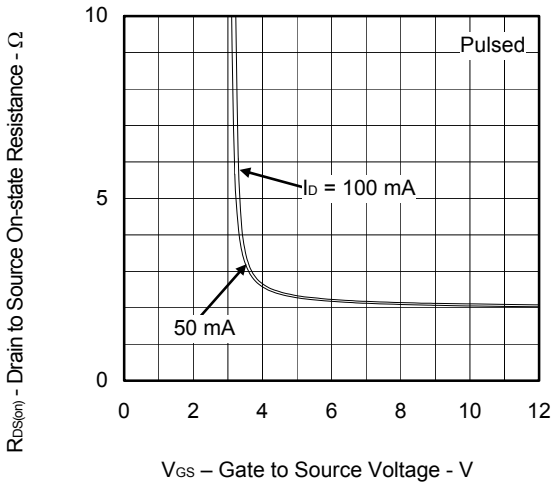
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



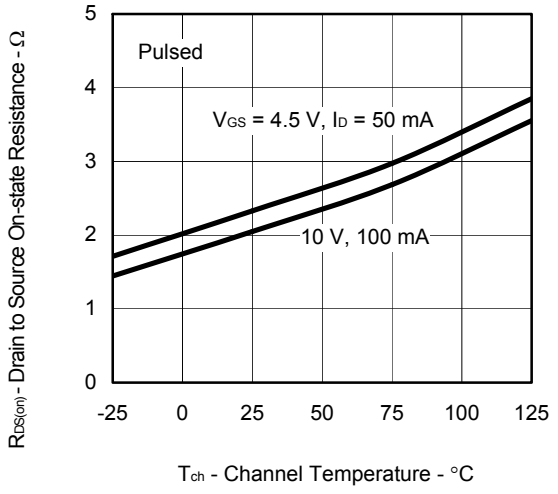
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



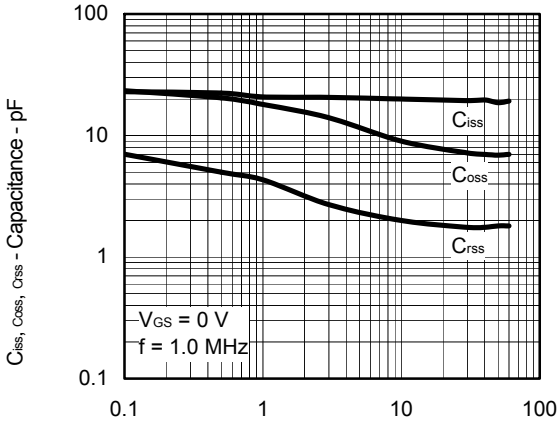
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



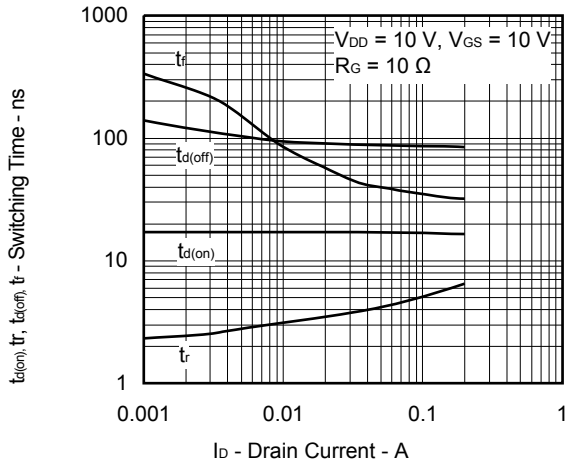
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



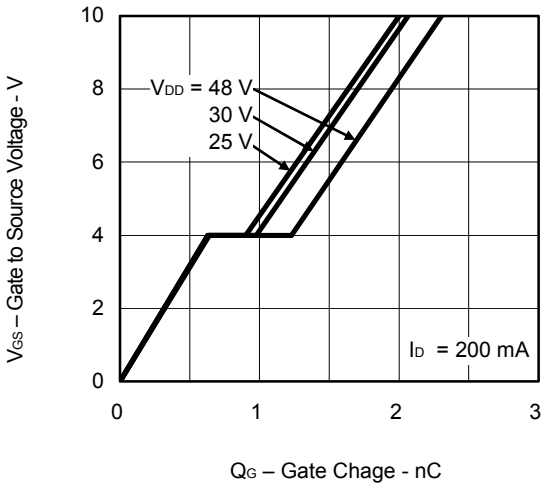
CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



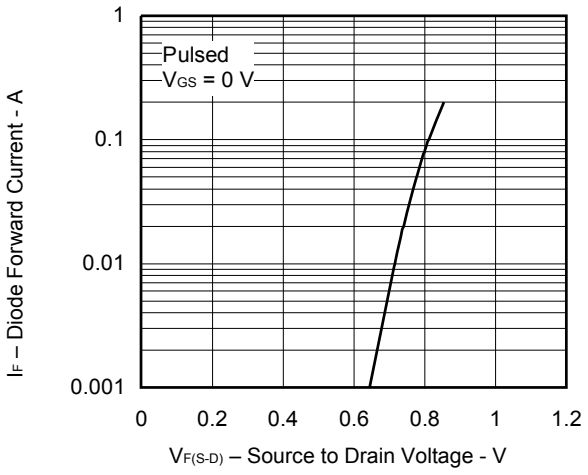
SWITCHING CHARACTERISTICS



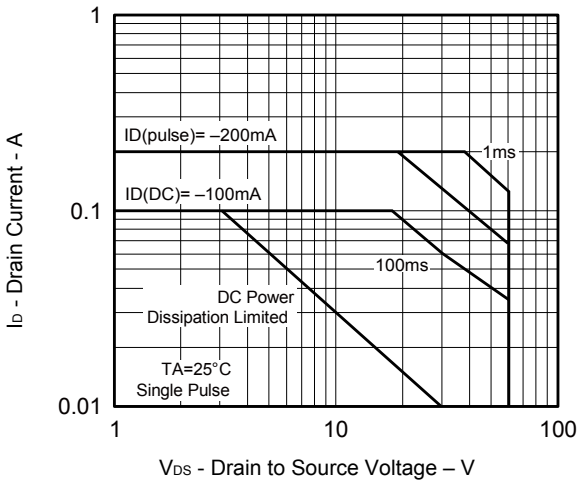
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

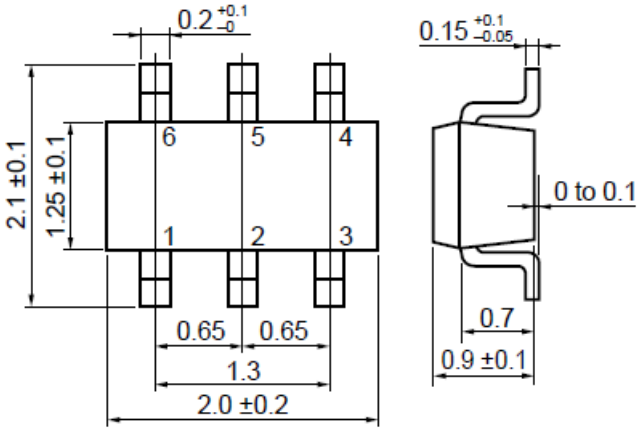


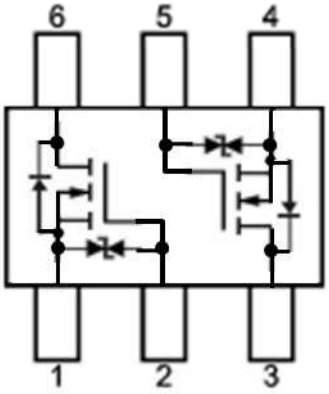
FORWARD BIAS SAFE OPERATING AREA



Package Drawings (Unit: mm)

SC-88 (6pSSP)

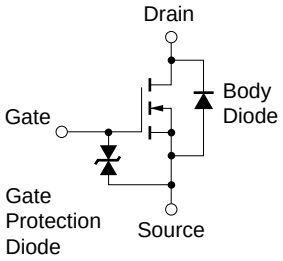




PIN CONNECTION

1. Source 1
2. Gate 1
3. Drain 2
4. Source 2
5. Gate 2
6. Drain 1

Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Rev.	Date	Description	
		Page	Summary
1.00	Sep , 2013	–	First Edition Issued
2.00	Jul, 2015	2	- Changed Electrical Characteristics - Changed Test Circuit Switching Time
		3, 4, 5	Changed all graphs

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