

## 74F573 Octal D-Type Latch with 3-STATE Outputs

### General Description

The 74F573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs.

This device is functionally identical to the 74F373 but has different pinouts.

### Features

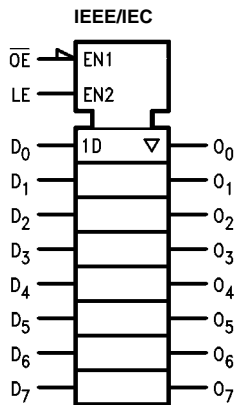
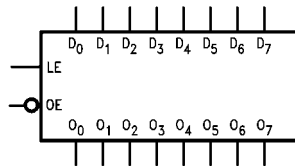
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74F373
- 3-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

### Ordering Code:

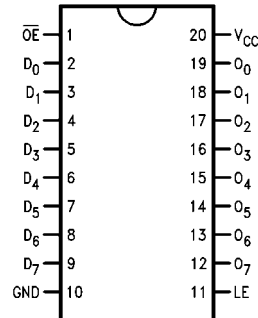
| Order Number | Package Number | Package Description   |
|--------------|----------------|---|
| 74F573SC     | M20B           | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74F573SJ     | M20D           | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide             |
| 74F573PC     | N20A           | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide     |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

| Pin Names                      | Description                              | U.L.<br>HIGH/LOW | Input $I_{IH}/I_{IL}$<br>Output $I_{OH}/I_{OL}$ |
|--------------------------------|--|------------------|---|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                              | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| LE                             | Latch Enable Input (Active HIGH)         | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| $\overline{OE}$                | 3-STATE Output Enable Input (Active LOW) | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| O <sub>0</sub> -O <sub>7</sub> | 3-STATE Latch Outputs                    | 150/40(33.3)     | -3 mA/24 mA (20 mA)                             |

## Functional Description

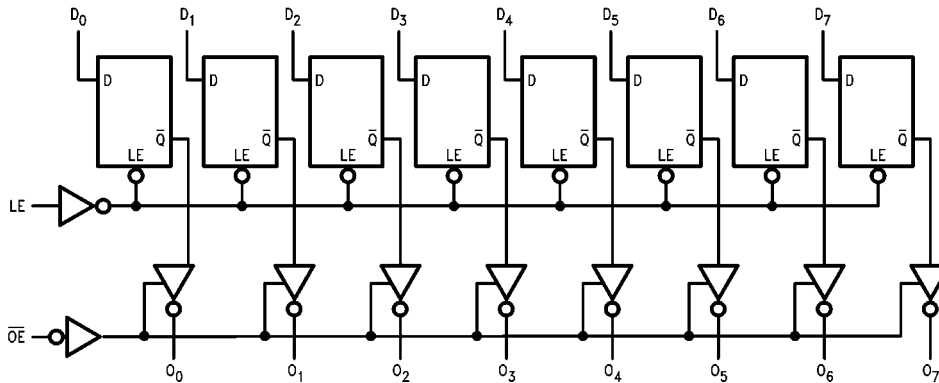
The 74F573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D<sub>n</sub> inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

## Function Table

| Inputs          |    |   | Outputs        |
|-----------------|----|---|----------------|
| $\overline{OE}$ | LE | D | O              |
| L               | H  | H | H              |
| L               | H  | L | L              |
| L               | L  | X | O <sub>0</sub> |
| H               | X  | X | Z              |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
O<sub>0</sub> = Value stored from previous clock cycle

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature  | -65°C to +150°C                      |
| Ambient Temperature under Bias   | -55°C to +125°C                      |
| Junction Temperature under Bias  | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                            | -0.5V to +7.0V                       |
| Input Voltage (Note 2)   | -0.5V to +7.0V                       |
| Input Current (Note 2)   | -30 mA to +5.0 mA                    |
| Voltage Applied to Output<br>in HIGH State (with V <sub>CC</sub> = 0V) |                                      |
| Standard Output  | -0.5V to V <sub>CC</sub>             |
| 3-STATE Output   | -0.5V to +5.5V                       |
| Current Applied to Output<br>in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |
| ESD Last Passing Voltage (Min)   | 4000V                                |

**Recommended Operating Conditions**

|                              |                |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C   |
| Supply Voltage               | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol           | Parameter                         | Min  | Typ                      | Max         | Units | V <sub>CC</sub> | Conditions   |
|------------------|-----------------------------------|--|--------------------------|-------------|-------|-----------------|--|
| V <sub>IH</sub>  | Input HIGH Voltage                | 2.0  |                          |             | V     |                 | Recognized as a HIGH Signal  |
| V <sub>IL</sub>  | Input LOW Voltage                 |  |                          | 0.8         | V     |                 | Recognized as a LOW Signal   |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |  |                          | -1.2        | V     | Min             | I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub>  | Output HIGH Voltage               | 10% V <sub>CC</sub><br>10% V <sub>CC</sub><br>5% V <sub>CC</sub><br>5% V <sub>CC</sub> | 2.5<br>2.4<br>2.7<br>2.7 |             | V     | Min             | I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA<br>I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA |
| V <sub>OL</sub>  | Output LOW Voltage                | 10% V <sub>CC</sub>  |                          | 0.5         | V     | Min             | I <sub>OL</sub> = 24 mA  |
| I <sub>IH</sub>  | Input HIGH Current                |  |                          | 20.0<br>5.0 | μA    | Max             | V <sub>IN</sub> = 2.7V   |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test |  |                          | 7.0         | μA    | Max             | V <sub>IN</sub> = 7.0V   |
| I <sub>CEX</sub> | Output HIGH Leakage Current       |  |                          | 50          | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>   |
| V <sub>ID</sub>  | Input Leakage Test                | 4.75   |                          |             | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded  |
| I <sub>OD</sub>  | Output Leakage Circuit Current    |  |                          | 3.75        | μA    | 0.0             | V <sub>ID</sub> = 150 mV<br>All Other Pins Grounded  |
| I <sub>IL</sub>  | Input LOW Current                 |  |                          | -0.6        | mA    | Max             | V <sub>IN</sub> = 0.5V   |
| I <sub>OZH</sub> | Output Leakage Current            |  |                          | 50          | μA    | Max             | V <sub>OUT</sub> = 2.7V  |
| I <sub>OZL</sub> | Output Leakage Current            |  |                          | -50         | μA    | Max             | V <sub>OUT</sub> = 0.5V  |
| I <sub>OS</sub>  | Output Short-Circuit Current      | -60  |                          | -150        | mA    | Max             | V <sub>OUT</sub> = 0V  |
| I <sub>ZZ</sub>  | Bus Drainage Test                 |  |                          | 500         | μA    | 0.0V            | V <sub>OUT</sub> = 5.25V   |
| I <sub>CCL</sub> | Power Supply Current              |  | 35                       | 55          | mA    | Max             | V <sub>O</sub> = LOW   |
| I <sub>CCZ</sub> | Power Supply Current              |  | 35                       | 55          | mA    | Max             | V <sub>O</sub> = HIGH Z  |

### AC Electrical Characteristics

| Symbol           | Parameter                        | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |     |      | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |      | Units |
|------------------|----------------------------------|---|-----|------|---|------|--|------|-------|
|                  |                                  | Min   | Typ | Max  | Min   | Max  | Min  | Max  |       |
| t <sub>PLH</sub> | Propagation Delay                | 3.0   | 5.3 | 7.0  | 3.0   | 9.0  | 3.0  | 8.0  | ns    |
| t <sub>PHL</sub> | D <sub>n</sub> to O <sub>n</sub> | 2.0   | 3.7 | 6.0  | 2.0   | 7.0  | 2.0  | 6.5  |       |
| t <sub>PLH</sub> | Propagation Delay                | 5.0   | 9.0 | 11.0 | 5.0   | 13.5 | 5.0  | 12.0 | ns    |
| t <sub>PHL</sub> | LE to O <sub>n</sub>             | 3.0   | 5.2 | 7.0  | 3.0   | 7.5  | 3.0  | 7.0  |       |
| t <sub>PZH</sub> | Output Enable Time               | 2.0   | 5.0 | 8.0  | 2.0   | 10.0 | 2.0  | 9.0  | ns    |
| t <sub>PZL</sub> |                                  | 2.0   | 5.6 | 8.5  | 2.0   | 10.0 | 2.0  | 9.5  |       |
| t <sub>PHZ</sub> | Output Disable Time              | 1.5   | 4.5 | 5.5  | 1.5   | 7.0  | 1.5  | 6.5  | ns    |
| t <sub>PLZ</sub> |                                  | 1.5   | 3.8 | 5.5  | 1.5   | 5.5  | 1.5  | 5.5  |       |

### AC Operating Requirements

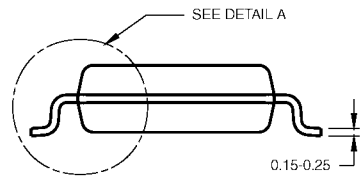
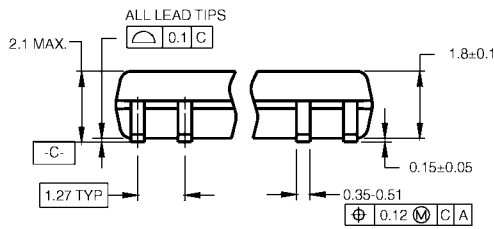
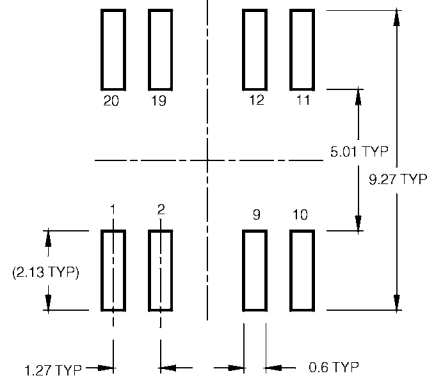
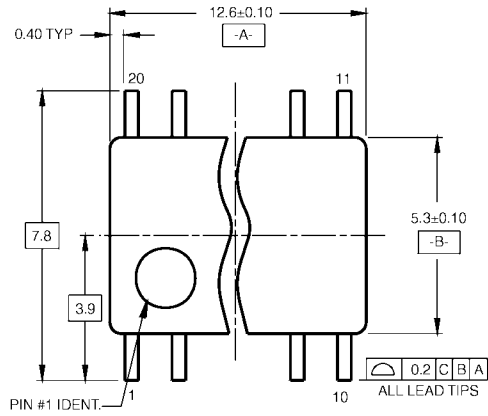
| Symbol             | Parameter               | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V |     | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = +5.0V |     | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V |     | Units |
|--------------------|-------------------------|---|-----|---|-----|--|-----|-------|
|                    |                         | Min   | Max | Min   | Max | Min  | Max |       |
| t <sub>S</sub> (H) | Setup Time, HIGH or LOW | 2.0   |     | 2.0   |     | 2.0  |     | ns    |
| t <sub>S</sub> (L) | D <sub>n</sub> to LE    | 2.0   |     | 2.0   |     | 2.0  |     |       |
| t <sub>H</sub> (H) | Hold Time, HIGH or LOW  | 3.0   |     | 3.0   |     | 3.0  |     | ns    |
| t <sub>H</sub> (L) | D <sub>n</sub> to LE    | 3.5   |     | 4.0   |     | 3.5  |     |       |
| t <sub>W</sub> (H) | LE Pulse Width, HIGH    | 4.0   |     | 4.0   |     | 4.0  |     | ns    |

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M20B**

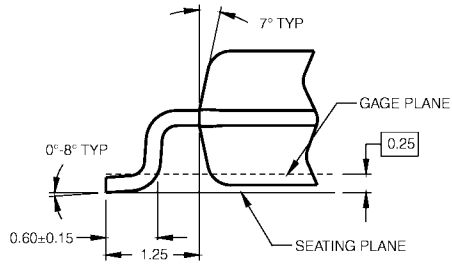
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:  
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 B. DIMENSIONS ARE IN MILLIMETERS.  
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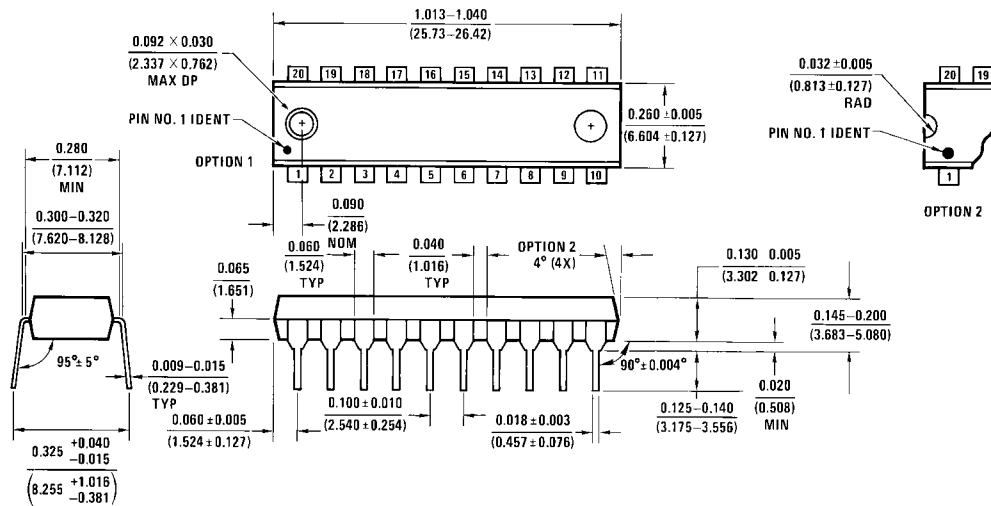
M20DRevB1



DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N20A**

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