

N-channel 30 V 2.95 m Ω logic level MOSFET in LFPAK33 using NextPower Technology

Rev. 2 — 15 June 2012

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching

Synchronous buck regulator

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25 ^{\circ}C$	-	-	30	V
I _D	drain current	$T_{mb} = 25 \text{ °C}; V_{GS} = 10 \text{ V}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	<u>[1]</u> -	-	70	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	91	W
T _j	junction temperature		-55	-	175	°C
Static charact	teristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 10	-	3.3	3.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	-	2.45	2.95	mΩ
Dynamic char	racteristics					
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 15 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	4.4	-	nC
$Q_{G(tot)}$	total gate charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 15 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	16.7	-	nC

^[1] Continuous current is limited by package.



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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		D
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	1 2 3 4	mbb076 S
			SOT1210 (LFPAK33)	

3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN2R9-30MLC	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 4 leads	SOT1210		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25 ^{\circ}C$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; see <u>Figure 1</u>	[1] -	70	Α
		V _{GS} = 10 V; T _{mb} = 100 °C; see <u>Figure 1</u>	[1] -	70	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 4	-	523	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	91	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	340	-	V
Source-drain	diode				
Is	source current	T _{mb} = 25 °C	-	70	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	523	Α
Avalanche rug	gedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 70 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω ; unclamped; see Figure 3	-	75	mJ

^[1] Continuous current is limited by package.

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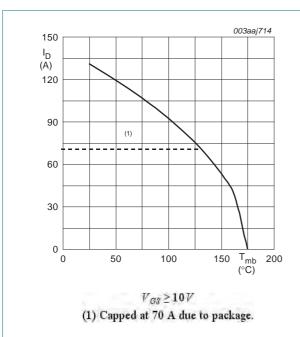


Fig 1. Continuous drain current as a function of mounting base temperature

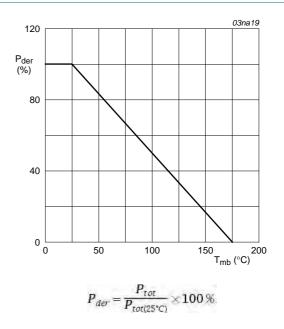


Fig 2. Normalized total power dissipation as a function of mounting base temperature

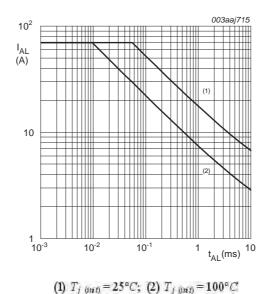
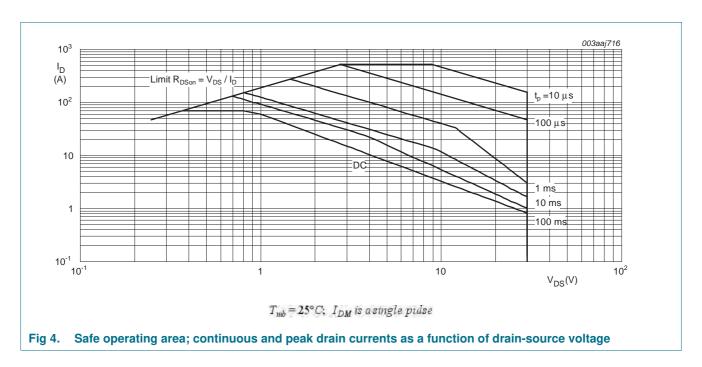


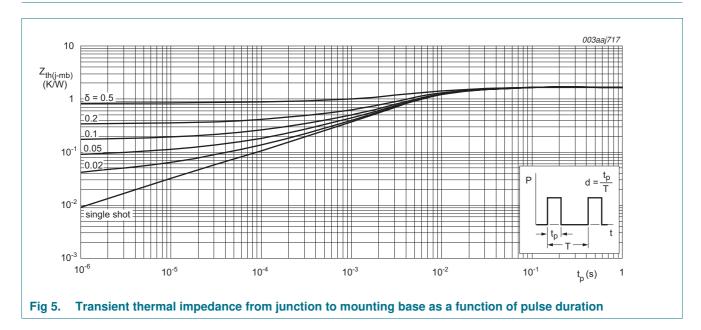
Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see <u>Figure 5</u>	-	1.44	1.65	K/W



6. Characteristics

Table 6 Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
$V_{\text{GS(th)}}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1.45	1.78	2.15	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature		-	-4.3	-	mV/K
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 10	-	3.3	3.8	mΩ
		$V_{GS} = 4.5 \text{ V}$; $I_D = 25 \text{ A}$; see Figure 11; see Figure 10	-	-	6.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 10	-	2.45	2.95	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ °C};$ see <u>Figure 10</u> ; see <u>Figure 11</u>	-	-	5.05	mΩ
R_G	gate resistance	f = 1 MHz	1.23	2.46	4.92	Ω
Dynamic o	haracteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	36.1	-	nC
		I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	16.7	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	34.8	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 4.5 \text{ V}$;	-	6.1	-	nC
$Q_{GS(th)} \\$	pre-threshold gate-source charge	see <u>Figure 12</u> ; see <u>Figure 13</u>	-	3.9	-	nC
$Q_{GS(th\text{-}pl)}$	post-threshold gate-source charge		-	2.2	-	nC
Q _{GD}	gate-drain charge		-	4.4	-	nC
$V_{GS(pl)} \\$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 15 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	2.7	-	V
C _{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	2419	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 14</u>	-	500	-	pF
C _{rss}	reverse transfer capacitance		-	180	-	pF

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; \ R_L = 0.6 \ \Omega; \ V_{GS} = 4.5 \text{ V}; \\ R_{G(ext)} = 4.7 \ \Omega$	-	17.7	-	ns
t _r	rise time		-	30.8	-	ns
$t_{d(off)}$	turn-off delay time		-	24.6	-	ns
t _f	fall time		-	19.3	-	ns
Q _{oss}	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 ^{\circ}\text{C}$	-	15.1	-	nC
Source-drai	in diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see Figure 15	-	0.82	1.1	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	21.8	-	ns
Q _r	recovered charge	V _{DS} = 15 V	-	15.6	-	nC
ta	reverse recovery rise time	$V_{GS} = 0 \text{ V; } I_S = 25 \text{ A; } dI_S/dt = -100 \text{ A/}\mu\text{s;}$ $V_{DS} = 15 \text{ V; see } \frac{\text{Figure 16}}{\text{Im}}$	-	12.9	-	ns
t _b	reverse recovery fall time		-	8.9	-	ns

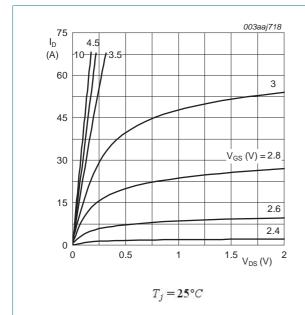


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

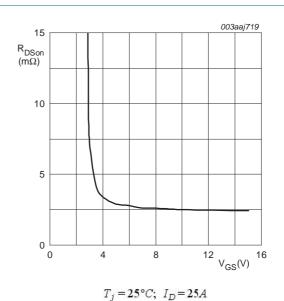


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

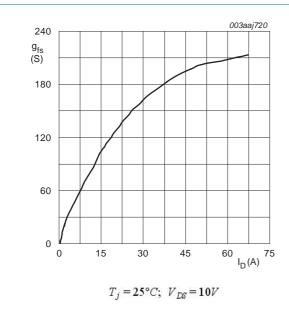


Fig 8. Forward transconductance as a function of drain current; typical values

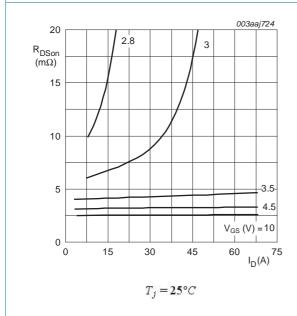


Fig 10. Drain-source on-state resistance as a function of drain current; typical values

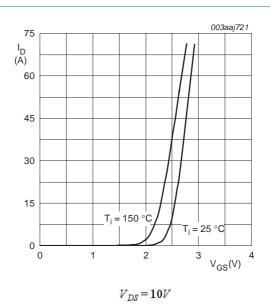


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

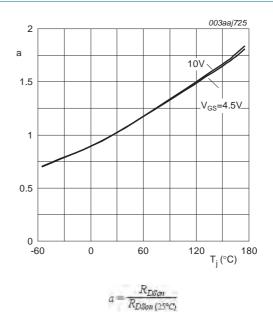


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature

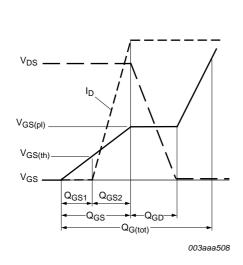


Fig 12. Gate charge waveform definitions

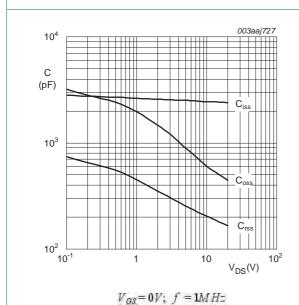
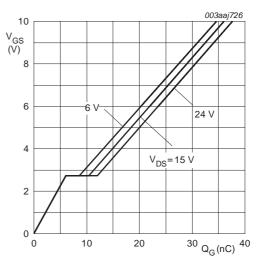


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $T_j = 25^{\circ}C; I_D = 25A$

Fig 13. Gate-source voltage as a function of gate charge; typical values

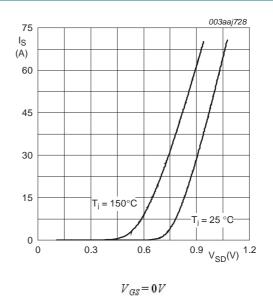
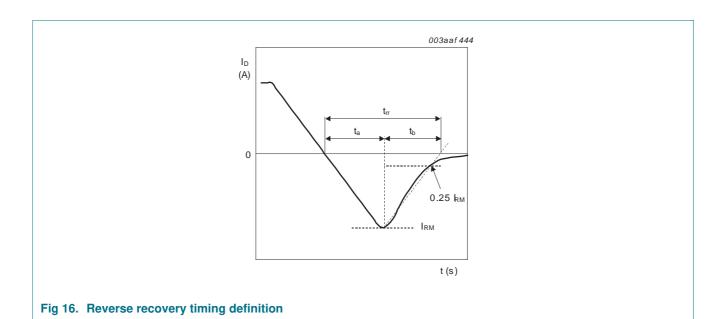


Fig 15. Source current as a function of source-drain voltage; typical values



7. Package outline

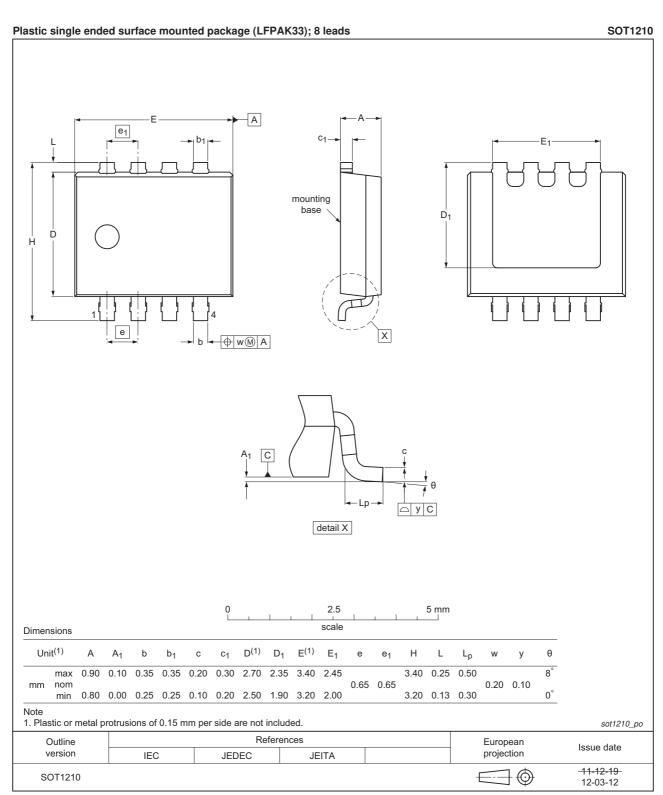


Fig 17. Package outline SOT1210 (LFPAK33)

PSMN2R9-30MLC

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R9-30MLC v.2	20120615	Product data sheet	-	PSMN2R9-30MLC v.1

N-channel 30 V 2.95 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

9. Legal information

9.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design
- [2] The term 'short data sheet' is explained in section "Definitions"
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