SY89832U

2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination

Precision Edge®

General Description

The SY89832U is a 2.5V, high-speed, 2GHz differential, low voltage differential swing (LVDS) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF–AC reference output is included for AC-coupled applications.

The SY89832U is a part of Micrel's high-speed clock synchronization family. For 3.3V applications, see SY89833L or SY89833AL. For applications that require a different I/O combination, consult Micrel's website at www.micrel.com and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

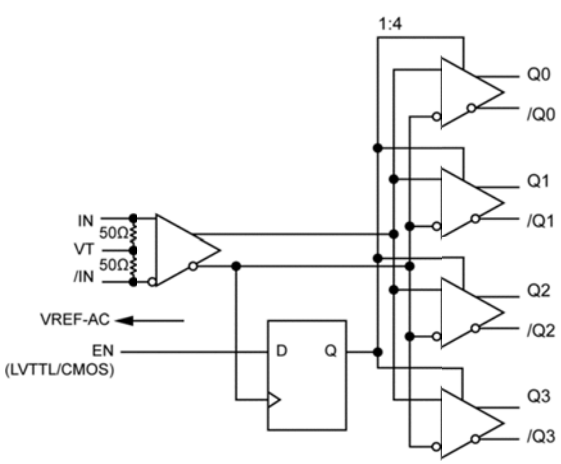
Features

- Guaranteed AC performance over temperature and voltage:
  - DC-to >2.0GHz throughput
  - <570ps propagation delay (IN-to-Q)
  - <20ps within-device skew
  - <200ps rise/fall time
- Ultra-low jitter design:
  - 81fs$_{RMS}$ phase jitter
- Unique, patented input termination and VT pin accepts DC- and AC-coupled inputs
- High-speed LVDS outputs
- 2.5V voltage supply operation
- Industrial temperature range: –40°C to +85°C
- Available in a 16-pin (3mm × 3mm) QFN package

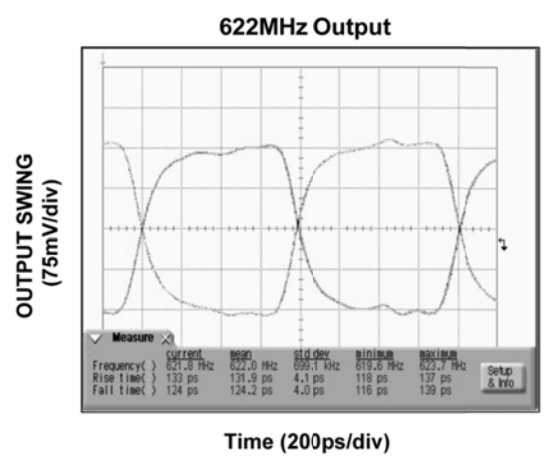
Applications

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

Functional Block Diagram



Typical Performance



Precision Edge is a registered trademark of Micrel, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • http://www.micrel.com

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89832UMG	QFN-16	Industrial	832U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89832UMG TR[2]	QFN-16	Industrial	832U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC Electricals only.
2. Tape and Reel.

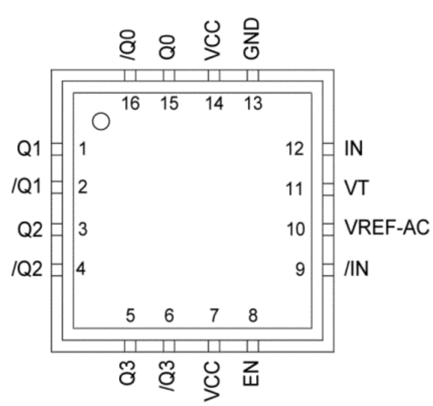
Truth Table

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0[3]	1[3]

Note:

3. On next negative transition of the input signal (IN).

Pin Configuration



16-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential (Outputs): Normally terminated with 100Ω across the pair (Q, /Q). See LVDS Outputs section for more details.Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	The single-ended, TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signs as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an intermediate state if left open. See Input Interface Applications section for more details.
10	VREF-AC	Reference Voltage: These outputs bias to VCC–1.4V. They are used when AC coupling the inputs (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.01μF low ESR capacitor to VCC. See Input Interface Applications section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See Input Interface Applications section for more details.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors and place as close to each VCC pin as possible.

Absolute Maximum Ratings[4]

Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}). ....–0.5V to V_{CC} +0.3V
LVDS Output Current (I_{OUT}).....................................±10mA
Input Current
    Source or Sink Current on (IN, /IN) ....±50mA
VREF-AC Current
    Source or Sink Current on (I_{VT})............................±2mA
Lead Temperature (soldering, 20s)........................... 260°C
Storage Temperature (T_S)........................–65°C to +150°C

Operating Ratings[5]

Supply Voltage Range (V_{IN}) .... +2.375V to +2.675V
Ambient Temperature (T_A) ....–40°C to +85°C
Package Thermal Resistance[6]
    QFN
    (θ_{JA}) Still-Air ....60°C/W
    (Ψ_{JB})..32°C/W

DC Electrical Characteristics[7]

T_A = -40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, maximum V_{CC}.		75	100	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)		0.1		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage (IN, /IN)		–0.3		V_{IH}-0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 4.	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN – /IN|	See Figure 5.	0.2			V
$\|I_{IN}\|$	Input Current (IN, /IN)	Note 8			45	mA
V_{REF-AC}	Output Reference Voltage		V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V

Notes:

4. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
5. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
6. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
8. Due to the internal termination the input current depends on the applied voltages at IN, /IN and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

LVDS Outputs DC Electrical Characteristics[7]

V_{CC} = 2.5V ±5%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OUT}	Output Voltage Swing	See Figure 4.	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 5.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		–50		50	mV

LVTTL/CMOS DC Electrical Characteristics[7]

V_{CC} = 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

AC Electrical Characteristics[9]

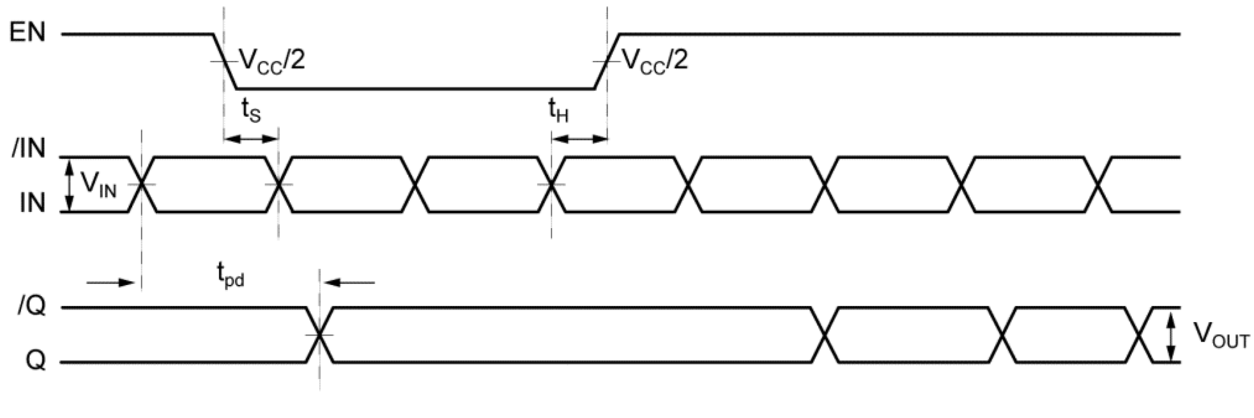
V_{CC} = 2.5V ±5% or 3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C unless otherwise stated.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Frequency		$V_{OUT} \geq 200mV$	2.0	2.5		GHz
t_{pd}	Propagation Delay	IN-to-Q	$V_{IN} < 400mV$	370	470	570	ps
			$V_{IN} \geq 400mV$	300	410	500	ps
t_{SKEW}	Within-Device Skew		Note 10		5	20	ps
	Part-to-Part Skew		Note 11			200	ps
t_S	Set-Up Time	EN to IN, /IN	Note 12	300			ps
t_H	Hold Time	EN to IN, /IN	Note 12	500			ps
t_{JITTER}	Additive Phase Jitter		Carrier = 622MHz Integration Range: 12kHz – 20MHz		81		fs
			Carrier = 250MHz Integration Range: 12kHz – 20MHz		195		fs
t_r, t_f	Output Rise/Fall Times (20% to 80%)		At full output swing.	70	150	200	ps

Notes:

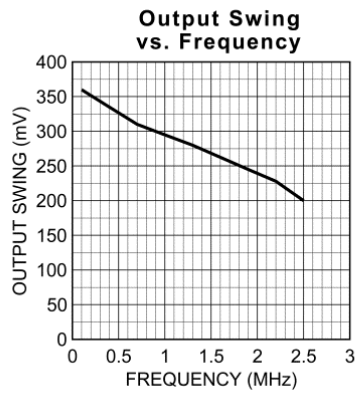
9. High-frequency AC parameters are guaranteed by design and characterization.
10. Within device skew is measured between two different outputs under identical input transitions.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
12. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

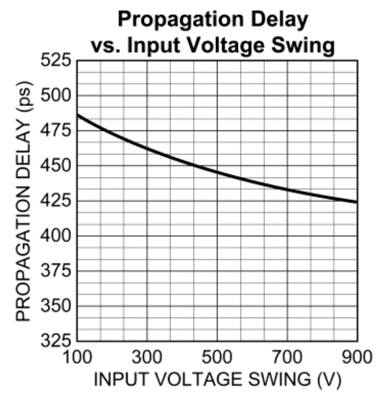
Timing Diagram



Typical Operating Characteristics

V_{CC} = 2.5V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs; T_A = 25°C, unless otherwise stated.

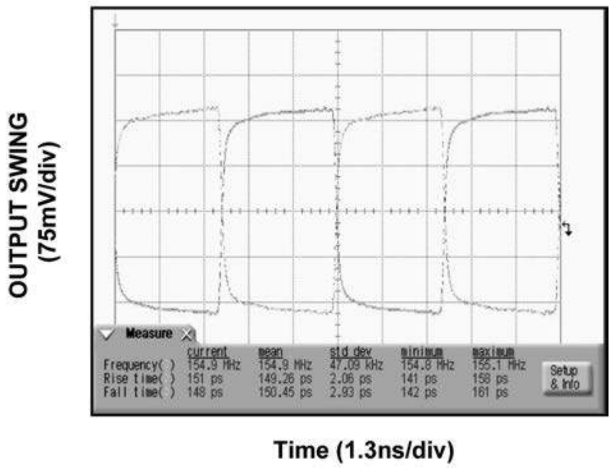




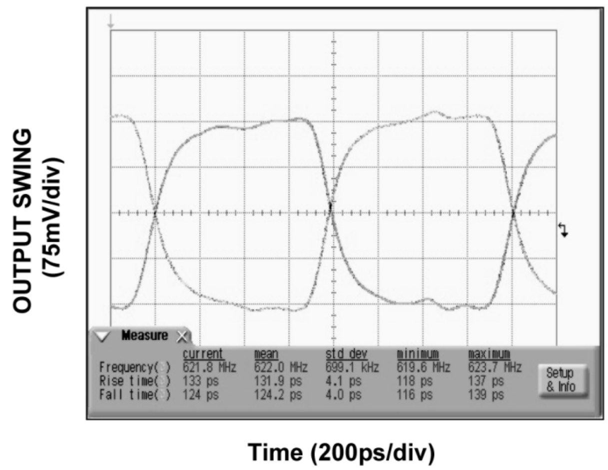
Functional Characteristics

V_{CC} = 2.5V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs; T_A = 25°C, unless otherwise stated.

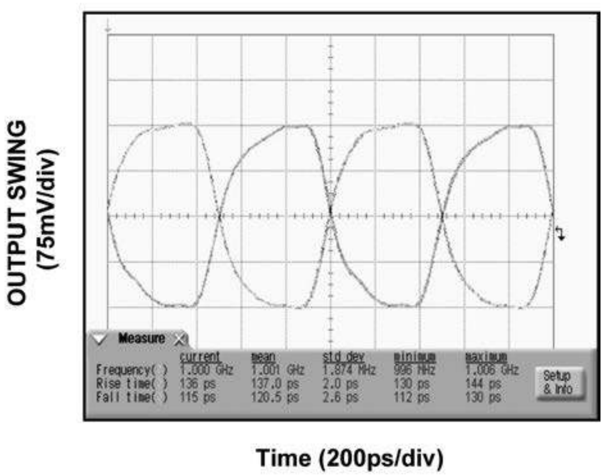
155MHz Output



622MHz Output

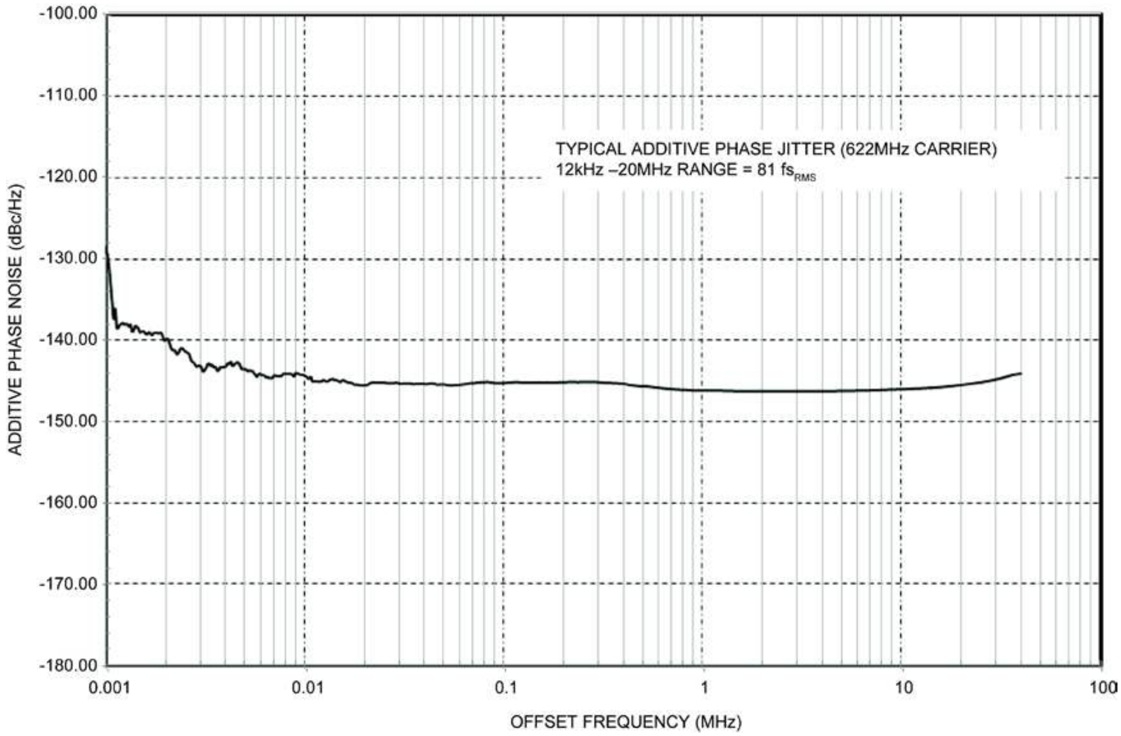


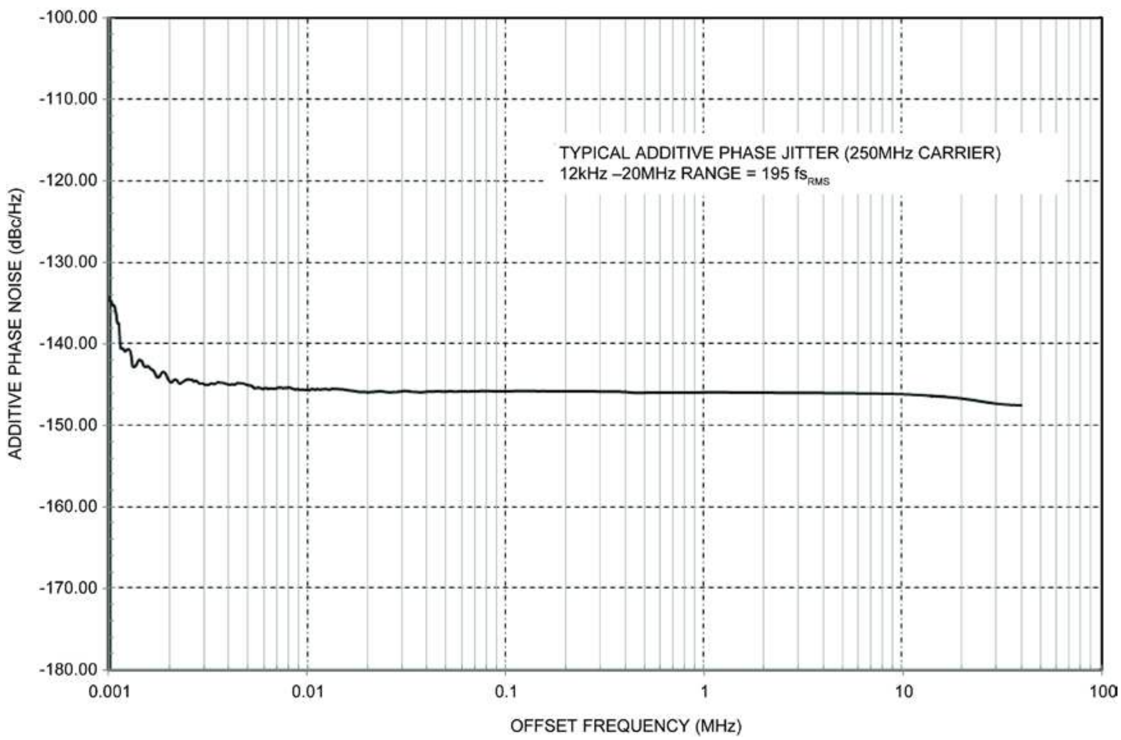
1GHz Output



Additive Phase Noise Plots

V_{CC} = +3.3V, GND = 0, T_A = 25°C





Input Stage

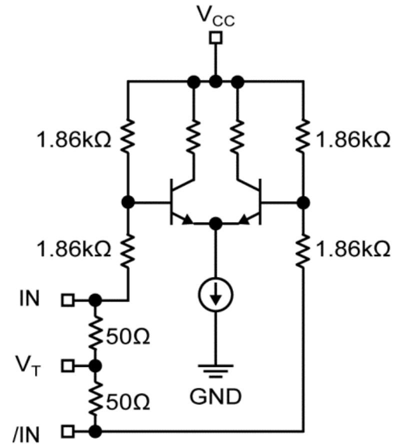


Figure 1. Simplified Differential Input Buffer

LVDS Outputs

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common-mode above ground.

The common-mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receiver.

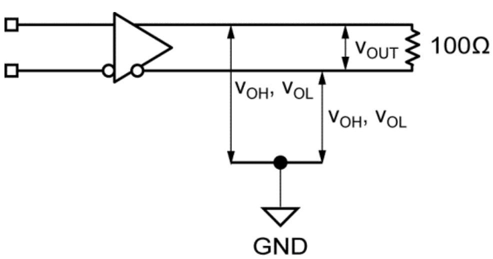


Figure 2. LVDS Differential Measurement

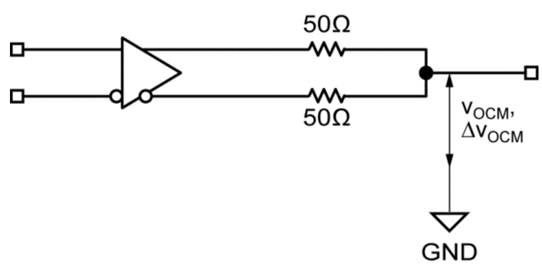


Figure 3. LVDS Common Mode Measurement

Single-Ended and Differential Swings

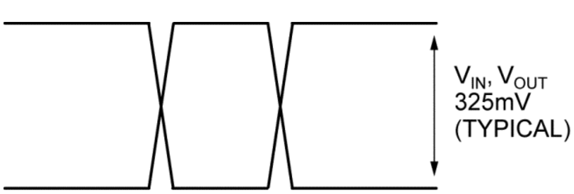


Figure 4. Single-Ended Swing

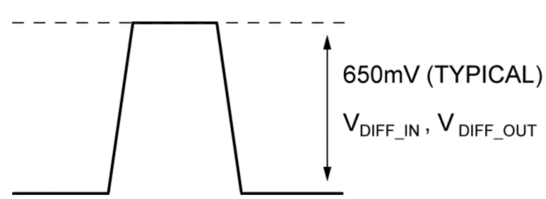


Figure 5. Differential Swing

tcghelp@micrel.com or (408) 955-1690

Input Interface Applications

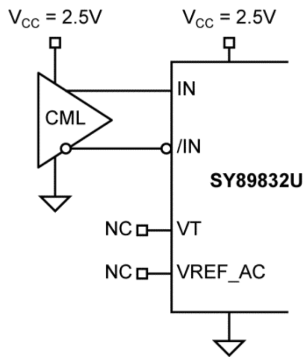


Figure 6. DC-Coupled CML Input Interface

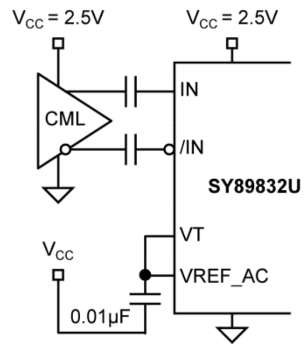


Figure 7. AC-Coupled CML Input Interface

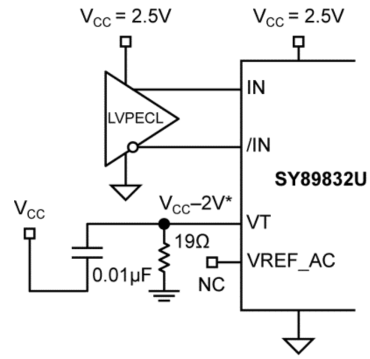


Figure 8. DC-Coupled LVPECL Input Interface

(*Bypass with 0.01µF to GND)

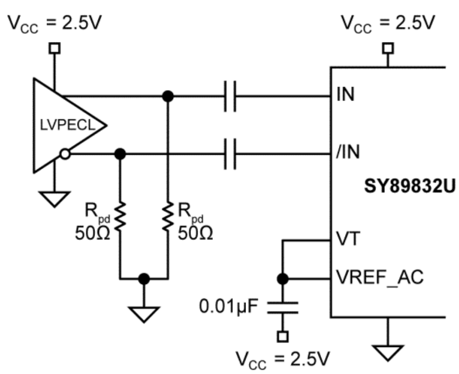


Figure 9. AC-Coupled LVPECL Input Interface

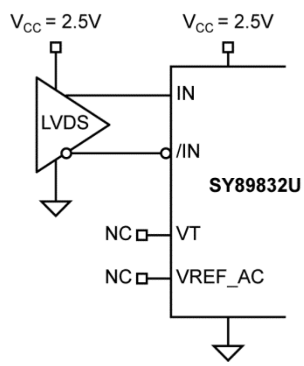


Figure 10. LVDS Input Interface

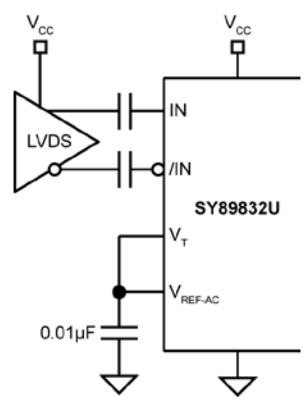
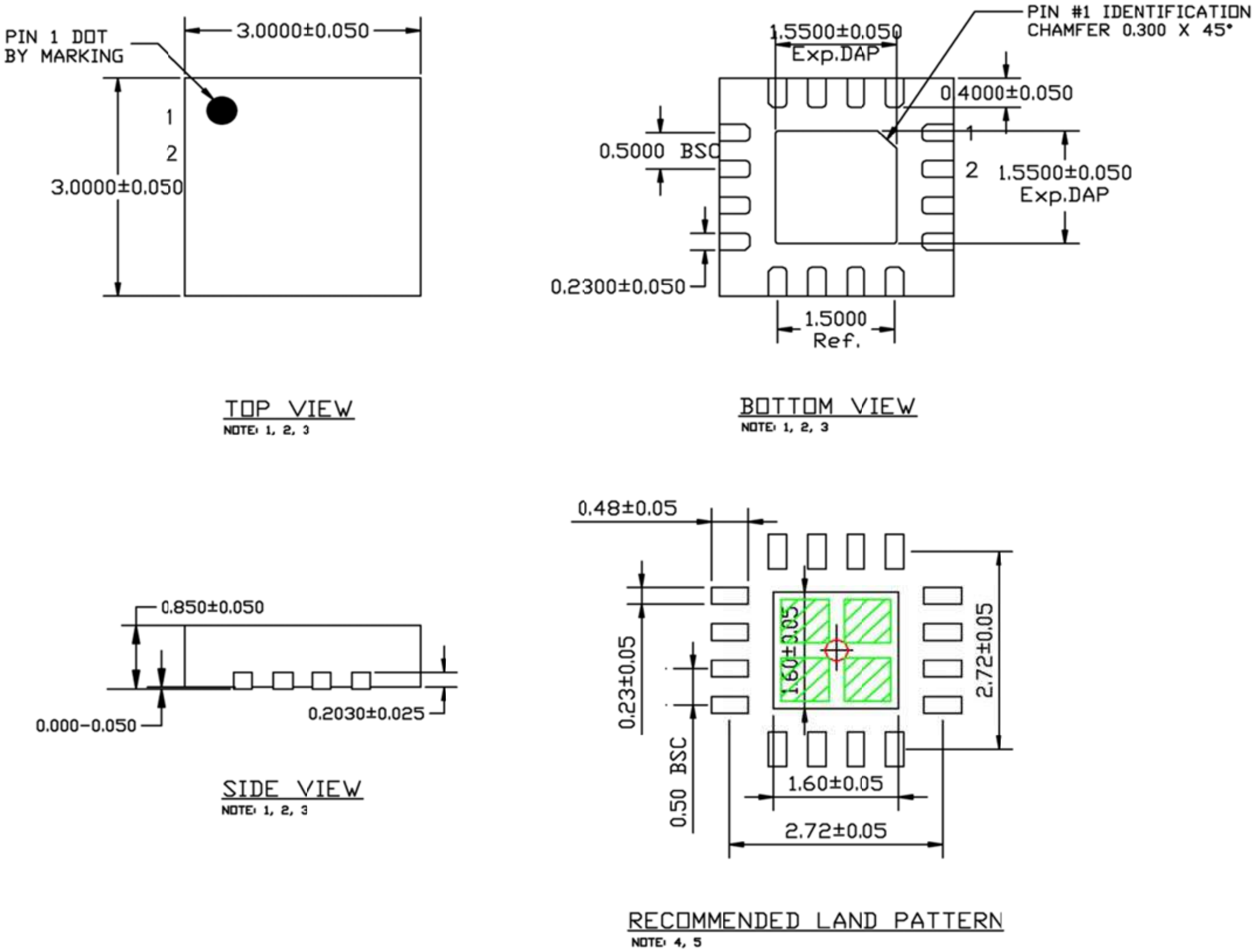


Figure 11. AC-Coupled LVDS Input Interface

tcghelp@micrel.com or (408) 955-1690

Package Information and Recommended Land Pattern[13]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

16-Pin 3mm × 3mm QFN (MM)

Note:

13. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

Micrel, Inc. is a leading global manufacturer of IC solutions for the worldwide high-performance linear and power, LAN, and timing & communications markets. The Company's products include advanced mixed-signal, analog & power semiconductors; high-performance communication, clock management, MEMs-based clock oscillators & crystal-less clock generators, Ethernet switches, and physical layer transceiver ICs. Company customers include leading manufacturers of enterprise, consumer, industrial, mobile, telecommunications, automotive, and computer products. Corporation headquarters and state-of-the-art wafer fabrication facilities are located in San Jose, CA, with regional sales and support offices and advanced technology design centers situated throughout the Americas, Europe, and Asia. Additionally, the Company maintains an extensive network of distributors and reps worldwide.