CSD23382F4 12-V P-Channel FemtoFET™ MOSFET

1 Features

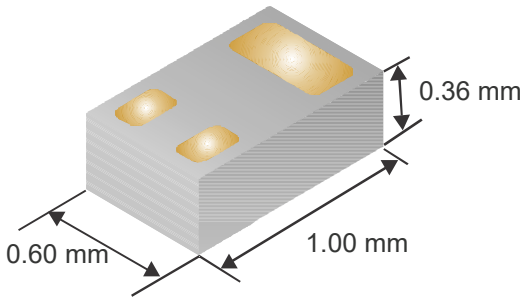
- Low on-resistance
- Ultra-low Q_g and Q_{gd}
- Ultra-small footprint (0402 case size)
  - 1.0 mm × 0.6 mm
- Low profile
  - 0.36-mm maximum height
- Integrated ESD protection diode
  - Rated > 2-kV HBM
  - Rated > 2-kV CDM
- Pb terminal plating
- Halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

3 Description

This 66-mΩ, 12-V P-channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Typical Device Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-source voltage	–12		V
Q_g	Gate charge total (–4.5 V)	1.04		nC
Q_{gd}	Gate charge gate-to-drain	0.15		nC
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V	149	mΩ
		V_{GS} = –2.5 V	90	
		V_{GS} = –4.5 V	66	
$V_{GS(th)}$	Threshold voltage	–0.8		V

Ordering Information[1]

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD23382F4	3000	7-inch reel	Femto (0402) 1.0 mm × 0.6 mm Land Grid Array (LGA)	Tape and reel
CSD23382F4T	250	7-inch reel		

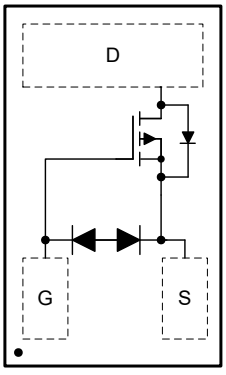
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-source voltage	–12	V
V_{GS}	Gate-to-source voltage	±8	V
I_D	Continuous drain current[1]	–3.5	A
I_{DM}	Pulsed drain current, T_A = 25°C[2]	–22	A
I_G	Continuous gate clamp current	–35	mA
	Pulsed gate clamp current[2]	–350	
P_D	Power dissipation[1]	500	mW
$V_{(ESD)}$	Human body model (HBM)	2	kV
	Charged device model (CDM)	2	kV
T_J, T_{stg}	Operating junction and storage temperature range	–55 to 150	°C

(1) Typical $R_{\theta JA}$ = 85°C/W on 1-inch² (6.45 cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52 mm) thick FR4 PCB.

(2) Pulse duration ≤ 100 µs, duty cycle ≤ 1%



Top View

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2021) to Revision E (January 2022)	Page
• Changed maximum height from "0.35-mm" to "0.36-mm" in *Features* section	1
• Changed maximum height from "0.35-mm" to "0.36-mm" in *Typical Device Dimensions*	1
• Changed maximum height from "0.35-mm" to "0.36-mm" in *Mechanical Dimensions* section	8

Changes from Revision C (October 2014) to Revision D (October 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added footnote with link to support document	9

Changes from Revision B (July 2014) to Revision C (October 2014)	Page
• Corrected timing V_{DS} to read –6 V	3

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–12			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –9.6 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –8 V			–10	µA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	–0.5	–0.8	–1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		149	199	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.5 A		90	105	mΩ
		V_{GS} = –4.5 V, I_{DS} = –0.5 A		66	76	mΩ
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.5 A		3.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –6 V, f = 1 MHz		180	235	pF
C_{oss}	Output Capacitance			118	154	pF
C_{rss}	Reverse Transfer Capacitance			12.8	16.6	pF
R_G	Series Gate Resistance			350		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –6 V, I_{DS} = –0.5 A		1.04	1.35	nC
Q_{gd}	Gate Charge Gate-to-Drain			0.15		nC
Q_{gs}	Gate Charge Gate-to-Source			0.50		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.18		nC
Q_{oss}	Output Charge	V_{DS} = –6 V, V_{GS} = 0 V		1.08		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –6 V, V_{GS} = –4.5 V, I_{DS} = –0.5 A,R_G = 2 Ω		28		ns
t_r	Rise Time			25		ns
$t_{d(off)}$	Turn Off Delay Time			66		ns
t_f	Fall Time			41		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = –0.5 A, V_{GS} = 0 V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= –6 V, I_F = –0.5 A, di/dt = 200 A/µs		1.8		nC
t_{rr}	Reverse Recovery Time			8.4		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYP	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)	85	°C/W
	Junction-to-Ambient Thermal Resistance(2)	245	

(1) Device mounted on FR4 material with 1-inch^2 (6.45 cm^2), 2-oz. (0.071-mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

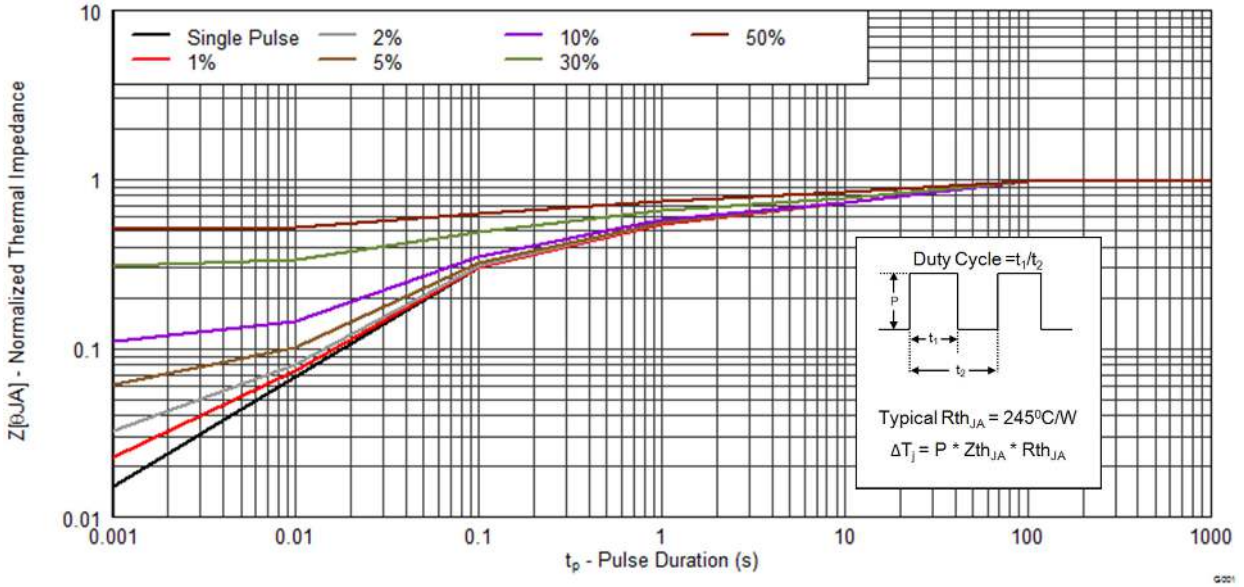


Figure 5-1. Transient Thermal Impedance

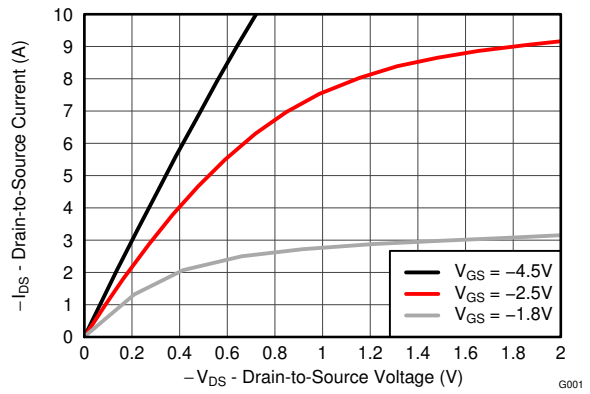
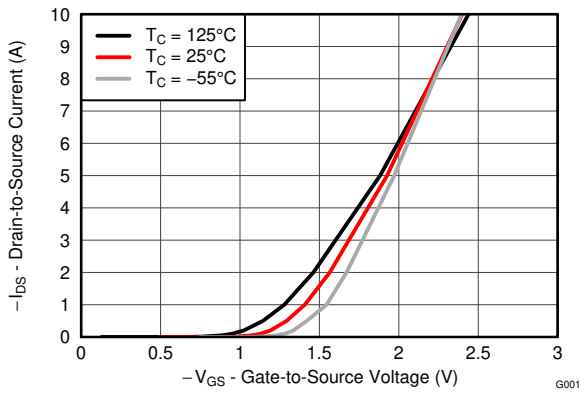


Figure 5-2. Saturation Characteristics

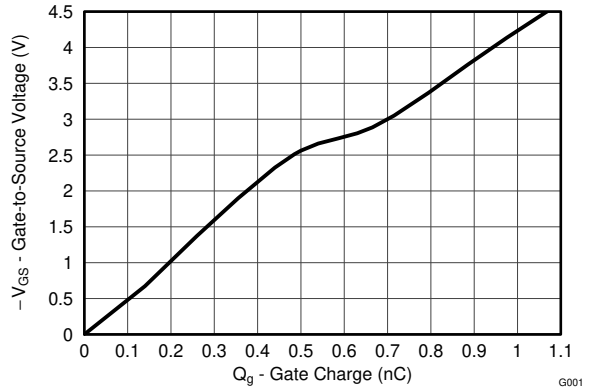


VDS = –5 V

Figure 5-3. Transfer Characteristics

5.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



I_D = –0.5 A V_{DS} = 6 V

Figure 5-4. Gate Charge

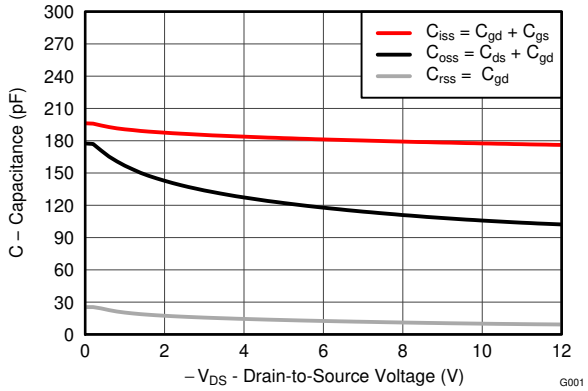
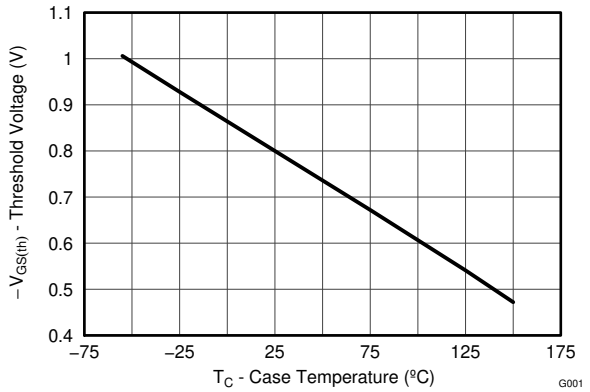


Figure 5-5. Capacitance



I_D = –250 µA

Figure 5-6. Threshold Voltage vs Temperature

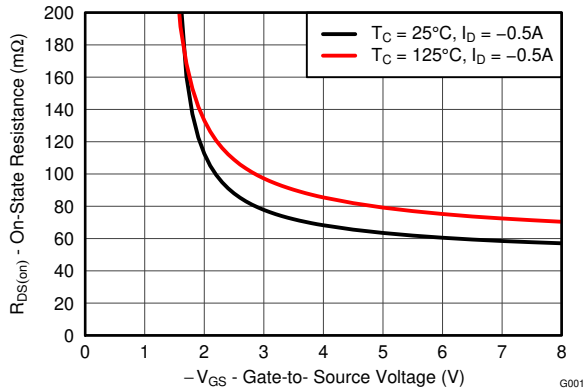
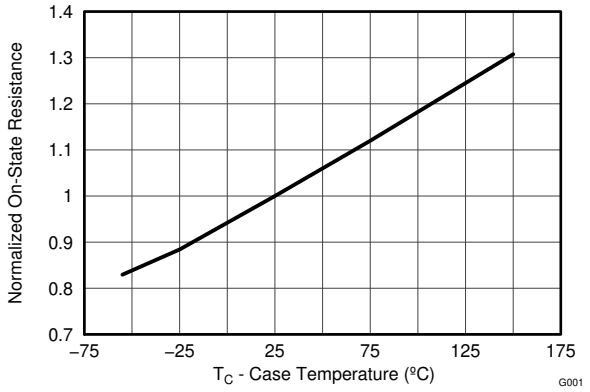


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



V_{GS} = –4.5 V I_D = –0.5 A

Figure 5-8. Normalized On-State Resistance vs Temperature

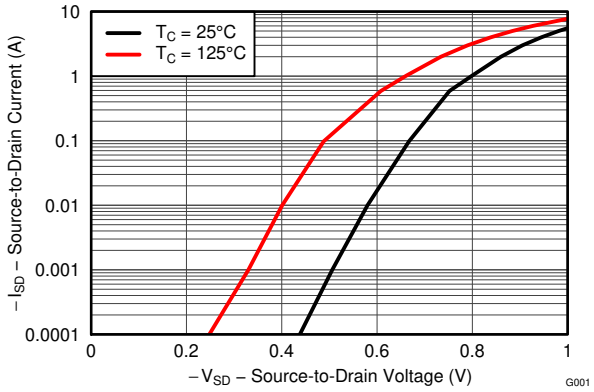
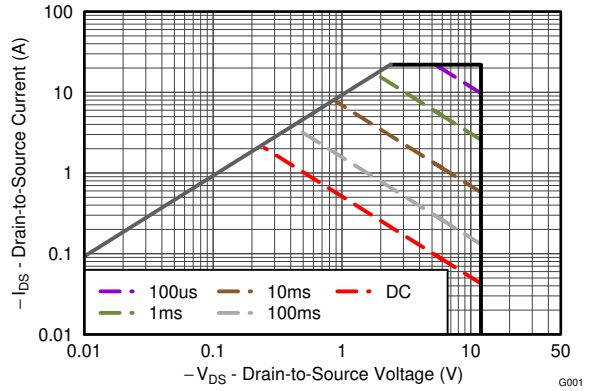


Figure 5-9. Typical Diode Forward Voltage

5.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



Single Pulse Typ $R_{\theta JA}$ = 245°C/W

Figure 5-10. Maximum Safe Operating Area

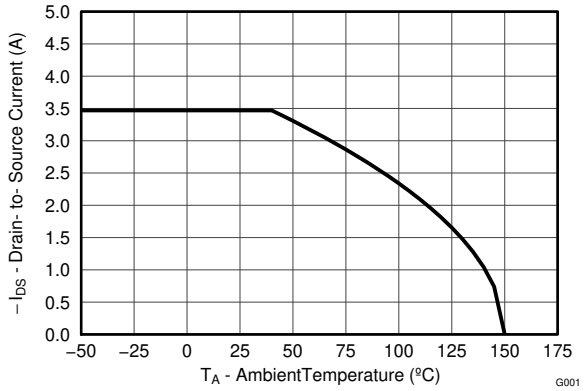


Figure 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

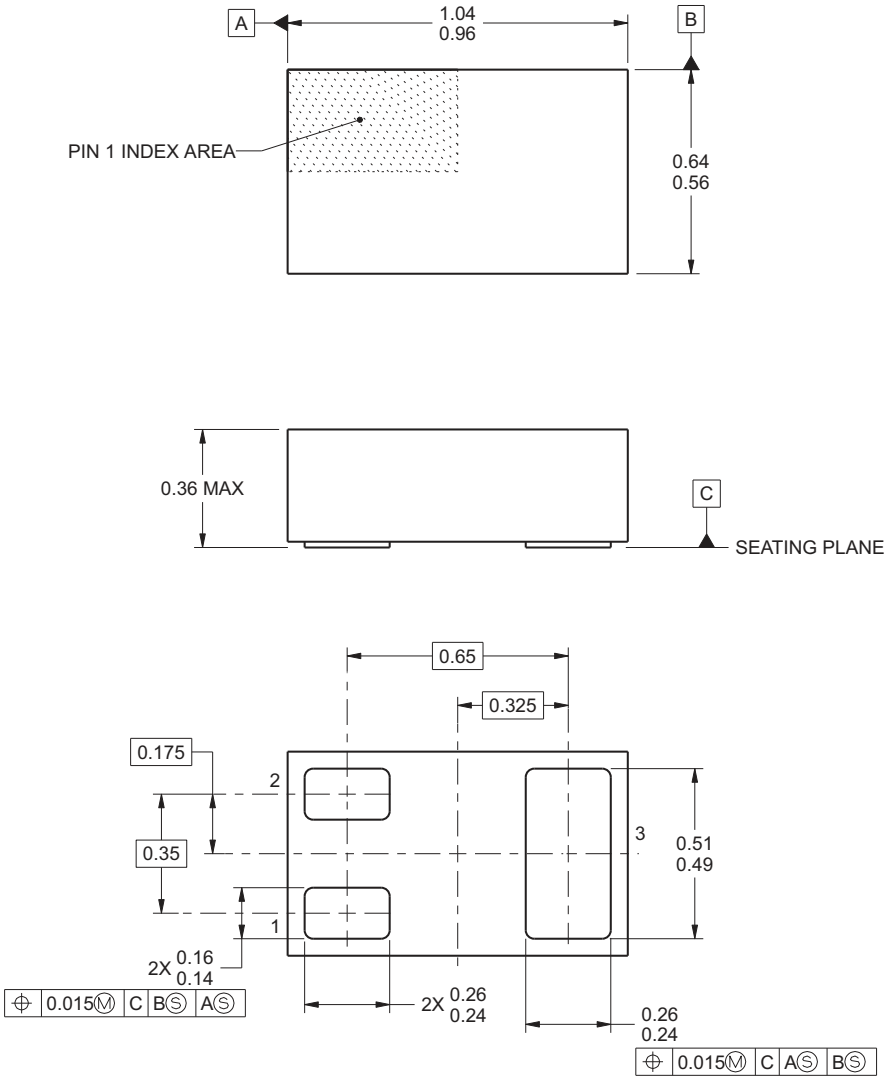
6.3 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

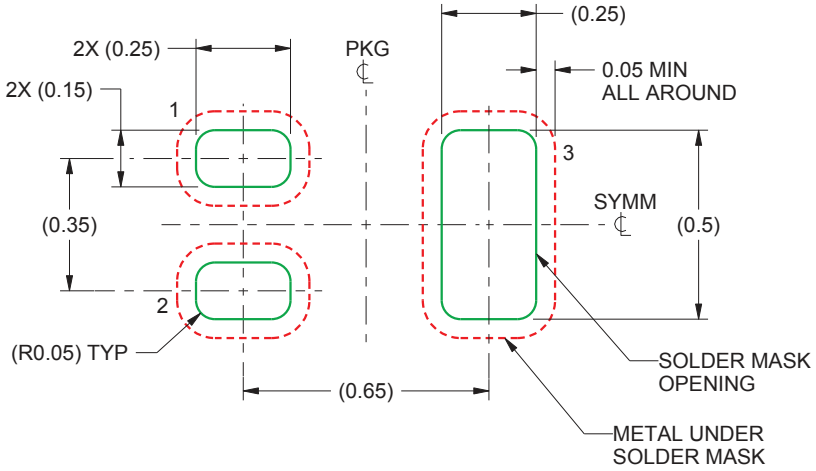


A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

Pin Configuration

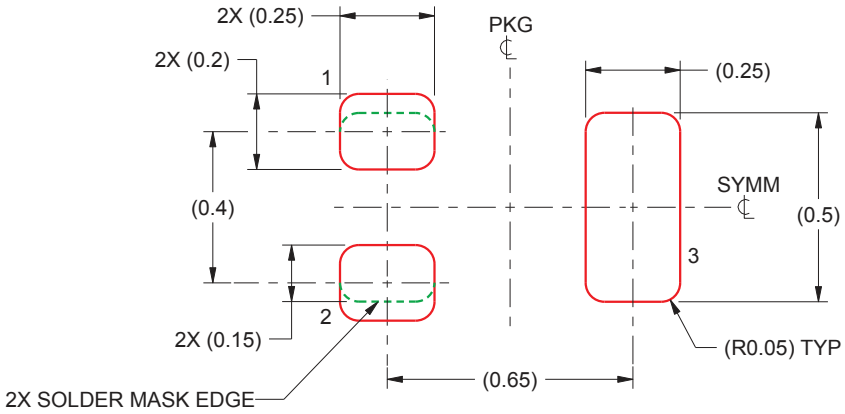
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



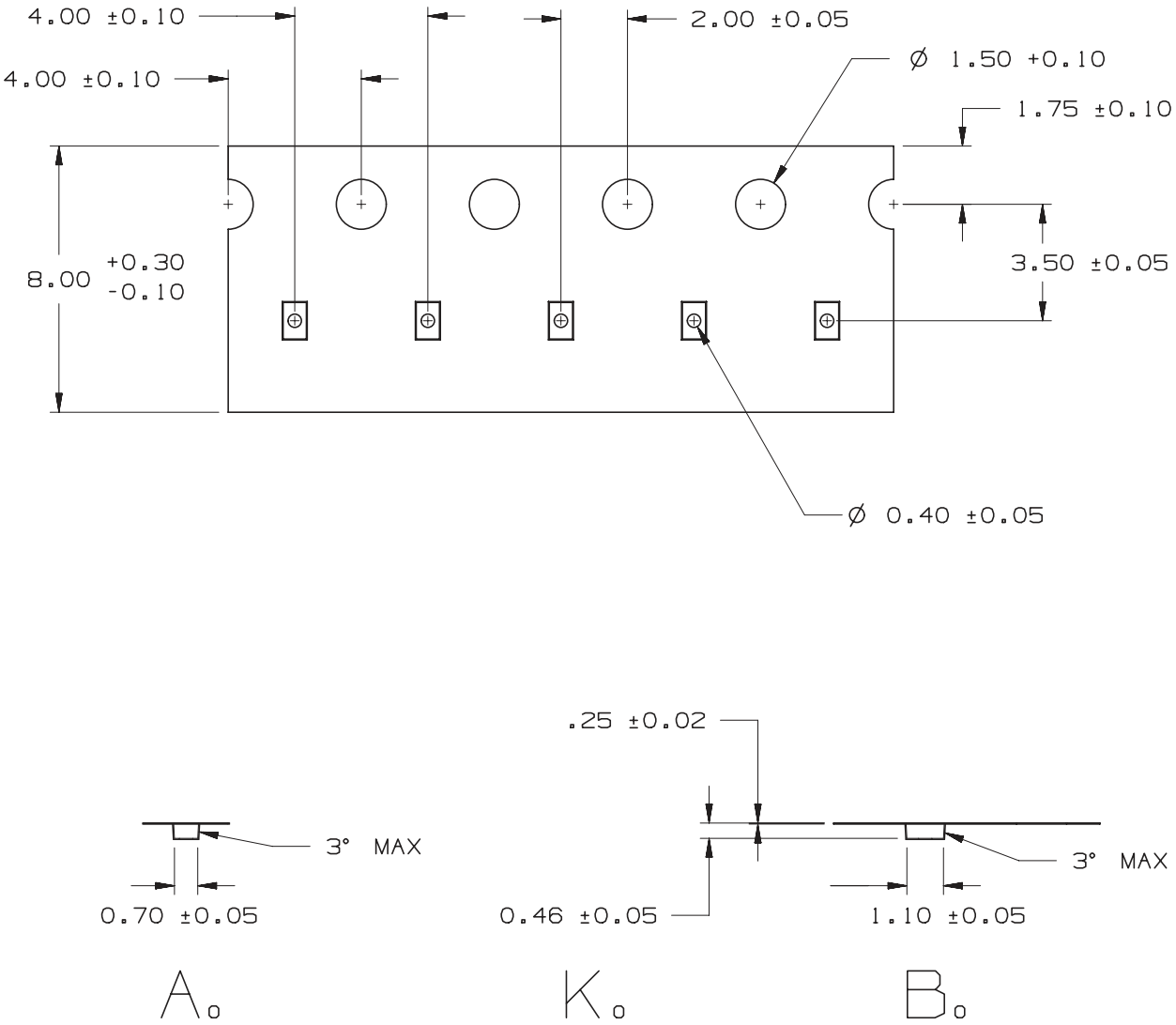
A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

7.4 CSD23382F4 Embossed Carrier Tape Dimensions



A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23382F4	ACTIVE	PICOSTAR	YJC	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	0 to 0	EM	Samples
CSD23382F4T	ACTIVE	PICOSTAR	YJC	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	EM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

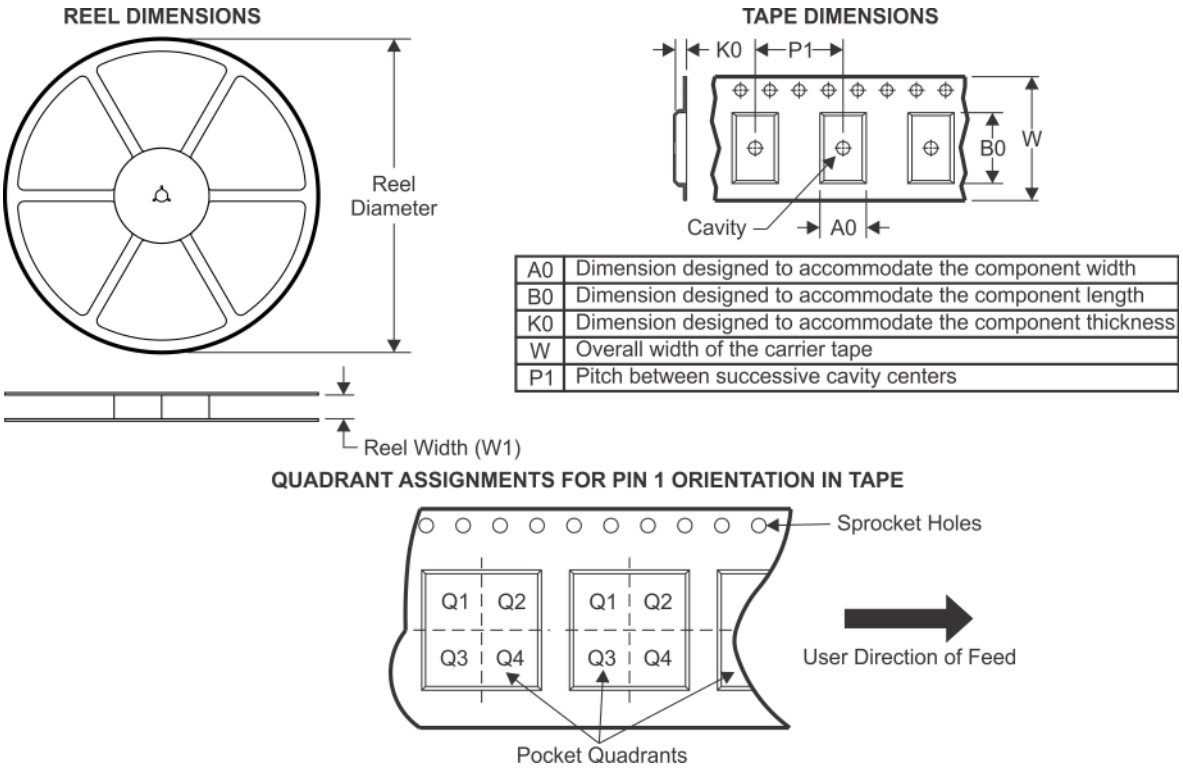
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

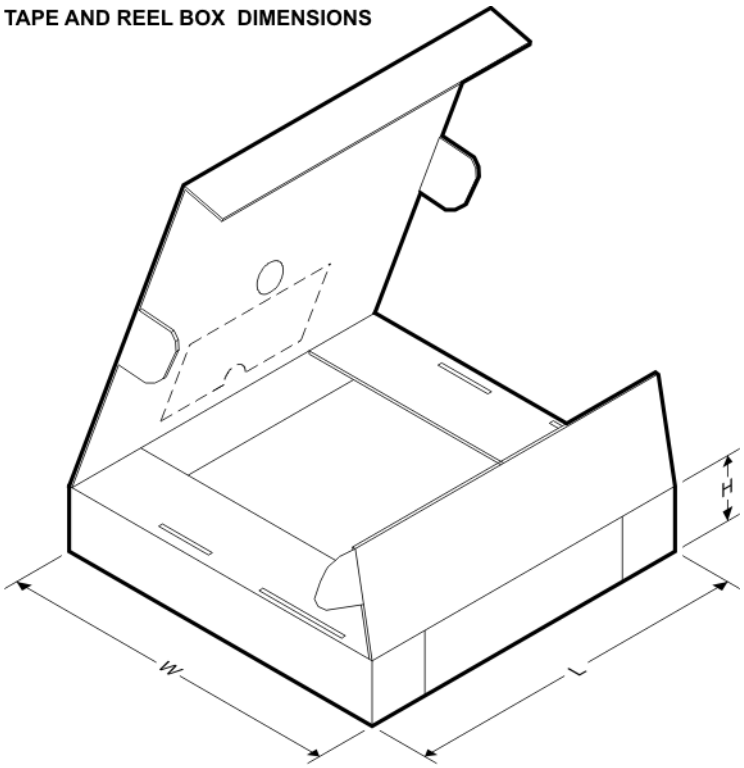


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD23382F4	PICOSTAR	YJC	3	3000	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD23382F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD23382F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD23382F4	PICOSTAR	YJC	3	3000	220.0	220.0	35.0
CSD23382F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD23382F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

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