ATWINC15x0B-MU

ATWINC15x0B-MU IEEE® 802.11 b/g/n Network Controller SoC

Introduction

The Microchip ATWINC15x0B is a single chip IEEE 802.11 b/g/n Radio/Baseband/MAC network controller optimized for low-power mobile applications. The ATWINC15x0B supports single stream 1x1 802.11n mode providing up to 72 Mbps PHY rate. The ATWINC15x0B features a fully integrated Power Amplifier (PA), Low Noise Amplifier (LNA), Switch and Power Management Unit (PMU). The ATWINC15x0B also features an on-chip microcontroller with Flash and RAM memory for system software. The ATWINC15x0B offers very low power consumption while simultaneously providing high performance and minimal bill of materials. The ATWINC15x0B can be interfaced with a host microcontroller (MCU) over Serial Peripheral Interface (SPI). The only external clock source required for the ATWINC15x0B is a high-speed crystal oscillator with 26 MHz frequency. The ATWINC15x0B is available as a QFN package.

The references to the ATWINC15x0B include the following devices, unless otherwise noted:

- ATWINC1500B
- ATWINC1510B

Features

- IEEE 802.11 b/g/n 20 MHz (1x1) Solution
- Single Spatial Stream in 2.4 GHz ISM Band
- Integrated T/R Switch
- Superior Sensitivity and Range via Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Supports Soft-AP
- Supports IEEE 802.11 WEP, WPA and WPA2 Security
- Supports Enterprise Security with WPA/WPA2 (802.11x) (supported from firmware release 19.6.1 and above):
  - EAP-TLS
  - EAP-PEAPv0/1 with TLS
  - EAP-TTLSv0 with MSCHAPv2
  - EAP-PEAPv0/1 with MSCHAPv2
- Superior MAC Throughput via Hardware Accelerated Two-Level A-MSDU/A-MPDU Frame Aggregation and Block Acknowledgment
- On-Chip Memory Management Engine to Reduce Host Load
- Integrated Wi-Fi® and Networking
- Complete Firmware Upgrade OTA
- Integrated Flash Memory for System Software
  - 4 Mb Flash - ATWINC1500B
  - 8 Mb Flash - ATWINC1510B
- SPI Host Interface
- Power Save Modes:

  - <4 µA Power Down mode typical at 3.3V I/O
  - 380 µA Doze mode with chip settings preserved (used for beacon monitoring)[1]
  - On-chip low-power sleep oscillator
  - Fast host wake up from the Doze mode by a pin or host I/O transaction
- Fast Boot Options:
  - On-chip boot ROM (firmware instant boot)
  - SPI Flash boot (firmware patches and state variables)
  - Low-leakage on-chip memory for state variables
  - Fast AP re-association (150 ms)
- On-Chip Network Stack to Offload MCU:
  - Network features: TCP, UDP, DHCP, ARP, HTTP, TLS and DNS
- Hardware Accelerators for Wi-Fi and TLS Security to Improve Connection Time
- Hardware Accelerator for IP Checksum
- Hardware Accelerators for OTA Security
- Operating Conditions:
  - Operating temperature: -40°C to +85°C (RF performance at room temperature of 25°C with a 2-3 dB change at boundary conditions)
  - I/O operating voltage (VDDIO): 2.7V to 3.6V
  - DC/DC converter power supply (VBAT): 3.0V to 4.2V

Notes:

1. For more details on the module power modes, refer to the Power Consumption section.
2. For more information on the software features, refer to the *Wi-Fi Network Controller Software Design Guide* (DS00002389).

Table of Contents

1. Ordering Information and IC Marking

The following table provides the ordering information for the ATWINC1500B and ATWINC1510B.

Table 1-1. Ordering Details

Ordering Code[1]	Package Type	Package Size	IC Marking
ATWINC1500B-MU-ABCD	QFN in Tray, Tape and Reel	5 mm x 5 mm	ATWINC1500B
ATWINC1510B-MU-ABCD	QFN in Tape and Reel	5 mm x 5 mm	ATWINC1510B

Note:

1. ABCD interprets as:
   "A" can be "Y" indicating Tray, or "T" indicating Tape and Reel.

   "BCD" equals to "042" for part assigned with MAC ID and blank for part with no MAC ID.

   The following table lists possible combinations for ordering the ATWINC1500B and ATWINC1510B.

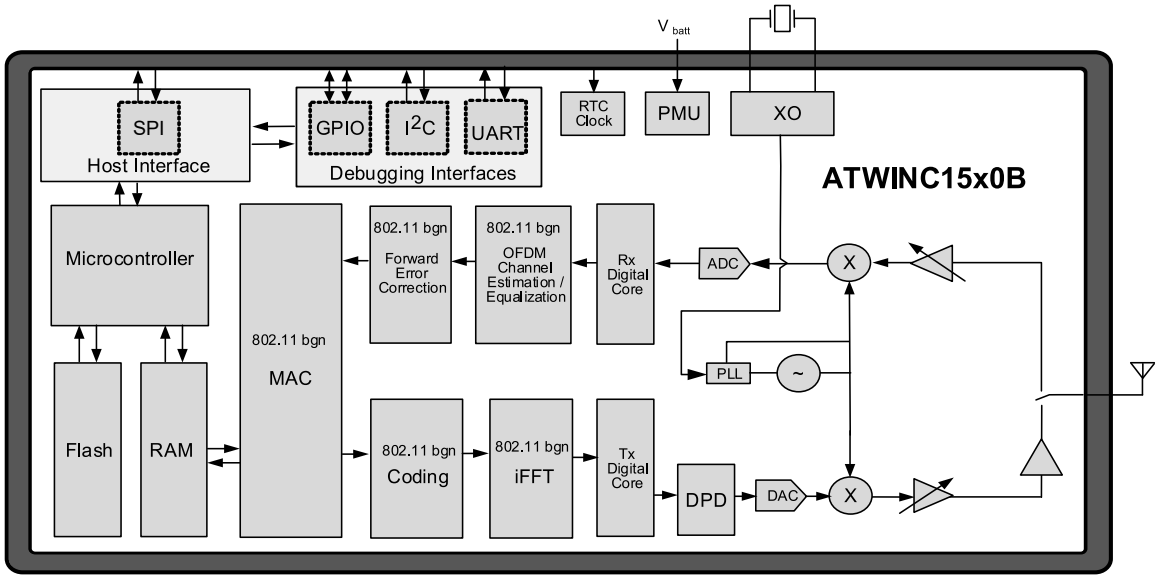
Ordering Code	Description
ATWINC1500B-MU-T	4 Mb Flash with no MAC ID and ship in Tape and Reel
ATWINC1500B-MU-Y	4 Mb Flash with no MAC ID and ship in Tray
ATWINC1500B-MU-Y042	4 Mb Flash with MAC ID assigned and ship in Tray
ATWINC1500B-MU-T042	4 Mb Flash with MAC ID assigned and ship in Tape and Reel
ATWINC1510B-MU-T	8 Mb Flash with no MAC ID and ship in Tape and Reel
ATWINC1510B-MU-Y	8 Mb Flash with no MAC ID and ship in Tray
ATWINC1510B-MU-Y042	8 Mb Flash with MAC ID assigned and ship in Tray
ATWINC1510B-MU-T042	8 Mb Flash with MAC ID assigned and ship in Tape and Reel

2. Functional Overview

2.1 Block Diagram

The ATWINC15x0B block diagram is shown in the following figure.

Figure 2-1. ATWINC15x0B Block Diagram

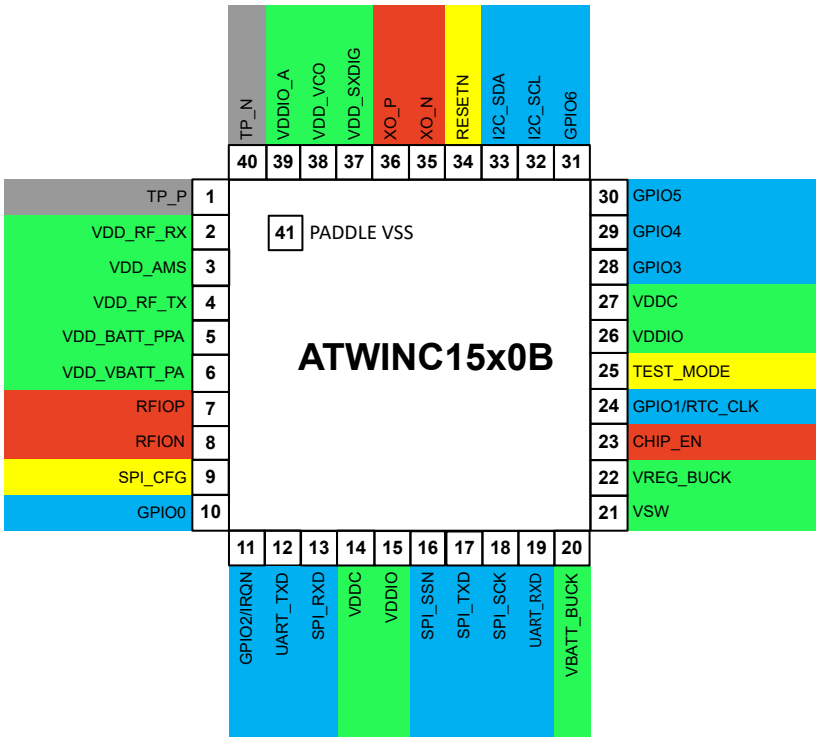


2.2 Pinout Information

The ATWINC15x0B is offered in an exposed pad 40-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in the following figure. The color shading is used to indicate the pin type as follows:

- Green – power
- Red – analog
- Blue – digital I/O
- Yellow – digital input
- Grey – unconnected or reserved

Figure 2-2. ATWINC15x0B Pin Assignment



2.3 Pinout Description

The ATWINC15x0B pins with default peripheral mapping are described in the following table.

Table 2-1. ATWINC15x0B Pin Description

Pin Number	Pin Name	Pin Type	Description
1	TP_P	Analog	Test pin/no connect
2	VDD_RF_RX	Power	Tuner RF supply(1)
3	VDD_AMS	Power	Tuner BB supply(1)
4	VDD_RF_TX	Power	Tuner RF supply(1)
5	VDD_BATT_PPA	Power	PA 1st stage supply(1)
6	VDD_VBATT_PA	Power	PA 2nd stage supply(1)
7	RFIOP	Analog	Positive RF differential I/O
8	RFION	Analog	Negative RF differential I/O
9	SPI_CFG	Digital Input	Tie to VDDIO through a 1 MΩ resistor to enable the SPI interface
10	GPIO0	Digital I/O, Programmable Pull-Up	GPIO0(2)
11	GPIO2/IRQN	Digital I/O, Programmable Pull-Up	GPIO2(2)/ATWINC15x0B interrupt output; connect to host interrupt input pin

.....continued

Pin Number	Pin Name	Pin Type	Description
12	UART_TXD	Digital I/O, Programmable Pull-Up	UART transmit output from ATWINC15x0B; added for debug and testing only
13	SPI_RXD	Digital I/O, Programmable Pull-Up	SPI MOSI (Master Out, Slave In) pin
14	VDDC	Power	Digital core power supply(1)
15	VDDIO	Power	Digital I/O power supply(1)
16	SPI_SSN	Digital I/O, Programmable Pull-Up	SPI slave select (active-low)
17	SPI_TXD	Digital I/O, Programmable Pull-Up	SPI MISO (Master In, Slave Out) pin
18	SPI_SCK	Digital I/O, Programmable Pull-Up	SPI clock
19	UART_RXD	Digital I/O, Programmable Pull-Up	UART receive input to ATWINC15x0B; added for debug and testing only
20	VBATT_BUCK	Power	Battery supply for DC/DC converter(1)
21	VSW	Power	Switching output of DC/DC converter(1)
22	VREG_BUCK	Power	• Core power from DC/DC converter(1) • Decouple with 10 µF and 0.01 µF capacitor to GND and place these capacitors as recommended in 10.1.3 Power Management Unit
23	CHIP_EN	Analog	• Module enable pin • High level enables the module and low level places module in Power-Down mode • By default, connect a host output to low at power-up; if the host output is tristated, add a 1 MΩ pull-down resistor to ensure a low level at power-up
24	GPIO1/RTC_CLK	Digital I/O, Programmable Pull-Up	GPIO1/32 kHz clock input(2)
25	TEST_MODE	Digital Input	Test mode – User must tie this pin to GND
26	VDDIO	Power	Digital I/O power supply(1)
27	VDDC	Power	Digital core power supply(1)
28	GPIO3	Digital I/O, Programmable Pull-Up	GPIO3(2)
29	GPIO4	Digital I/O, Programmable Pull-Up	GPIO4(2)
30	GPIO5	Digital I/O, Programmable Pull-Up	GPIO5(2)
31	GPIO6	Digital I/O, Programmable Pull-Up	GPIO6(2)

.....continued			
Pin Number	**Pin Name**	**Pin Type**	**Description**
32	I2C_SCL	Digital I/O, Programmable Pull-Up	• I^2C slave clock (high-drive pad, see ATWINC15x0B Electrical Characteristics table) • Currently, used only for debug development • Leave unconnected • It is recommended to add Test Point (TP) to this pin
33	I2C_SDA	Digital I/O, Programmable Pull-Up	• I^2C slave data (high-drive pad, see ATWINC15x0B Electrical Characteristics table) • Currently, used only for debug development • Leave unconnected • It is recommended to add Test Point (TP) to this pin
34	RESETN	Digital Input	• Active-low hard Reset • Assert low to put the module in Reset state • Assert high to put the module in Normal state and move it out of Reset state • By default, connect a host output to low at power-up; if the host output is tri-stated, add a 1 MΩ pull-down resistor to ensure a low level at power-up
35	XO_N	Analog	Crystal oscillator N
36	XO_P	Analog	Crystal oscillator P
37	VDD_SXDIG	Power	SX power supply(1)
38	VDD_VCO	Power	VCO power supply(1)
39	VDDIO_A	Power	Tuner VDDIO power supply(1)
40	TP_N	Analog	Test pin/no connect
41	PADDLE VSS	Power	Connect to system board ground

Notes:

1. For more information, refer to 7.1 Power Architecture.
2. Usage of the GPIO functionality is not supported by the ATWINC15x0 firmware. The data sheet will be updated once the support for this feature is added.

2.4 Package Description

The following table provides information on the physical details of the ATWINC15x0B devices.

Table 2-2. ATWINC15x0B QFN Package Information

Parameter	Value	Units	Tolerance
Package size	5x5	mm	±0.1 mm
QFN pad count	40	mm	-
Total thickness	0.85	mm	+0.15/-0.05 mm

.....continued

Parameter	Value	Units	Tolerance
QFN pad pitch	0.40	mm	-
Pad width	0.20	mm	±0.05 mm
Exposed pad size	3.85 x 3.85	mm	-

For drawing details, see 11. Package Outline Drawing.

3. Clocking

This section details the clocking sources of the ATWINC15x0B.

3.1 Crystal Oscillator

The following table provides the values of the ATWINC15x0B crystal oscillator parameters.

Table 3-1. ATWINC15x0B Crystal Oscillator Parameters

Parameter	Min.	Typ.	Max.	Unit
Crystal resonant frequency	—	26	—	MHz
Crystal equivalent series resistance	—	50	150	Ω
Stability – Initial offset(1)	-100	—	100	ppm

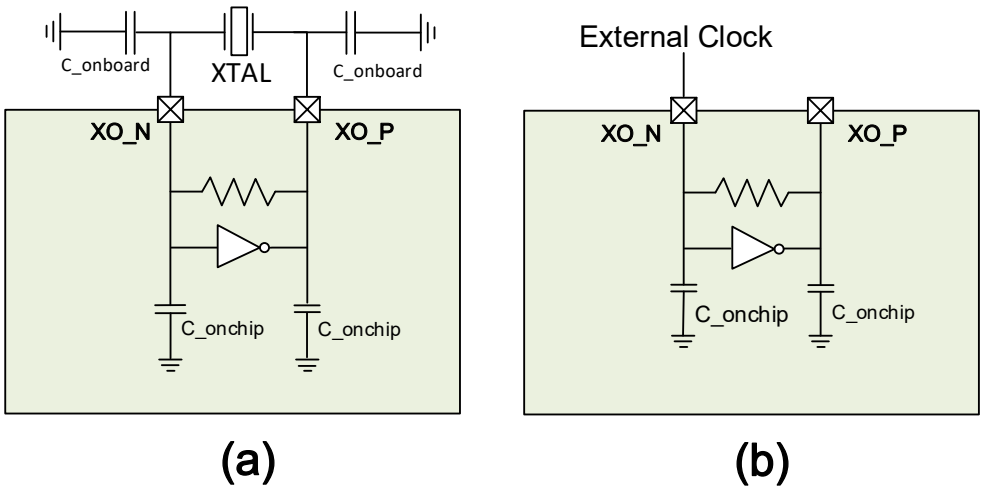
Note:

1. The initial offset must be calibrated to maintain ±25 ppm in all operating conditions. This calibration is performed during final production testing.

The block diagram in the following figure (a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5 pF internal capacitance on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5 pF can be applied to the XO_N terminal as shown the following figure (b).

The XO has 5 pF internal capacitance on each terminal XO_P and XO_N. This internal capacitance must be considered when calculating the external loading capacitance, c_onboard, for the XTAL.

Figure 3-1. ATWINC15x0B XO Connections



(a) Crystal Oscillator is Used

(b) Crystal Oscillator is Bypassed

The following table specifies the electrical and performance requirements for the external clock.

Table 3-2. ATWINC15x0B Bypass Clock Specification

Parameter	Min.	Typ.	Max.	Unit	Comments
Oscillator frequency	—	26	—	MHz	Must drive 5 pF load at desired frequency
Voltage swing	0.5	—	1.2	Vpp	Must be AC coupled
Stability – Temperature and aging	-25	—	+25	ppm	—
Phase noise	—	—	-130	dBc/Hz	At 10 kHz offset
Jitter (RMS)	—	—	<1	psec	Based on integrated phase noise spectrum from 1 kHz to 1 MHz

3.2 Low-Power Oscillator

The ATWINC15x0B has an internal 32 kHz clock to provide timing information to various Sleep functions. Alternatively, the ATWINC15x0B allows an 32 kHz external clock for this purpose, which is provided through pin 24 (RTC_CLK). The software is used to select between the internal clock and the external clock.
Note: The current software implementation does not require an 32.768 kHz clock.

The internal low-power clock is a ring-oscillator and has accuracy within 10,000 ppm. When using the internal low-power clock, the advance wake-up time in the beacon monitoring mode must be increased to 1% of the sleep time to compensate for the oscillator inaccuracy. For example, for the DTIM interval value of 1, wake-up time must be increased by 1 ms.

4. CPU and Memory Subsystem

This chapter describes the Cortus APS3 32-bit processor and memory subsystem of the ATWINC15x0B.

4.1 Processor

The ATWINC15x0B has a Cortus APS3 32-bit processor. The processor performs MAC functions, including but not limited to: association, authentication, power management, security key management and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as Station (STA) and Access Point (AP) modes.

4.2 Memory Subsystem

The APS3 core uses a 128 KB instruction/boot ROM along with a 160 KB instruction RAM and a 64 KB data RAM. The ATWINC15x0B devices are populated with either 4 Mb or 8 Mb of Flash memory depending on the model that is ordered. This memory can be used for system software. For more information, see the Ordering Details table. In addition, the device uses a 128 KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

4.3 Nonvolatile Memory (eFuse)

The ATWINC15x0B IC have 768 bits of nonvolatile eFuse memory that can be read by the CPU after device Reset. The eFuse is partitioned into six 128-bit banks (Bank 0 – Bank 5). Each bank has the same bitmap (refer to the following figure). The purpose of the first 80 bits in each bank is fixed and the remaining 48 bits are general-purpose software-dependent bits, or reserved for future use.

Note: If the IQ Amp Used, IQ Amp Correction, IQ Pha Used and IQ Pha Correction bit fields are programmed, Bank 0 must not be programmed with any values; only the Bank Invalid bit has to be programmed in this case.

This nonvolatile one-time-programmable (OTP) memory can be used for storing the following customer-specific parameters:

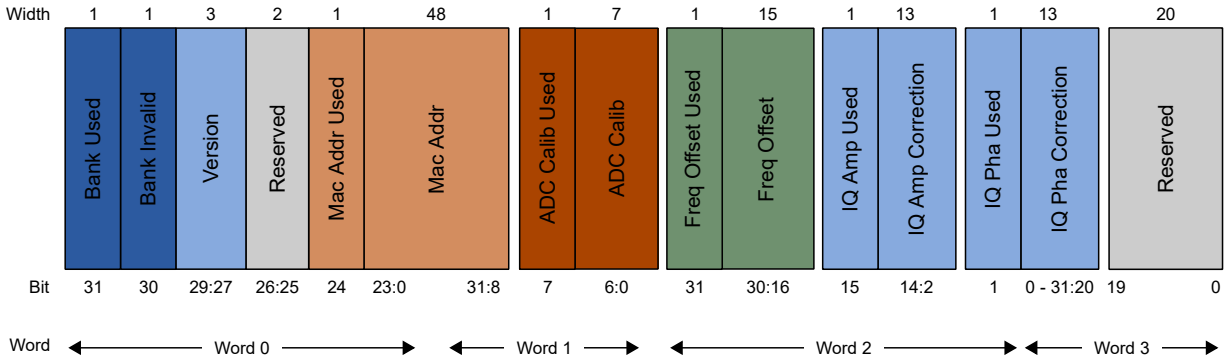
- MAC address
- Calibration information (TX power, crystal frequency offset and so on)
- Other software-specific configuration parameters

Several updates of the device parameters are allowed after the initial programming because each bank can be programmed independently. For example, if the MAC address is currently programmed in Bank 2 and the MAC address has to be changed. To change this, perform the following steps:

1. Contents of Bank 2 have to be invalidated by programming the Bank Invalid bit.
2. Bank 3 has to be programmed with the new MAC address along with the values of ADC Calib (if used in Bank 2), frequency offset (from Bank 2), IQ Amp Correction (from Bank 2) and IQ Pha Correction (from Bank 2). The used bit field for the corresponding bit field must also be programmed.
3. Contents of Bank 3 have to be validated by programming the used bit field of Bank 3.

Each bit field (i.e., MAC Addr, ADC Calib, Freq Offset, IQ Amp Correction and IQ Pha Correction) has its corresponding Used bit field. This Used bit field indicates to the firmware that the values in these bit fields are valid. A value of '0' in the Used bit field indicates that the following bit field is invalid and a value of '1' programmed to the Used bit field indicates that the corresponding bit field is valid and can be used by the firmware. By default, all the ATWINC15x0B devices are programmed with IQ Amp and IQ Phase fields of Bank 1. In IC variants where the MAC address is assigned, the MAC address bit field is programmed in Bank 1. For more information on IC marking, refer to Ordering Details.

Figure 4-1. Bit Map for ATWINC15x0B eFuse Bank *(1)*



Note:

1. The bit map has been updated with bit fields, IQ Amp Correction and IQ Pha Correction fields, from firmware version 19.7 onwards. Earlier, these bit fields were reserved for future use. For customers using firmware older than 19.7, IQ Amp Correction and IQ Pha Correction bit fields are not used by the firmware.

The matrix table below provides details on how different versions of the firmware would handle the IQ Amp Used, IQ Amp Correction, IQ Pha Used and IQ Pha Correction bit fields during initialization.

Firmware Version Used by Customer	IQ Amp Used and IQ Pha Used Bit Status	
	Device with IQ Amp Used and IQ Pha Used Bits with Value '1'	Device with IQ Amp Used and IQ Pha Used Bits with Value '0'
19.7 or later for WINC1500	The firmware loads the IQ cal values from the IQ Amp Correction and IQ Pha Correction bit fields of the corresponding eFuse bank and proceeds with the initialization.	The firmware ignores the values in the IQ Amp Correction and IQ Pha Correction bit fields of the corresponding eFuse bank and proceeds with the initialization.
Prior to 19.7 for WINC1500	The firmware does not check for the IQ Amp and IQ Pha Used bit fields and proceeds with initialization.	

5. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

5.1 MAC

The ATWINC15x0B MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP and WPA2 CCMP-AES.

The control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, beacon TX control, interframe spacing and so on), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication) and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

5.1.1 Features

The ATWINC15x0B IEEE 802.11 MAC supports the Following Functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF Multiple Access Categories Traffic Scheduling
- Advanced IEEE 802.11n Features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate block acknowledgment
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA Security with Key Management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Advanced Power Management
  - Standard 802.11 power save mode
- RTS-CTS and CTS-Self Support
- Supports Either STA or AP Mode in the Infrastructure Basic Service Set Mode

5.2 PHY

The ATWINC15x0B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in Single Stream mode with 20 MHz bandwidth. Advanced algorithms are employed to achieve maximum throughput in a real-world communication environment with impairments and interference. The PHY implements all the required functions that include FFT, filtering, FEC (Viterbi decoder), frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

5.2.1 Features

The ATWINC15x0B IEEE 802.11 PHY supports the following functions:

- Single Antenna 1x1 Stream in 20 MHz Channels
- Supports IEEE 802.11b DSSS-CCK Modulation: 1, 2, 5.5, 11 Mbps
- Supports IEEE 802.11g OFDM Modulation: 6, 9, 12,18, 24, 36, 48, 54 Mbps
- Supports IEEE 802.11n HT Modulations MCS0-7, 20 MHz, 800 ns and 400 ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2 Mbps(1)
- IEEE 802.11n Mixed Mode Operation
- Per Packet TX Power Control
- Advanced Channel Estimation/Equalization, Automatic Gain Control, CCA, Carrier/Symbol Recovery and Frame Detection

Note:

1. Currently, short GI is not supported by firmware. The data sheet will be updated when the feature is supported.

5.3 Radio

This section describes the properties and characteristics of ATWINC15x0B and Wi-Fi radio transmit and receive performance capabilities of the IC.

The performance measurements are taken at the RF pin assuming 50Ω differential; the RF performance is assured for room temperature of 25ºC with a derating of 2 dB to 3 dB at boundary conditions.

Measurements are taken under typical conditions: VBATT=3.3 V; VDDIO=3.3 V; temperature: +25ºC

Table 5-1. Features and Properties

Feature	Description
Part number	ATWINC15x0B-MU
WLAN standard	IEEE 802.11 b/g/n, Wi-Fi compliant
Host interface	SPI
Frequency range	2.412 GHz ~ 2.484 GHz (2.4 GHz ISM Band)
Number of channels	11 for North America 13 for Europe 14 for Japan
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM /64-QAM,16-QAM, QPSK, BPSK
Data rate	802.11b: 1, 2, 5.5, 11 Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Data Rate (20 MHz, normal GI, 800 ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps

.....continued	
Feature	**Description**
Data Rate (20 MHz, short GI, 400 ns)(1)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2 Mbps
Operating temperature	-40 to +85ºC
Storage temperature	-40 to +125 ºC
Humidity	Operating humidity: 10% to 95% Non-condensing Storage humidity: 5% to 95% Non-condensing

Note:

1. Currently, short GI is not supported by firmware. The data sheet will be updated when the feature is supported.

6. External Interfaces

The ATWINC15x0B external interfaces include:

- I^2C slave for debug
- SPI slave for control and data transfer
- One UART for debug
- General Purpose Input/Output (GPIO) pins(1)

Note:

1. Usage of the GPIO functionality is not supported by the ATWINC15x0 firmware. The data sheet will be updated once the support for this feature is added.

6.1 Interfacing with the Host Microcontroller

This section describes interfacing the ATWINC15x0B with the host microcontroller. The interface is comprised of a slave SPI and additional control signals, as shown in the following figure. For more information on SPI interface specification and timing, refer to the SPI Interface. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 6-1. Interfacing with the Host Microcontroller

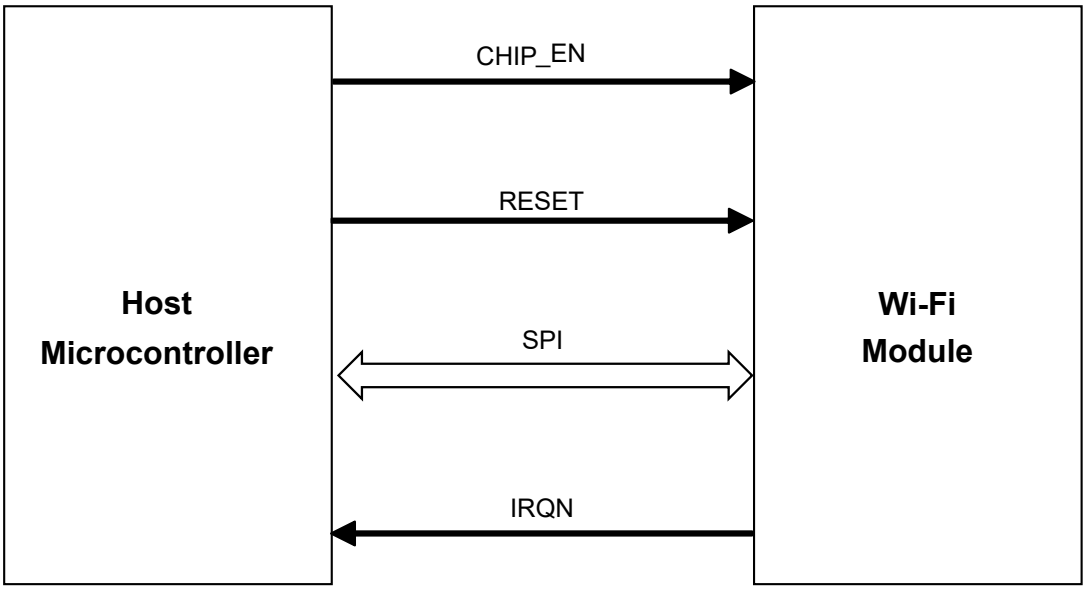


Table 6-1. Host Microcontroller Interface Pins

Pin Number	Function
11	IRQN
13	SPI_MOSI
16	SPI_SSN
17	SPI_MISO
18	SPI_CLK
23	CHIP_EN
34	RESETN

6.2 SPI Slave Interface

The ATWINC15x0B provides a Serial Peripheral Interface (SPI) that operates as an SPI slave. This is the main interface to the host. The SPI slave interface can be used to control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in the following table. The RXD pin is the same as the Master Output, Slave Input (MOSI) and the TXD pin is the same as the Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available following Reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 6-2. ATWINC15x0B SPI Slave Interface Pin Mapping

Pin Number	Pin Name	SPI Function
9	SDIO_SPI_CFG	Must be tied to VDDIO
16	SSN	Active low slave select
18	SPI_SCK	Serial clock
13	SPI_RXD	Serial data receive (MOSI)
17	SPI_TXD	Serial data transmit (MISO)

When the SPI is not selected, that is, when SSN is high, the SPI interface does not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

The SPI slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiates DMA transfer.

The SPI slave interface supports four Standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

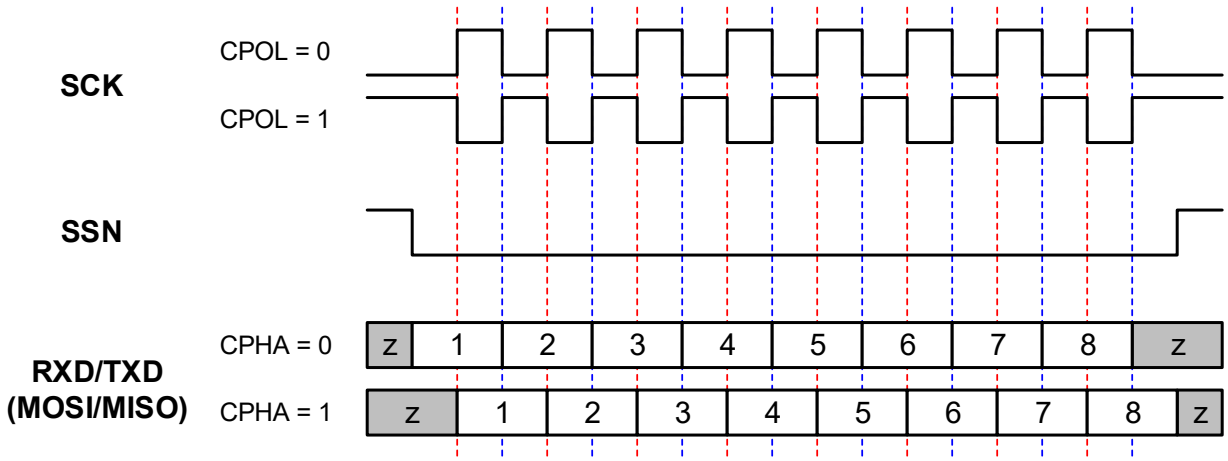
Table 6-3. SPI Modes

Mode	CPOL	CPHA
0[1]	0	0
1	0	1
2	1	0
3	1	1

Note:

1. The ATWINC15x0 firmware uses SPI MODE 0 to communicate with the host.

Figure 6-2. ATWINC15x0B SPI Slave Clock Polarity and Clock Phase Timing



The red lines in the following figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Figure 6-3. ATWINC15x0BSPI Slave Timing Diagram

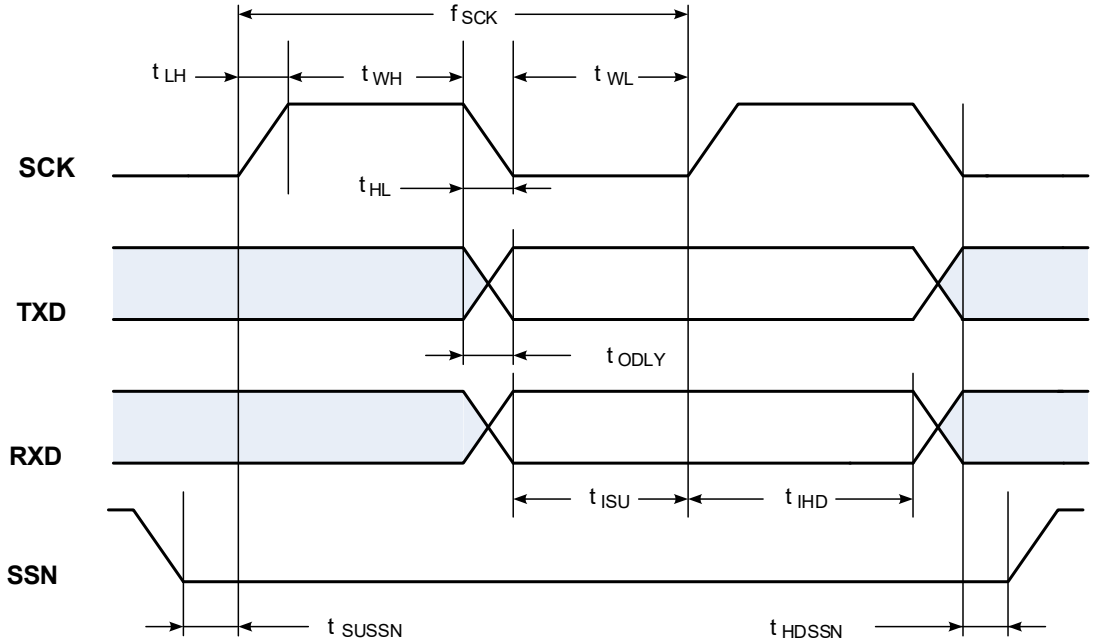


Table 6-4. ATWINC15x0B SPI Slave Timing Parameters (1)

Parameter	Symbol	Min.	Max.	Units
Clock input frequency(2)	f_{SCK}	—	48	MHz
Clock low pulse width	t_{WL}	4	—	ns
Clock high pulse width	t_{WH}	5	—	
Clock rise time	t_{LH}	0	7	
Clock fall time	t_{HL}	0	7	
TXD output delay(3)	t_{ODLY}	4	9 from SCK fall	
RXD input setup time	t_{ISU}	1	—	
RXD input hold time	t_{IHD}	5	—	
SSN input setup time	t_{SUSSN}	3	—	
SSN input hold time	t_{HDSSN}	5.5	—	

Note:

1. Timing is applicable to all the SPI modes.
2. Maximum clock frequency specified is limited by the SPI slave interface internal design. Actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing is based on 15 pF output loading. Under all conditions, $t_{LH} + t_{WH} + t_{HL} + t_{WL}$ must be less than or equal to $1/f_{SCK}$.

6.3 UART Interface

The ATWINC15x0B supports the Universal Asynchronous Receiver/Transmitter (UART) interface. This interface is intended for debugging purposes only. The UART is available on pins 12 and 19. It is recommended to add test

points for these pins. The UART is compatible with the RS-232 standard and the ATWINC15x0B operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

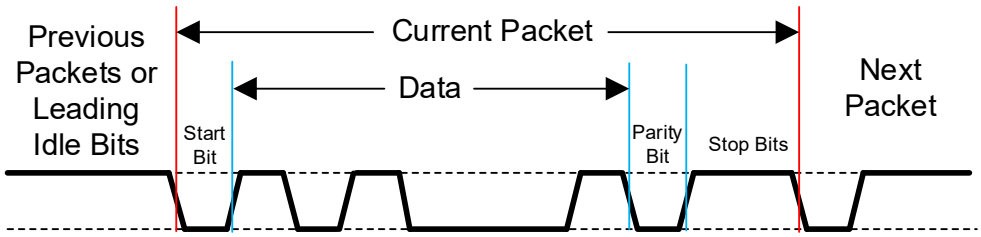
The following is the default configuration for accessing the UART interface of the ATWINC15x0B:

- Baud rate: 460800
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of the UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity and two stop bits.

Figure 6-4. Example of UART RX or TX Packet



6.4 GPIO Pins

Seven General Purpose Input/Output (GPIO) pins, labeled GPIO 0 to 6, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input.

Note: Usage of the GPIO functionality is not supported by the WINC15x0 FW. The datasheet will be updated once the support for this feature is added.

7. Power Management

7.1 Power Architecture

The ATWINC15x0B uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. This architecture is shown in the following figure. The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the core supply used by the digital and RF/AMS blocks. The following table shows the typical values for the digital and RF/AMS core voltages. The PA and eFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure.

Figure 7-1. ATWINC15x0B Power Architecture

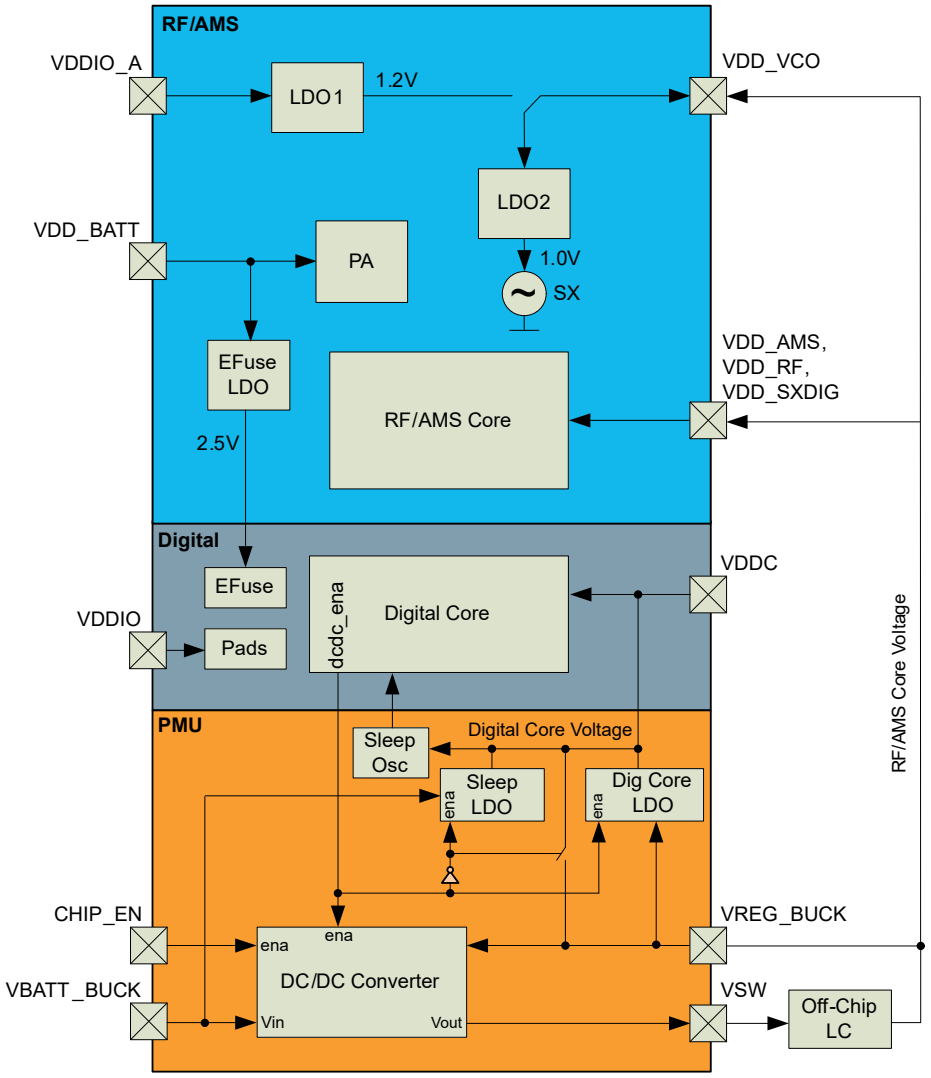


Table 7-1. ATWINC15x0B Power Consumption

Parameter	Typical
RF/AMS Core Voltage (VREG_BUCK)	1.25V
Digital Core Voltage (VDDC)	1.10V

The power connections in Figure 7-1 provide a conceptual framework for understanding the ATWINC15x0B power architecture. For more details on reference design, see 9. Reference Design for an example of power supply connections, including proper isolation of the supplies used by the digital and RF/AMS blocks.

7.2 Power Consumption

7.2.1 Description of Device States

The ATWINC15x0B has several device states:

- ON_Transmit – Device is actively transmitting an 802.11 signal with highest output power and nominal current consumption
- ON_Receive – Device is actively receiving an 802.11 signal with lowest sensitivity and nominal current consumption
- ON_Doze – Device is ON but is neither transmitting nor receiving
- Power_Down – Device core supply off (leakage)
- IDLE connect – Device is connected with one DTIM beacon interval

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – Device pin (pin 23) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state CHIP_EN has to change between high and low (GND) voltage. When VDDIO is OFF and CHIP_EN is low, the chip is powered off with no leakage (for more information, refer to 7.2.2 Restrictions for Power States).

7.2.2 Restrictions for Power States

When no power is supplied to the device, that is, the DC/DC Converter output and VDDIO are OFF (at ground potential), a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode turns on when a voltage higher than one diode-drop is supplied to the pin.

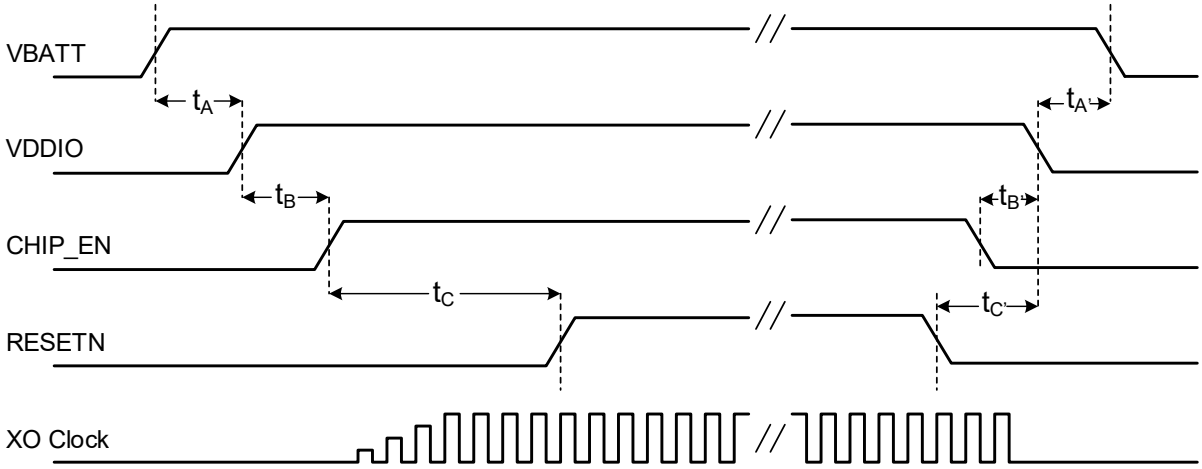
If a voltage must be applied to the signal pads while the chip is in a low-power state, the VDDIO supply must be on so the SLEEP or Power_Down state can be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below the ground to any pin.

7.3 Power Up/Power Down Sequence

The power up and power down sequence for ATWINC15x0B is shown in the following figure.

Figure 7-2. ATWINC15x0B Power Up/Down Sequence



The following table lists the parameters for the timing.

Table 7-2. ATWINC15x0B Power Up/Power Down Sequence

Symbol	Min.	Max.	Unit	Description	Condition
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5			CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0			VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0			CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0			RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

7.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents digital I/O pin states corresponding to the device power modes.

Table 7-3. ATWINC15x0B Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input driver	Pull-Up/Down Resistor (1)
Power_Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled

.....continued

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input driver	Pull-Up/Down Resistor (1)
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

Note:

1. The pull-up/pull-down resistor value used is 96 kΩ ±10%.

7.5 Chip Reset

If a chip reset is performed on the ATWINC15x0B, the RESETN signal must be pulsed low for a minimum of 1 µs to reset the device successfully.

8. Electrical Specifications

8.1 Absolute Maximum Ratings

The values listed in this section are the ratings that can be peaked by the device, but not sustained without causing irreparable damage to the device.

Table 8-1. ATWINC15x0B Absolute Maximum Ratings

Characteristic	Symbol	Min.	Max.	Unit
Core supply voltage	V_{DDC}	-0.3	1.5	V
I/O supply voltage	V_{DDIO}	-0.3	5.0	
Battery supply voltage	V_{BATT}	-0.3	5.0	
Digital input voltage	V_{IN}(1)	-0.3	VDDIO	
Analog input voltage	V_{AIN} (2)	-0.3	1.5	
ESD Human Body Model	V_{ESDHBM}(3)	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
Storage Temperature	TA	-40	125	ºC
Junction Temperature	—	—	125	
RF input power max	—	—	23	dBm

Notes:

1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG, VDD_VCO.
3. For V_{ESDHBM}, each pin is classified as Class 1, Class 2 or both:
   - The Class 1 pins include all the pins (both analog and digital).
   - The Class 2 pins are all digital pins only.
   - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins.

⚠ CAUTION Stresses listed in the above table may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

8.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for ATWINC15x0B.

Table 8-2. ATWINC15x0B Recommended Operating Conditions(3)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
I/O supply voltage	VDDIO(1)	2.7	3.3	3.6	V
Battery supply voltage	VBATT(2)	3.0	3.3	4.2	V
Operating temperature	—	-40	25	85	ºC

Notes:

1. I/O supply voltage is applied to VDDIO_A and VDDIO pins.
2. Battery supply voltage is applied to VDD_BATT_PPA, VDD_BATT_PA and VBATT_BUCK pins.
3. For more details on power connections, refer to 7. Power Management and Table 8.3.

8.3 DC Electrical Characteristics

The following table provides the DC characteristics for the ATWINC15x0B digital pads.

Table 8-3. ATWINC15x0B Electrical Characteristics

Characteristic	Min.	Typ.	Max.	Unit
Input low voltage (V_{IL})	-0.30	—	0.65	V
Input high voltage (V_{IH})	VDDIO-0.60	—	VDDIO+0.30	
Output low voltage (V_{OL})	—	—	0.45	
Output high voltage (V_{OH})	VDDIO-0.50	—	—	
Output loading	—	—	20	pF
Digital input load	—	—	6	
Pad drive strength (regular pads(1))	8	13.5	—	mA
Pad drive strength (high-drive pads(1))	16	27	—	

Note:

1. The I2C_SCL and I2C_SDA are high-drive pads and all other pads are regular.

8.4 Current Consumption in Various Device States

The following table provides the current consumption of ATWINC15x0B in various device states.

Table 8-4. ATWINC15x0B Current Consumption

Device State	Code Rate	Output Power, dBm	Current Consumption (1)	
			IVBATT	IVDDIO
ON_Transmit	802.11b 1 Mbps	17.5	268 mA	22 mA
	802.11b 11 Mbps	18.5	264 mA	22 mA
	802.11g 6 Mbps	17.5	269 mA	22 mA
	802.11g 54 Mbps	16.0	266 mA	22 mA
	802.11n MCS 0	17.0	268 mA	22 mA
	802.11n MCS 7	14.5	265 mA	22 mA
ON_Receive	802.11b 1 Mbps	N/A	61 mA	22 mA
	802.11b 11 Mbps	N/A	61 mA	22 mA
	802.11g 6 Mbps	N/A	61 mA	22 mA
	802.11g 54 Mbps	N/A	61 mA	22 mA
	802.11n MCS 0	N/A	61 mA	22 mA
	802.11n MCS 7	N/A	61 mA	22 mA

.....continued

Device State	Code Rate	Output Power, dBm	Current Consumption (1)	
			IVBATT	IVDDIO
ON_Doze	N/A	N/A	380 µA	<10 µA
Power_Down	N/A	N/A	<0.5 µA	<3.5 µA

Note:

1. Conditions: VBATT =3.3V, VDDIO=3.3V and at 25°C

8.5 Wi-Fi Performance Characteristics

8.5.1 Receiver Performance

The following table shows the typical Receiver performance for the ATWINC15x0B.

Table 8-5. ATWINC15x0B Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,412	—	2,484	MHz
Sensitivity 802.11b (8% PER)	1 Mbps DSS	—	-95	—	dBm
	2 Mbps DSS	—	-90	—	
	5.5 Mbps DSS	—	-92	—	
	11 Mbps DSS	—	-86	—	
Sensitivity 802.11g (10% PER)	6 Mbps OFDM	—	-90	—	dBm
	9 Mbps OFDM	—	-89	—	
	12 Mbps OFDM	—	-88	—	
	18 Mbps OFDM	—	-85	—	
	24 Mbps OFDM	—	-83	—	
	36 Mbps OFDM	—	-80	—	
	48 Mbps OFDM	—	-76	—	
	54 Mbps OFDM	—	-74	—	
Sensitivity 802.11n (10% PER) (BW=20 MHz)	MCS 0	—	-89	—	dBm
	MCS 1	—	-87	—	
	MCS 2	—	-85	—	
	MCS 3	—	-82	—	
	MCS 4	—	-77	—	
	MCS 5	—	-74	—	
	MCS 6	—	-72	—	
	MCS 7	—	-70.5	—	

.....continued

Parameter	Description	Min.	Typ.	Max.	Unit
Maximum receive signal level	1-11 Mbps DSS	—	0	—	dBm
	6-54 Mbps OFDM	—	0	—	
	MCS 0 – 7	—	0	—	
Adjacent channel rejection	1 Mbps DSS (30 MHz offset)	—	50	—	dB
	11 Mbps DSS (25 MHz offset)	—	43	—	
	6 Mbps OFDM (25 MHz offset)	—	40	—	
	54 Mbps OFDM (25 MHz offset)	—	25	—	
	MCS 0 – 20 MHz BW (25 MHz offset)	—	40	—	
	MCS 7 – 20 MHz BW (25 MHz offset)	—	20	—	
Cellular blocker immunity	776-794 MHz CDMA	—	-14	—	dBm
	824-849 MHz GSM	—	-10	—	
	880-915 MHz GSM	—	-10	—	
	1710-1785 MHz GSM	—	-15	—	
	1850-1910 MHz GSM	—	-15	—	
	1850-1910 MHz WCDMA	—	-24	—	
	1920-1980 MHz WCDMA	—	-24	—	

8.5.2 Transmitter Performance

The following table explains the ATWINC15x0B Transmitter performance.

Table 8-6. ATWINC15x0B Transmitter Performance *(1, 4)*

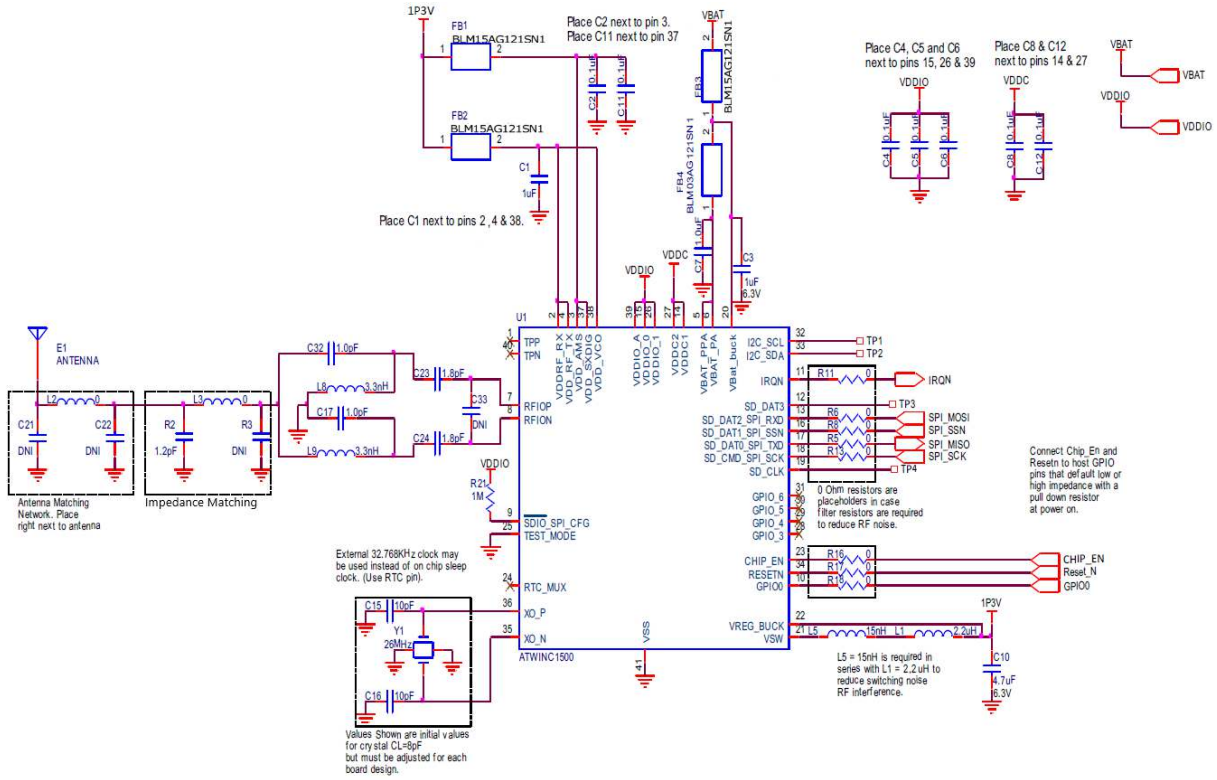
Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,412	—	2,484	MHz
Output power (1, 2, 3) ON_Transmit	802.11b 1 Mbps	—	13.6	—	dBm/MHz
	802.11b 11 Mbps	—	15.3	—	
	802.11g 6 Mbps	—	18.9	—	
	802.11g 54 Mbps	—	14.3	—	
	802.11n MCS 0	—	18.9	—	
	802.11n MCS 7	—	12.2	—	
TX power accuracy	—	—	±1.5 (3)	—	dB
Carrier suppression	—	—	30.0	—	dBc
Harmonic output power	2nd	—	—	-41	dBm/MHz
	3rd	—	—	-41	

Notes:

1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured at balun output.
3. Operating temperature range is -40°C to +85°C. RF performance is assured at room temperature of 25°C with a 2-3 dB change at boundary conditions.
4. The availability of some specific channels and/or operational frequency bands are country dependent and must be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.

9. Reference Design

Figure 9-1. ATWINC15x0B Reference Schematic Design (1, 2)



Notes:

1. Add test points for I2C_SCL (32) and I2C_SDA (33) pins.
2. Add test points for UART TxD (12) and RxD (19) pins.
3. Add a 10 µF and 0.01 µF decoupling capacitor to 1P3V net. Refer to 10.1.3 Power Management Unit for layout guidelines.

9.1 Bill of Material

Table 9-1. Bill of Material

Item	Qty	Reference	Value	Description	Manufacturer	Part Number
1	2	C1, C3	1.0 µF	CAP, CER, 1.0 µF, 20%, X5R, 0402, 6.3V	Panasonic	ECJ-0EB0J105M
2	7	C2, C4, C5, C6, C8, C11, C12	0.1 µF	CAP, CER, 0.1 µF, 10%, X5R, 0402, 10V	AVX	0402ZD104KAT2A
3	1	C10	4.7 µF	CAP, CER, 4.7 µF, 4V, 20%, X5R, 0402	Murata	GRM155R60G475ME47D
4	2	C17, C32	1 pF	CAP, CER, 1 pF, 50V, NP0, 0201	Murata	GRM0335C1H1R0CA01D

.....continued

Item	Qty	Reference	Value	Description	Manufacturer	Part Number
5	2	C15, C16	10 pF	CAP, CER, 10PF, 50V, 1%, NP0, 0402	Murata	GRM1555C1H100FA01D
6	2	C23, C24	1.8 pF	CAP, CER, 1.8 pF, 50V, NP0, 0201	Murata	GRM0335C1H1R8CA01D
7	1	R2	1.2 pF	CAP, CER, 1.2PF, 50V, NP0, 0201	Murata	GRM0335C1H1R2CA01D
8	—	C21, C22, C33, R3	DNI	—	—	—
9	1	C7	1.0 µF	CAP, CER, 1 µF, 4V, 20%, X6S, 0201	Murata	GRM033C80G105MEA2D
10	3	FB1, FB2, FB3	BLM15AG121SN1	FERRITE, 120Ω @100 MHz, 0402	Murata	BLM15AG121SN1
11	1	FB4	BLM03AG121SN1D	FERRITE BEAD, 120Ω, 200 MA, 0201	Murata	BLM03AG121SN1D
12	1	L1	2.2 µH	POWER INDUCTOR, 2.2 µH, 20%, 750 mA, 0.3Ω, 0603	Murata	LQM18PN2R2MFRL
13	1	L5	15 nH	INDUCTOR, 15 nH, 300 MA, 0402	Murata	LQG15HS15NJ02D
15	2	L8, L9	3.3 nH	INDUCTOR, 3.3+/-0.2 nH, 750 MA, 0201	Murata	LQP03TN3N3C02D
16	10	R5, R6, R8, R11, R13, R16, R17, R18, L2, L3	0R	RESISTOR, Thick Film, 0Ω, 0201	Panasonic	ERJ-1GN0R00C
17	1	R21	1 Mohm	RESISTOR, Thick Film, 1 MΩ, 0402	Yageo	RC0100FR-071ML
18	4	TP1, TP2, TP3, TP4	Test point	—	—	—
19	1	U1	ATWINC1500B-MU-T	IC, WiFi, 40QFN	Microchip	ATWINC1510B-MU-T
20	1	Y1	26.000 MHz	CRYSTAL, 26 MHz, 10 pF, SMD	Abracon	ABM10-26.000MHZ-D30-T3
21	1	E1	Antenna	2.4 GHz Antenna	—	—

10. Design Consideration

This chapter provides the guidelines on placement and routing to achieve the best performance.

10.1 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board must have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3x3 grid of vias.
- To avoid electromagnetic field blocking, keep any large metal objects as far away from the antenna as possible.
- Do not enclose the antenna within a metal shield.
- Keep noise-radiating components or signals, within the 2.4 GHz to 2.5 GHz frequency band, away from the antenna and shield those components if possible. Any noise radiated from the host board in this frequency band degrades the sensitivity of the chip.

10.1.1 Power and Ground

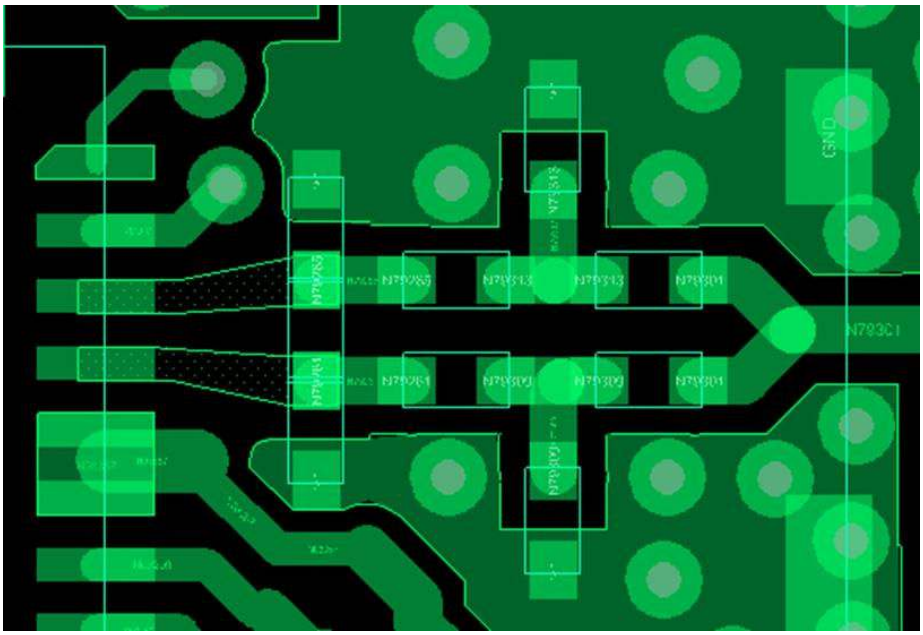
- Dedicate the layer immediately below the layer containing the RF traces from the ATWINC15x0B for the ground. Ensure that this ground plane does not get broken up by routes.
- Power traces can be routed on all layers except the ground layer.
- Power supply routes must be heavy copper fill planes to ensure low inductance.
- The power pins of the ATWINC15x0B must have a via directly to the power plane, close to the power pin.
- Decoupling capacitors must have a via next to the capacitor pin and this via must be directly connected to the power plane and avoid a long trace for this connection.
- The ground pad of the decoupling capacitor must have a via directly connected to the ground plane.
- Each decoupling capacitor must have its own via directly connected to the ground plane and directly connected to the power plane next to the pad.
- The decoupling capacitors must be placed as close as possible to the pin that it is filtering.

10.1.2 RF Traces and Components

The RF trace from RFIOP (Pin #7) and RFION (Pin #8) of the ATWINC15x0B to the balun must be 50Ω differential controlled impedance. The route from the balun to the antenna connector must be a 50Ω controlled impedance trace. This trace must be routed in reference to the ground plane. This ground reference plane must extend entirely under the ATWINC15x0B QFN package and to the sides of the these routes.

- Determine the available PCB stack-ups and the trace dimensions to achieve 50Ω single-ended controlled impedance.
- Do not have any signal traces below/adjacent to the RF trace in the PCB.
- Ensure that the RF traces from ATWINC15x0B to the antenna is as short as possible to reduce path losses and to mitigate the trace from picking-up noise.
- Place guard ground vias on either side of the RF trace running from device to the antenna feed point in the PCB.
- Do not use thermal relief pads for the ground pads of all components in the RF path. These component pads must be completely filled with GND copper polygon. Place individual vias to the GND pads of these components.
- It is recommended to have a 3x3 grid of ground vias solidly connecting the exposed ground paddle of the ATWINC15x0B to the ground plane on the inner/other layers of the PCB. This acts as a good ground and thermal conduction path for the ATWINC15x0B.
- Ensure that all digital signals that may be toggling while the ATWINC15x0B is active are placed as far away from the antenna as possible.
- Ensure that the matching components and balun are placed as close to the RFIOP and RFION pins as possible (C33, C23, C24, C17, C32, L8 and L9 in the reference schematic). The following figure shows the placement and routing of these components.

Figure 10-1. Placement and Routing of Balun and Matching Components



10.1.3 Power Management Unit

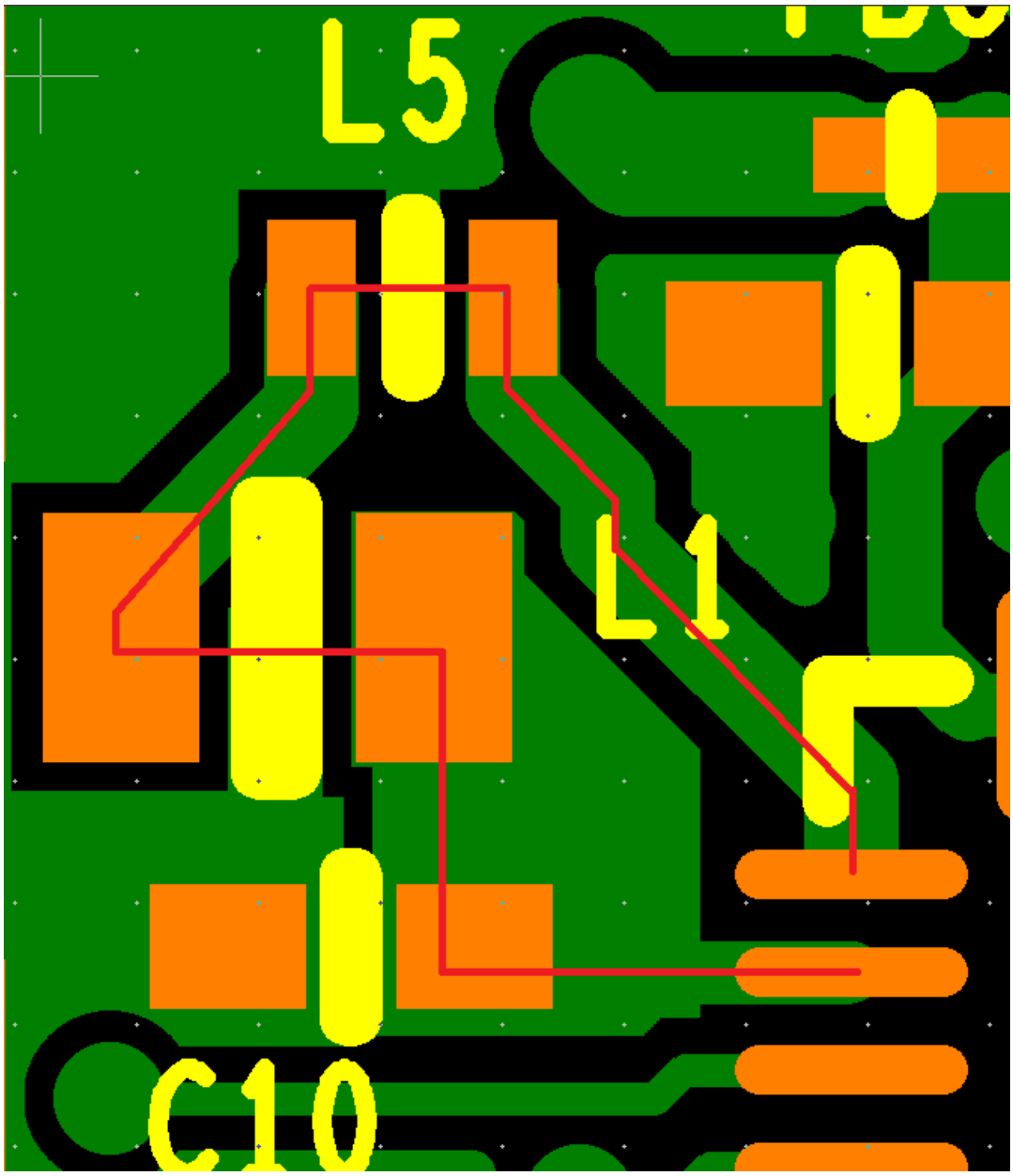
The ATWINC15x0B contains an on-chip switching regulator that regulates the V_{BAT} supply for supplying to the rest of the device. It is crucial to place and route the components associated with this circuit correctly to ensure proper operation and especially to reduce any radiated noise that can be picked up by the antenna and can severely reduce the receiver sensitivity. The external components for the PMU consist of two inductors, L5 = 15 nH and L1 = 2.2 µH, and a capacitor, C10 = 4.7 µF. These components must be placed as close as possible to the ATWINC15x0B pin #21 (VSW).

The trace loop from the VSW pin to the VREG_BUCK pin through the components, inductors L5 and L1 and, then, followed by a capacitor, C10, must be as short as possible.

Add a via between C10 and VREG_BUCK to trace out the 1P3V power rail for adding additional capacitors, 10 uF and 0.01 uF, and further route the trace to power the subsystems VDD_VCO, VDD_RF_RX, VDD_RF_TX, VDD_AMS and VDD_SXDIG.

The smaller inductor, L5, must be placed closest to pin #21 (VSW). Current flows from pin #21 (VSW) through L5, then L1, then through C10 to the ground and back to the center ground paddle of the ATWINC15x0B package. Place the components so that the current loop is as small as possible. Ensure that there is a ground via to the inner ground plane right next to the ground pin of C10. The ground return path must be extremely low inductance. Failure to provide a short, heavy ground return between the capacitor and the ATWINC15x0B ground pad results in incorrect operation of the on-chip switching regulator. The following figure shows an example placement and routing of these components. The trace that creates the loop is highlighted in red.

Figure 10-2. Placement and Routing of PMU Components

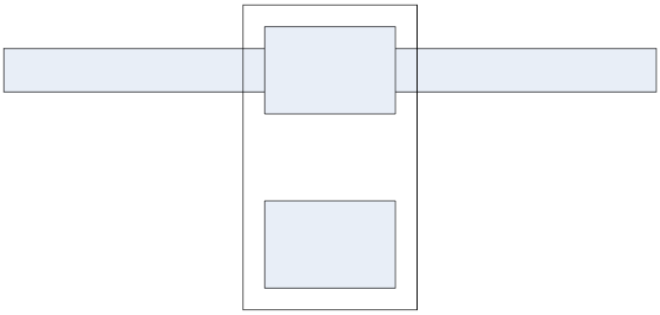


10.1.4 Additional Suggestions

Ensure that the route traces directly through the pads of all the filter capacitors and not by a stub route.

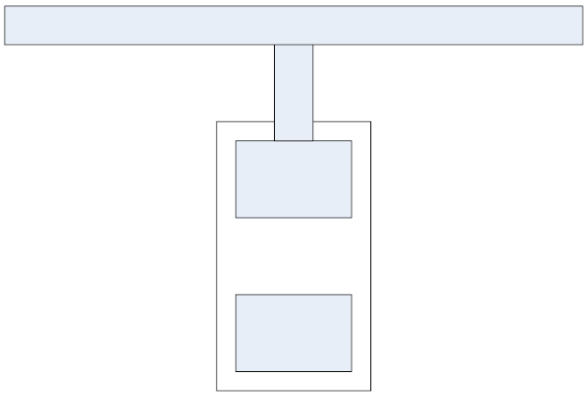
The following figure shows the correct way to route through a capacitor pad.

Figure 10-3. Correct Routing Through Capacitor Pad



The following figure shows a stub route to the capacitor pad. This must be avoided, as it adds additional impedance in series with the capacitor.

Figure 10-4. Incorrect Stub Route To Capacitor Pad



10.1.5 Ground

The following are the guidelines for ground vias:

- The center ground pad of the device must be solidly connected to the ground plane by using a 3x3 grid of vias.
- Ground vias must surround the perimeter of the pad.
- One of these ground vias must be placed in the center pad as close as possible to pins #7 (RFIOP) and #8 (RFION).
- The ground via serves as the RF ground return path.
- A ground via must be placed in the center pad and closer to the #21 (VSW) pin.
- This acts as a ground return path for the PMU.

10.2 Sensitive Traces

This section describes the guidelines for sensitive traces and signals.

10.2.1 Signals

The following signals are very sensitive to noise and they must be kept as short as possible and kept isolated from all other signals by routing them far away from other traces or by using a ground to shield them. Also, isolate these signals from the noisy traces on the layers above and below them:

- XO_N
- XO_P
- RFIOP
- RFION

10.2.2 Supplies

The following power supply pins for the ATWINC15x0B are sensitive to noise, so the routes to these pins must be isolated from other noisy signals both on the same layer as the route and on the layers above and below. Use a ground between these sensitive signals to isolate them from other signals. It is important that the decoupling capacitors for these supplies are placed as close to the ATWINC15x0B pin as possible. This reduces the trace inductance between the capacitor and the ATWINC15x0B power pin to an absolute minimum:

- VDDRF_RX (pin #2)
- VDDRF_TX (pin #4)
- VDD_AMS (pin #3)
- VDD_SXDIG (pin #37)
- VDD_VCO (pin #38)

Additionally, while the VDDC (pin #14 and 27) and VBAT_BUCK (pin #20) supplies are not sensitive to picking up noise, they are noise-generating supplies. Therefore, keep the decoupling capacitors for these supply pins as close as possible to the VDDC and VBAT_BUCK pins and make sure that the routes for these supplies stay far away from sensitive pins and supplies.

10.3 Interferers

RF receiver performance is impacted due to interferers on the board that radiate noise into the antenna or coupling into the RF traces that go to the LNA input. Follow the guidelines given below to avoid the performance degradation:

- Ensure that there is no noisy circuitry placed anywhere near the antenna or the RF traces.
- All noise-generating circuits must also be shielded so they do not radiate noise that is picked up by the antenna.
- Ensure that there are no traces routed underneath the RF portion of the ATWINC15x0B.
- Ensure that there are no traces routed underneath any of the RF traces from the antenna to the ATWINC15x0B input. This applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current could flow on the ground plane and couple into the RF traces.

10.4 Antenna

The following guidelines can be used for selecting an antenna:

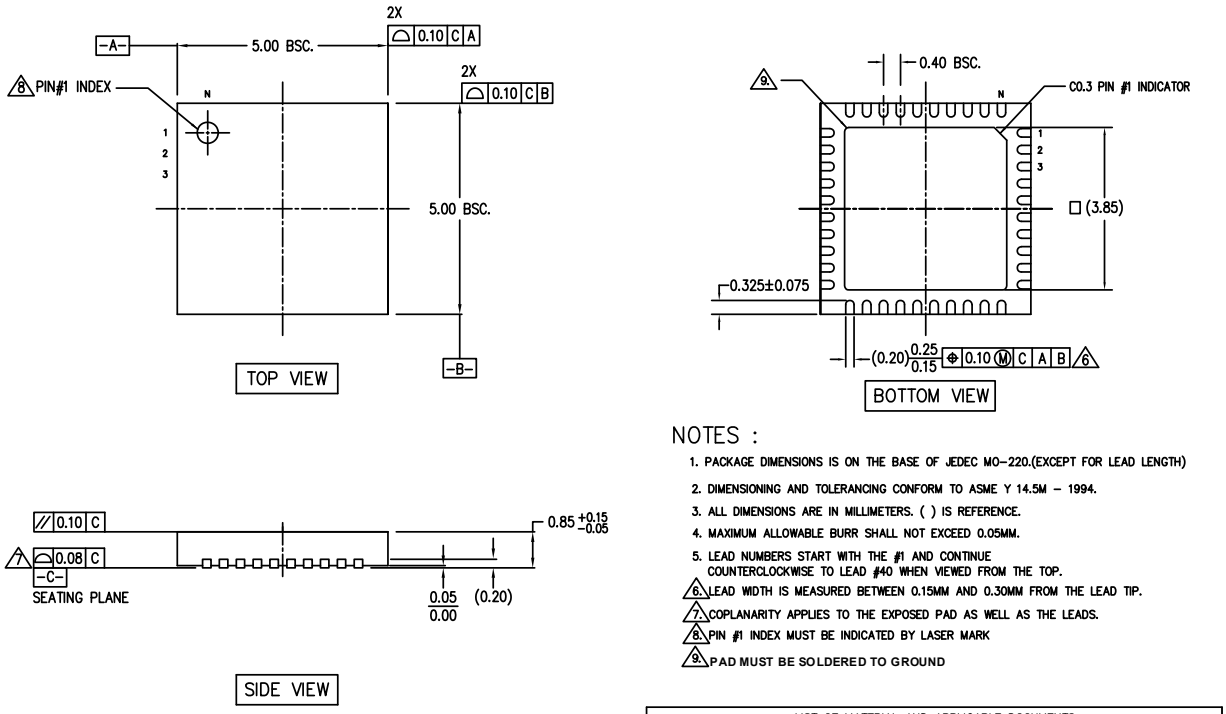
- Choose an antenna that covers the frequency band 2.400 GHz to 2.500 GHz and is designed for a 50Ω feed point.
- Follow the antenna vendor’s recommendations for pad dimensions, the spacing from the pad to the ground reference plane and the spacing from the edges of the pad to the ground fill on the same layer as the pad.
- Ensure that the antenna-matching components are placed as close as to the antenna pad as possible.

10.5 Reflow Profile Information

For information on reflow process guidelines, refer to the Solder Reflow Recommendation Application Note (DS00233).

11. Package Outline Drawing

Figure 11-1. ATWINC15x0B QFN Package Outline Drawing



NOTES :

1. PACKAGE DIMENSIONS IS ON THE BASE OF JEDEC MO-220.(EXCEPT FOR LEAD LENGTH)
2. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y 14.5M – 1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ( ) IS REFERENCE.
4. MAXIMUM ALLOWABLE BURR SHALL NOT EXCEED 0.05MM.
5. LEAD NUMBERS START WITH THE #1 AND CONTINUE COUNTERCLOCKWISE TO LEAD #40 WHEN VIEWED FROM THE TOP.
6. LEAD WIDTH IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE LEAD TIP.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.
8. PIN #1 INDEX MUST BE INDICATED BY LASER MARK
9. PAD MUST BE SOLDERED TO GROUND

LIST OF MATERIAL AND APPLICABLE DOCUMENTS			
SCALE: NONE	DATE: 02/28/13		TITLE: VQFN SAW 5 X 5 MM, 40 LEAD 3.85X3.85 EEP SIZE PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS		
PROJECTION UNLESS SPECIFIED	FRAC: .XX ±0.10 .XXX ±0.05 .XXXX ±0.03 ANGLE ±1°		

12. Reference Documentation

The following table provides the set of collateral documents to ease integration and device ramp.

Table 12-1. Reference Documents

Title	Content
Platform Getting Started Guide	Details how to evaluate the ATWINC15x0 Network Controller Module.
Flash Memory Download Procedure	Details the download procedures of firmware, root certificate, gain table values and so on.
ATWINC1500 Wi-Fi Network Controller Software Design Guide	Integration guide with a clear description of high-level arch, an overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
Software Programming Guide (ATWINC15x0)	Details the flow chart and how to use each API to implement all generic use cases (for example, start AP, start STA, provisioning, UDP, TCP, HTTP, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note.
Solder Reflow Recommendation Application Note	For more information on Reflow process guidelines, refer to *Solder Reflow Recommendation Application Note* (DS00233D).
ATWINC15x0B/ ATWINC15x0-MR210xB Errata	This document details on the anomalies identified in the ATWINC15x0 family of devices.
ATWINC15x0B Reference Design Package	This package contains the design collaterals (schematics, Bill of Materials, PCB design source files, Gerber) of the module, evaluation boards and its associated boards for ATWINC51x0B.
ATWINC15x0 – Deriving Application Gain Table Application Note	This application note describes the Wi-Fi gain table structure and procedure to derive the application gain table. This document provides further details on the steps to update the device with the gain table.
MCHPRT2 User guide	This document provides detailed information about the MCHPRT2 tool, which allows the user to easily configure, evaluate and test an RF system.

The development-support tools and documentation are available in www.microchip.com/wwwproducts/en/ATWINC1500-IC or www.microchip.com/wwwproducts/en/ATWINC1500. For queries or help, visit support.microchip.com or contact your local Microchip sales office.

13. Document Revision History

Note: The data sheet revision is independent of the die revision (Revision bit in the Device Identification register of the Device Service Unit, DSU.DID.REVISION) and the device variant (last letter of the ordering number).

Revision	Date	Section	Changes
B	08/2020	Document	Minor updates
		2. Functional Overview	• Updated pinout descriptions for various pins and added a note in 2.3 Pinout Description • Updated Pad width in 2.4 Package Description
		3.2 Low-Power Oscillator	Added information software implementation requirement for 32.768 kHz clock
		4.3 Nonvolatile Memory (eFuse)	Updated contents and image
		5.3 Radio	• Updated frequency value from 2472 to 2484 GHz and added a note in Table 5-1 • Added a note for FW support of Short GI
		6. External Interfaces	• Added 6.1 Interfacing with the Host Microcontroller • Removed I2C Slave Interface section
		7. Power Management	Updated Figure 7-1
		8. Electrical Specifications	Modified the following sections and regrouped them under Electrical Characteristics from other chapters: • 8.4 Current Consumption in Various Device States • 8.5.1 Receiver Performance • 8.5.2 Transmitter Performance • VDDIO Absolute Maximum Specification updated
		9. Reference Design	• Updated Figure 9-1 • Updated Table 9-1
		10. Design Consideration	Added new chapter
		Table 12-1	Added new references to Errata Sheet, Reference Design Package, Deriving Application Gain Table Application Note and MCHPRT2 User Guide

.....continued

Revision	Date	Section	Changes
A	10/2018	Document	• Updated from Atmel to Microchip template. • Assigned a new Microchip document number. Previous version is Atmel 42487 revision B. • Changed document style. • Changed the name to incorporate all the ATWINC15x0B devices. • Removed references to WAPI security.
		Ordering Details	• Updated ordering code details.
		Pinout Information	• Revised Pin Assignment figure for clarity.
		Package Description	• Corrected tolerance in Package Description table. • Revised QFN Package Outline drawing to be clearer.
		Power Management	• Added footnote to Digital I/O pin Behavior in Different Device States table. • Updated RF/RMS Core Voltage in PMU Output Voltages table.
		External Interfaces	• Added SPI Pin names to SPI Interface Pin Mapping table. • Added section for Chip Reset. • Revised timing parameters in SPI Slave Timing Parameter table.
		Clocking	• Revised RTC drawing in XO connections figure.
		Radio	• Revised b Mode number in Receiver Performance table. • Revised data and footnotes in Transmit Performance table.
		Reflow Profile Information	• Removed Reflow Profile Information chapter from the datasheet.

Atmel Document Revision History
Rev. B - 03/2016

Section	Changes
Package Description	• Updated device drawing to include note to solder the paddle pad to GND in POD Figure 3-2.
Radio Transmit Performance	• Revised table in transmit performance Table 7-2.
Power Management	• Revised Chapter 9 text and current consumption table information in Table 9-2. • Removed preliminary numbers note from performance numbers Table 9-2.
Reference Design	• Updated schematic figure in Figure 10-1.
Reflow Profile Information	• Added Chapter11 Reflow Profile Information.

Rev.A- 07/2015

Section	Changes
Document	• DS update to RevB offering • Changes from WINC1500A (42353D) to WINC1500B: • Miscellaneous minor updates and corrections
Features List	• Added hardware accelerators in feature list (SSL security, IP checksum, OTA security) • Corrected Power Down and Doze mode current in Table 9-2 and in feature list
Pinout and Package Information	• Changed RTC_CLK pad definition from pull-down to pull-up
Electrical Specifications	• Corrected Table 4-3 and added high-drive pads reference in Table 3-1
WLAN Subsystem	• Increased instruction RAM size from 128KB to 160KB • Updated radio performance in Table 7-1 and Table 7-2
External Interfaces	• Fixed typos for SPI Slave interface timing in Table 8-6 • Added second UART, increased UART data rates • Updated pin mux table: added new options for various interfaces • Improved description of Coexistence interface • Changed pin list to add GPIOs 3,4,5,6 - chip pinout identical WINC and WILC • Fixed typos for SPI Slave interface timing in Table 8-6 • Fixed typos for battery supply name: changed from VBAT to VBATT • Corrected Table 8-7
Power Management	• Added VDD_VCO switch and connection in the power architecture • Updated power consumption numbers • Modified sections 9.2.1 and 9.2.2 to add high-power and low-power modes and current consumption numbers • Corrected Power Down and Doze mode current in Table 9-2 and in feature list
Reference Schematic Design	• Updated reference schematic

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