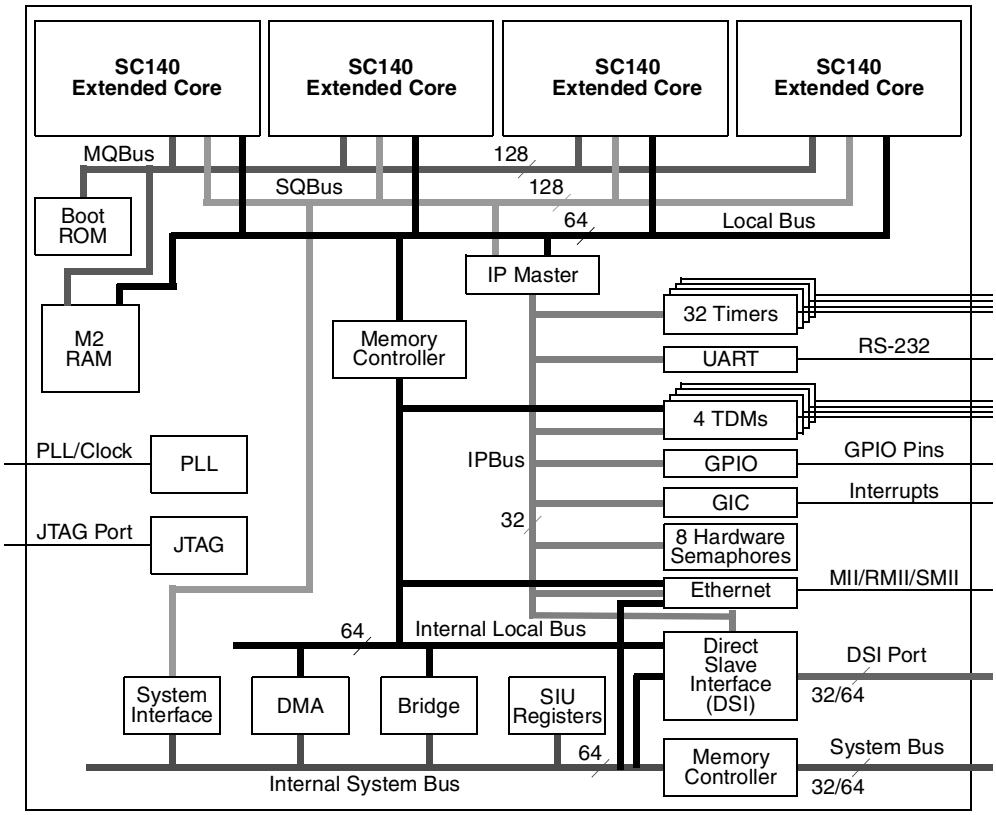
MSC8122

Quad Core 16-Bit Digital Signal Processor



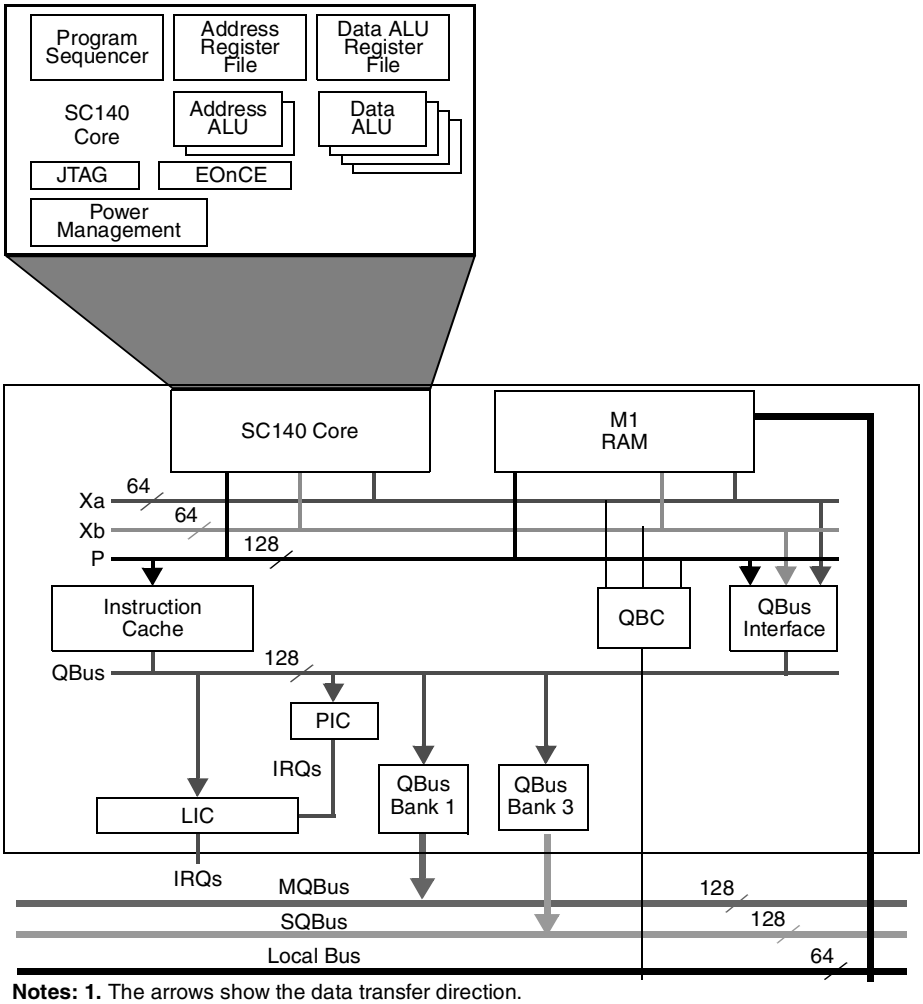
The raw processing power of this highly integrated system-on- a-chip device will enable developers to create next-generation networking products that offer tremendous channel densities while maintaining system flexibility, scalability, and upgradeability. The MSC8122 is offered in three core speed levels: 300, 400, and 500 MHz.

Figure 1. MSC8122 Block Diagram

The MSC8122 is a highly integrated system-on-a-chip that combines four SC140 extended cores with an RS-232 serial interface, four time-division multiplexed (TDM) serial interfaces, thirty-two general-purpose timers, a flexible system interface unit (SIU), an Ethernet interface, and a multi-channel DMA engine. The four extended cores can deliver a total 4800/6400/8000 DSP MMACS performance at 300/400/500 MHz.

Each core has four arithmetic logic units (ALUs), internal memory, a write buffer, and two interrupt controllers. The MSC8122 targets high-bandwidth highly computational DSP applications and is optimized for wireless transcoding and packet telephony as well as high-bandwidth base station applications. The MSC8122 delivers enhanced performance while maintaining low power dissipation and greatly reduces system cost.

Note: This document contains information on a new product. Specifications and information herein are subject to change without notice.



Notes: 1. The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. SC140 Extended Core Block Diagram

Features

Feature	Description
SC140 Cores	Four SC140 cores: • Up to 8000 MMACS using 16 ALUs running at up to 500 MHz. • A total of 1436 KB of internal SRAM (224 KB per core). Each SC140 core provides the following: • Up to 2000 MMACS using an internal 500 MHz clock. A MAC operation includes a multiply-accumulate command with the associated data move and pointer update. • 4 ALUs per SC140 core. • 16 data registers, 40 bits each. • 27 address registers, 32 bits each. • Hardware support for fractional and integer data types. • Very rich 16-bit wide orthogonal instruction set. • Up to six instructions executed in a single clock cycle. • Variable-length execution set (VLES) that can be optimized for code density and performance. • **IEEE**® Std 1149.1™ JTAG port. • Enhanced on-device emulation (EOnCE) with real-time debugging capabilities.

Feature	Description
Extended Core	Each SC140 core is embedded within an extended core that provides the following: • 224 KB M1 memory that is accessed by the SC140 core with zero wait states. • Support for atomic accesses to the M1 memory. • 16 KB instruction cache, 16 ways. • A four-entry write buffer that frees the SC140 core from waiting for a write access to finish. • External cache support by asserting the global signal (GBL) when predefined memory banks are accessed. • Programmable interrupt controller (PIC). • Local interrupt controller (LIC).
Multi-Core Shared Memories	• 475 KB M2 memory (shared memory) working at the core frequency, accessible from the local bus, and accessible from all four SC140 cores using the MQBus. • 4 KB bootstrap ROM.
M2-Accessible Multi-Core Bus (MQBus)	• A QBus protocol multi-master bus connecting the four SC140 cores to the M2 memory. • Data bus access of up to 128-bit read and up to 64-bit write. • Operation at the SC140 core frequency. • A central efficient round-robin arbiter controlling SC140 core access on the MQBus. • Atomic operation control of access to M2 memory by the four SC140 cores and the local bus.
Internal PLL	• Generates up to 500 MHz core clock and up to 166 MHz bus clocks for the 60x-compatible local and system buses and other modules. • PLL values are determined at reset based on configuration signal values.
60x-Compatible System Bus	• 64/32-bit data and 32-bit address 60x bus. • Support for multiple-master designs. • Four-beat burst transfers (eight-beat in 32-bit wide mode). • Port size of 64, 32, 16, and 8 controlled by the internal memory controller. • Bus can access external memory expansion or off-device peripherals, or it can enable an external host device to access internal resources. • Slave support, direct access by an external host to internal resources including the M1 and M2 memories. • On-device arbitration between up to four master devices.
Direct Slave Interface (DSI)	A 32/64-bit wide slave host interface that operates only as a slave device under the control of an external host processor. • 21–25 bit address, 32/64-bit data. • Direct access by an external host to internal and external resources, including the M1 and the M2 memories as well as external devices on the system bus. • Synchronous and asynchronous accesses, with burst capability in the synchronous mode. • Dual or Single strobe modes. • Write and read buffers improve host bandwidth. • Byte enable signals enables 1, 2, 4, and 8 byte write access granularity. • Sliding window mode enables access with reduced number of address pins. • Chip ID decoding enables using one $\overline{CS}$ signal for multiple DSPs. • Broadcast $\overline{CS}$ signal enables parallel write to multiple DSPs. • Big-endian, little-endian, and munged little-endian support.
3-Mode Signal Multiplexing	• 64-bit DSI, 32-bit system bus. • 32-bit DSI, 64-bit system bus. • 32-bit DSI, 32-bit system bus, and Ethernet (MII/RMII).

Feature	Description
Memory Controller	Flexible eight-bank memory controller: • Three user-programmable machines (UPMs), general-purpose chip-select machine (GPCM), and a page-mode SDRAM machine. • Glueless interface to SRAM, 166 MHz page mode SDRAM, DRAM, EPROM, Flash memory, and other user-definable peripherals. • Byte enables for either 64-bit or 32-bit bus width mode. • Eight external memory banks (banks 0–7). Two additional memory banks (banks 9, 11) control IPBus peripherals and internal memories. Each bank has the following features: — 32-bit address decoding with programmable mask. — Variable block sizes (32 KB to 4 GB). — Selectable memory controller machine. — Two types of data errors check/correction: normal odd/even parity and read-modify-write (RMW) odd/even parity for single accesses. — Write-protection capability. — Control signal generation machine selection on a per-bank basis. — Support for internal or external masters on the system bus. — Data buffer controls activated on a per-bank basis. — Atomic operation. — RMW data parity check (on system bus only). — Extensive external memory-controller/bus-slave support. — Parity byte select pin, which enables a fast, glueless connection to RMW-parity devices (on the system bus only). — Data pipeline to reduce data set-up time for synchronous devices.
Multi-Channel DMA Controller	• 16 time-multiplexed unidirectional channels. • Services up to four external peripherals. • Supports $\overline{\text{DONE}}$ or $\overline{\text{DRACK}}$ protocol on two external peripherals. • Each channel group services 16 internal requests generated by eight internal FIFOs. Each FIFO generates: — A watermark request to indicate that the FIFO contains data for the DMA to empty and write to the destination. — A hungry request to indicate that the FIFO can accept more data. • Priority-based time-multiplexing between channels using 16 internal priority levels. • Round-robin time-multiplexing between channels. • A flexible channel configuration: — All channels support all features. — All channels connect to the system bus or local bus. • Flyby transfers in which a single data access is transferred directly from the source to the destination without using a DMA FIFO.
Time-Division Multiplexing (TDM)	Up to four independent TDM modules, each with the following features: • Optional operating configurations: — Totally independent receive and transmit channels, each having one data line, one clock line, and one frame sync line. — Four data lines with one clock and one frame sync shared among the transmit and receive lines. • Glueless interface to E1/T1 framers and MVIP, SCAS, and H.110 buses. • Hardware A-law/ -law conversion. • Up to 62.5 Mbps per TDM for 400/500 MHz core operation; up to 50 Mbps per TDM for 300 MHz core. • Up to 256 channels. • Up to 16 MB per channel buffer (granularity 8 bytes), where A/ law buffer size is double (granularity 16 byte). • Receive buffers share one global write offset pointer that is written to the same offset relative to their start address. • Transmit buffers share one global read offset pointer that is read from the same offset relative to their start address. • All channels share the same word size. • Two programmable receive and two programmable transmit threshold levels with interrupt generation that can be used, for example, to implement double buffering. • Each channel can be programmed to be active or inactive. • 2-, 4-, 8-, or 16-bit channels are stored in the internal memory as 2-, 4-, 8-, or 16-bit channels, respectively. • The TDM Transmitter Sync Signal (TxTSYN) can be configured as either input or output. • Frame Sync and Data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock. • Frame sync can be programmed as active low or active high. • Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame. • MSB or LSB first support.

Feature	Description
Ethernet Controller	• Designed to comply with **IEEE** Std 802® including **IEEE** Std. 802.3™, 802.3u™, 802.3x™, and 802.3ac™. • Three Ethernet physical interfaces: — 10/100 Mbps MII. — 10/100 Mbps RMII. — 10/100 Mbps SMII. • Full and half-duplex support. • Full-duplex flow control (automatic PAUSE frame generation or software programmed PAUSE frame generation and recognition). • Support of out-of-sequence transmit queue (for initiating flow-control). • Programmable maximum frame length supports jumbo frames (up to 9.6k) and virtual local area network (VLAN) tags and priority. • Retransmission from transmit FIFO following a collision. • CRC generation and verification of inbound/outbound packets. • Address recognition: — Each exact match can be programmed to be accepted or rejected. — Broadcast address (accept/reject). — Exact match 48-bit individual (unicast) address. — Hash (256-bit hash) check of individual (unicast) addresses. — Hash (256-bit hash) check of group (multicast) addresses. — Promiscuous mode. • Pattern matching: — Up to 16 unique 4-byte patterns. — Pattern match on bit-basis. — Matching range up to 256 bytes deep into the frame. — Offsets to a maximum of 252 bytes. — Programmable pattern size in 4-byte increments up to 64 bytes. — Accept or reject frames if a match is detected. — Up to eight unicast addresses for exact matches. — Pattern matching accepts/rejects IP addresses. • Filing of receive frames based on pattern match; prioritization of frames. • Insertion with expansion or replacement for transmit frames; VLAN tag insertion. • RMON statistics. • Master DMA on the local bus for fetching descriptors and accessing the buffers. • Serial interface can be exposed either on GPIO pins or on the high ms bits of the DSI/system when the DSI and the system bus are both 32 bits. • MPC8260(PQ2) 8 byte width buffer descriptor mode as well as 32 byte width buffer descriptor mode. • MII Bridge (MIIGSK): — Programmable selection of the 50 MHz RMII reference clock source (external or internal). — Independent 2 bit wide transmit and receive data paths. — Six operating modes. — Four general-purpose control signals. — Programmable transmitted inter-frame bits to support inter-frame gap for frames in the SMII domain. • SMII features: — Multiplexed only with GPIO signals — Convey complete MII information between the PHY and MAC. — Allow direct MAC-to-MAC communication in SMII mode. — Can generate an interrupt request line while receiving inter-frame segments.

Feature	Description
UART	• Two signals for transmit data and receive data. • No clock, asynchronous mode. • Can be serviced either by the SC140 DSP cores or an external host on the system bus or the DSI. • Full-duplex operation. • Standard mark/space non-return-to-zero (NRZ) format. • 13-bit baud rate selection. • Programmable 8-bit or 9-bit data format. • Separately enabled transmitter and receiver. • Programmable transmitter output polarity. • Two receiver wake-up methods: — Idle line wake-up. — Address mark wake-up. • Separate receiver and transmitter interrupt requests. • Eight flags, the first five can generate interrupt request: — Transmitter empty. — Transmission complete. — Receiver full. — Idle receiver input. — Receiver overrun. — Noise error. — Framing error. — Parity error. • Receiver framing error detection. • Hardware parity checking. • 1/16 bit-time noise detection. • Maximum bit rate 6.25 Mbps. • Single-wire and loop operations.
General-Purpose I/O (GPIO) Port	• 32 bidirectional signal lines that either serve the peripherals or act as programmable I/O ports. • Each port can be programmed separately to serve up to two dedicated peripherals, and each port supports open-drain output mode.
I^2C Software Module	• Booting from a serial EEPROM. • Uses GPIO timing
Timers	Two modules of 16 timers each. • Cyclic or one-shot. • Input clock polarity control. • Interrupt request when counting reaches a programmed threshold. • Pulse or level interrupts. • Dynamically updated programmed threshold. • Read counter any time. Watchdog mode for the timers that connect to the device.
Hardware Semaphores	Eight coded hardware semaphores, locked by simple write access without need for read-modify-write mechanism.
Global Interrupt Controller (GIC)	• Consolidation of chip maskable interrupt and non-maskable interrupt sources and routing to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and to the cores. • Generation of 32 virtual interrupts (eight to each SC140 core) by a simple write access. • Generation of virtual $\overline{\text{NMI}}$ (one to each SC140 core) by a simple write access.
Reduced Power Dissipation	• Low power CMOS design. • Separate power supply for internal logic (1.1 or 1.2 V) and I/O (3.3 V). • Low-power standby modes. • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).
Packaging	• 0.8 mm pitch Flip-Chip Plastic Ball-Grid Array (FC-PBGA). • 431-connection (ball). • Lead-free or lead-bearing spheres. • 20 mm 20 mm.
Real-Time Operating System (RTOS)	The real-time operating system (RTOS) fully supports device architecture (multi-core, memory hierarchy, ICache, timers, DMA controller, interrupts, peripherals), as follows: • High-performance and deterministic, delivering predictive response time. • Optimized to provide low interrupt latency with high data throughput. • Preemptive and priority-based multitasking. • Fully interrupt/event driven. • Small memory footprint. • Comprehensive set of APIs.

Feature	Description
Multi-Core Support	• One instance of kernel code in all four SC140 cores. • Dynamic and static memory allocation from local memory (M1) and shared memory (M2).
Distributed System Support	Transparent inter-task communications between tasks running inside the SC140 cores and the other tasks running in on-board devices or remote network devices: • Messaging mechanism between tasks using mailboxes and semaphores. • Networking support; data transfer between tasks running inside and outside the device using networking protocols. • Integrated device drivers for such peripherals as TDM, UART, and external buses.
Software Support	• Task debugging utilities integrated with compilers and vendors. • Board support package (BSP) for the application development system (ADS). • Integrated development environment (IDE): — C/C++ compiler with in-line assembly so developers can generate highly optimized DSP code. Translates C/C++ code into parallel fetch sets and maintains high code density. — Librarian. User can create libraries for modularity. — A collection of C/C++ functions for developer use. — Highly efficient linker to produce executables from object code. — Seamlessly integrated real-time, non-intrusive multi-mode debugger for debugging highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. — Device simulation models enable design and simulation before hardware availability. — Profiler using a patented binary code instrumentation (BCI) technique helps developers identify program design inefficiencies. — Version control. CodeWarrior® includes plug-ins for ClearCase, Visual SourceSafe, and CVS.
Boot Options	• External memory. • External host. • UART. • TDM. • I^2C.
MSC8122ADS	• Host debug through single JTAG connector supports both processors. • MSC8103 as the MSC8122 host with both devices on the board. The MSC8103 system bus connects to the MSC8122 DSI. • Flash memory for stand-alone applications. • Communications ports: — 10/100Base-T. — 155 Mbit ATM over Optical. — T1/E1 TDM interface. — H.110. — Voice codec. — RS-232. — High-density (MICTOR) logic analyzer connectors to monitor MSC8122 signals — 6U cPCI form factor. • Emulates MSC8122 DSP farm by connecting to three other ADS boards.

Product Documentation

The documents listed in **Table 1** are required for a complete description of the MSC8122 and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back of this document.

Table 1. MSC8122 Documentation

Name	Description	Order Number
MSC8122 Technical Data	MSC8122 features list and physical, electrical, timing, and package specifications	MSC8122
MSC8122 User's Guide	User information includes system functionality, getting started, and programming topics	MSC8122UG
MSC8122 Reference Manual	Detailed functional description of the MSC8122 memory and peripheral configuration, operation, and register programming	MSC8122RM
SC140 DSP Core Reference Manual	Detailed description of the SC140 family processor core and instruction set	MNSC140CORE
Application Notes	Documents describing specific applications or optimized device operation including code examples	Refer to the MSC8122 product page.

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