

LVDS 4x4 CROSSPOINT SWITCH

FEATURES

- Signaling Rates >1.5 Gbps per Channel
- Supports Telecom/Datacom and HDTV Video Switching
- Non-Blocking Architecture Allows Each Output to be Connected to Any Input
- Compatible With ANSI TIA/EIA-644-A LVDS Standard
- 25 mV of Input Voltage Threshold Hysteresis
- Propagation Delay Times, 900 ps Typical
- Inputs Electrically Compatible With LVPECL, CML and LVDS Signal Levels
- Operates From a Single 3.3-V Supply
- Integrated 110-Ω Line Termination Resistors Available With SN65LVDT125

APPLICATIONS

- Clock Buffering / Clock Muxing
- Wireless Base Stations
- High-Speed Network Routing
- HDTV Video Switching

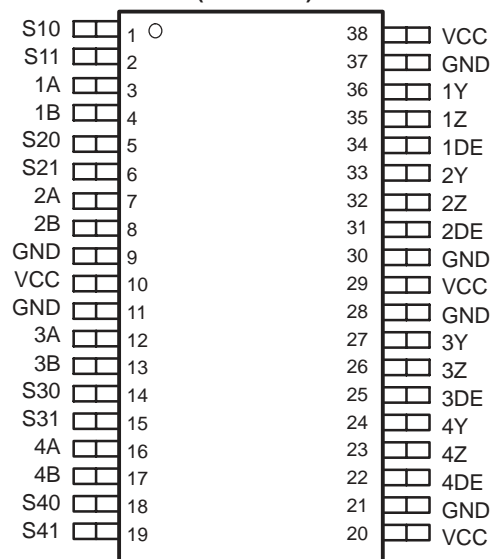
DESCRIPTION

The SN65LVDS125 and SN65LVDT125 are 4x4 nonblocking crosspoint switches. Low-voltage differential signaling (LVDS) is used to achieve signaling rates of 1.5 Gbps per channel. Each output driver includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVDT125 incorporates 110-Ω termination resistors for those applications where board space is a premium.

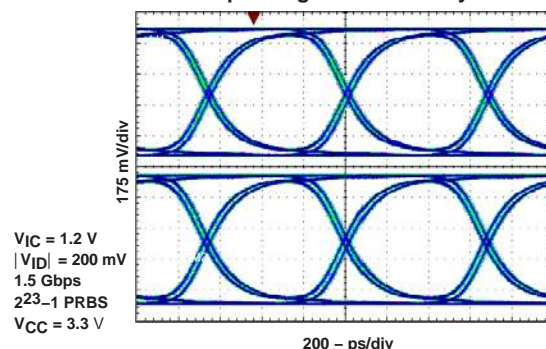
Designed to support signaling rates up to 1.5 Gbps for OC-12 clocks (622 MHz). The 1.5-Gbps signaling rate allows use in HDTV systems, including SMPTE 292 video applications requiring signaling rates of 1.485 Gbps.

The SN65LVDS125 and SN65LVDT125 are characterized for operation from –40°C to 85°C.

**SN65LVDS125DBT (Marked as LVDS125)
SN65LVDT125DBT (Marked as LVDT125)
(TOP VIEW)**



**Eye Pattern of Two Outputs
Operating Simultaneously**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

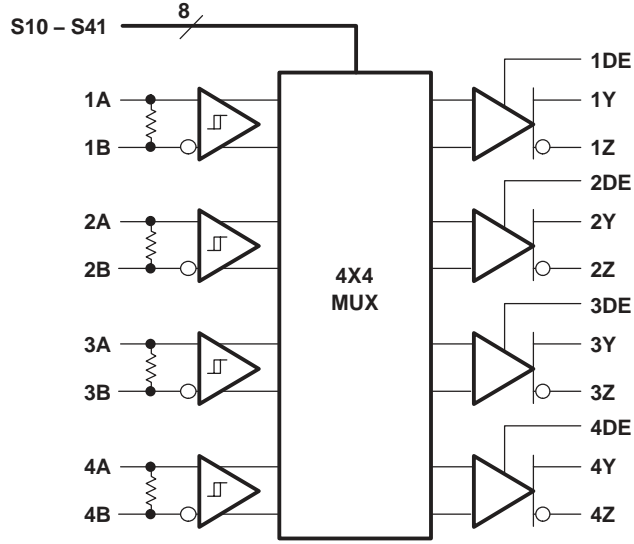
SN65LVDS125 SN65LVDT125

SLLS555C – DECEMBER 2002 – REVISED OCTOBER 2004



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

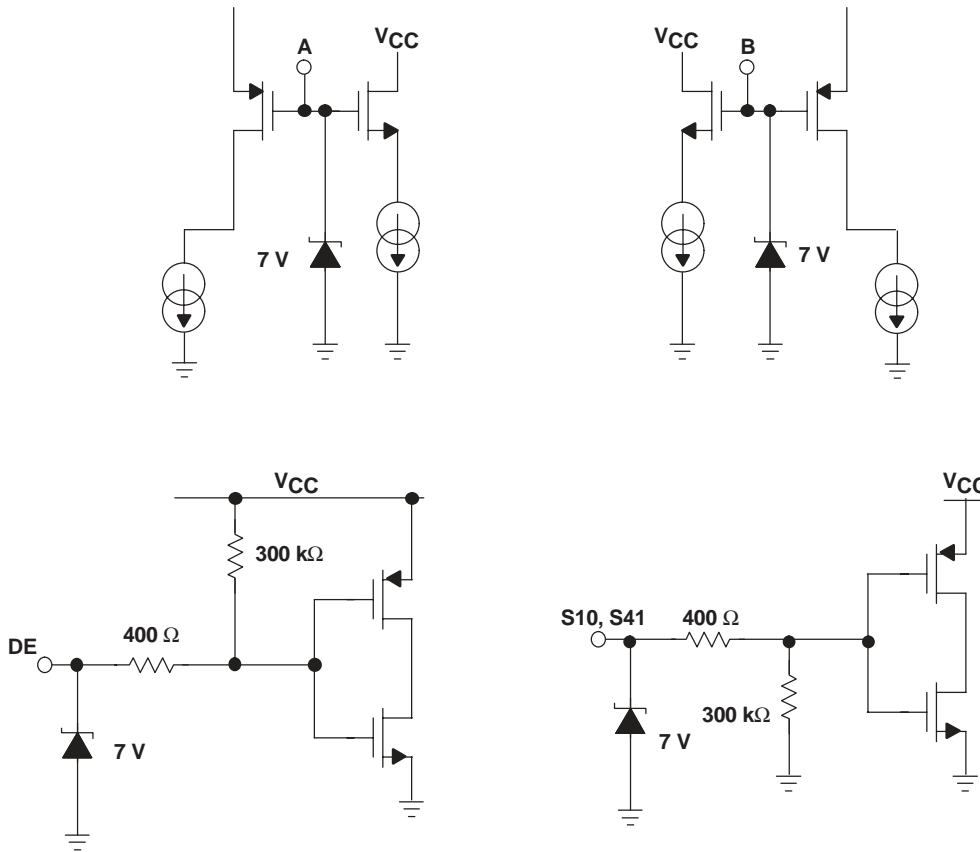
LOGIC DIAGRAM



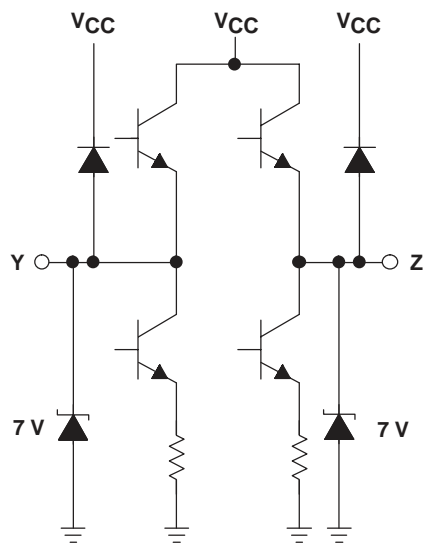
Integrated 110-Ω Termination on LVDT Only

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUT LVDS125



OUTPUT LVDS125



CROSSPOINT LOGIC TABLES

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S41	4Y/4Z
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

PACKAGE DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 85°C POWER RATING
TSSOP (DBT)	High-K ⁽²⁾	1772 mW	15.4 mW/°C	847 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) In accordance with the High-K thermal metric definitions of EIA/JESD51-6

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	VALUE	UNITS	
θ _{JB}	Junction-to-board thermal resistance		40.3	°C/W	
θ _{JC}	Junction-to-case thermal resistance		8.5		
P _D	Device power dissipation	Typical	V _{CC} = 3.3 V, T _A = 25°C, 750 MHz	356	mW
		Maximum	V _{CC} = 3.6 V, T _A = 85°C, 750 MHz	522	mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		UNITS	
Supply voltage range, V _{CC}		-0.5 V to 4 V	
Voltage range	S, DE	-0.5 V to 4 V	
	(A, B)	-0.5 V to 4 V	
	V _A - V _B (LVDT only)	1 V	
	(Y, Z)	-0.5 V to 4 V	
Electrostatic discharge	Human body model ⁽³⁾	All pins	±3 kV
	Charged-device model ⁽⁴⁾	All pins	±500 V
Continuous power dissipation		See Dissipation Rating Table	
Storage temperature range		-65°C to 150°C	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	S10–S41, 1DE–4DE	2			V
Low-level input voltage, V_{IL}	S10–S41, 1DE–4DE			0.8	V
Magnitude of differential input voltage $ V_{ID} $	LVDS	0.1			V
	LVDT	0.1		0.8	V
Input voltage (any combination of common-mode or input signals)		0		3.3	V
Junction temperature, T_J				140	°C
Operating free-air temperature, T_A (1)		–40		85	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

TIMING SPECIFICATIONS

PARAMETER		MIN	NOM	MAX	UNIT
t_{SET}	Input to select setup time		0.6		ns
t_{HOLD}	Input to select hold time		0.2		ns
t_{SWTCH}	Select to switch output		1.2	1.6	ns

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold	See Figure 1	–100			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis			25		mV
I_{IH}	High-level input current	1DE–4DE	$V_{IH} = 2\text{ V}$		–10	μA
		S10–S41		20		
I_{IL}	Low-level input current	1DE–4DE	$V_{IL} = 0.8\text{ V}$		–10	μA
		S10–S41		20		
I_I	Input current	$V_I = 0\text{ V}$ or 3.3 V , second input at 1.2 V (other input open for LVDT)	–20		20	μA
$I_{I(OFF)}$	Input current	$V_{CC} \leq 1.5\text{ V}$, $V_I = 0\text{ V}$ or 3.3 V , second input at 1.2 V (other input open for LVDT)	–20		20	μA
I_{IO}	Input offset current ($ I_{IA} - I_{IB} $) (LVDS)	$V_{IA} = V_{IB}$, $0 \leq V_{IA} \leq 3.3\text{ V}$	–6		6	μA
R_T	Termination resistance (LVDT)	$V_{ID} = 300\text{ mV}$, $V_{IC} = 0\text{ V}$ to 3.3 V	90	110	132	Ω
	Termination resistance (LVDT with power-off)	$V_{ID} = 300\text{ mV}$, $V_{IC} = 0\text{ V}$ to 3.3 V , $V_{CC} = 1.5\text{ V}$	90	110	132	
C_T	Differential input capacitance			0.6		pF

(1) All typical values are at 25°C and with a 3.3 V supply.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OD} $	Differential output voltage magnitude	See Figure 2	247	350	454	mV
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states	$V_{ID} = \pm 100$ mV	-50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{CC}	Supply current	$R_L = 100\Omega$, $C_L = 1$ pF		107	145	mA
I_{OS}	Short-circuit output current	V_{OY} or $V_{OZ} = 0$ V	-27		27	mA
I_{OSD}	Differential short circuit output current	$V_{OD} = 0$ V	-12		12	mA
I_{OZ}	High-impedance output current	$V_O = 0$ V or V_{CC}	-1		± 1	μ A
C_O	Differential output capacitance			1.2		pF

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	700	900	1200	ps
t_{PHL}	Propagation delay time, high-to-low-level output		700	900	1200	
t_r	Differential output signal rise time (20%–80%)			210	255	
t_f	Differential output signal fall time (20%–80%)			210	255	
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $) ⁽¹⁾			0	50	ps
$t_{sk(o)}$	Channel-to-channel output skew ⁽²⁾				150	ps
$t_{sk(pp)}$	Part-to-part skew ⁽³⁾				300	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽⁴⁾	750 MHz clock input ⁽⁵⁾ (see Figure 6)		0.4	3	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak) ⁽⁴⁾	750 MHz clock input ⁽⁶⁾ (see Figure 6)		4.7	13	ps
$t_{jit(pp)}$	Peak-to-peak jitter ⁽⁴⁾	1.5 Gbps $2^{23}-1$ PRBS input ⁽⁷⁾ (see Figure 6)		65	110	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak ⁽⁴⁾	1.5 Gbps 2^7-1 PRBS input ⁽⁸⁾ (see Figure 6)		56	90	ps
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 5			6	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				6	
t_{PZH}	Propagation delay, high-impedance -to-high-level output				50	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				50	

(1) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.

(2) $t_{sk(o)}$ is the maximum delay time difference between drivers over temperature, V_{CC} , and process.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) Jitter specifications are based on design and characterization. Stimulus system jitter of 1.9 ps $t_{jit(per)}$, 16 ps $t_{jit(cc)}$, 17 ps $t_{jit(pp)}$, and 7.2 ps $t_{jit(det)}$ have been subtracted from the values.

(5) Input voltage = $V_{ID} = 200$ mV, 50% duty cycle at 750 MHz, $t_r = t_f = 50$ ps (20% to 80%), measured over 1000 samples.

(6) Input voltage = $V_{ID} = 200$ mV, 50% duty cycle at 750 MHz, $t_r = t_f = 50$ ps (20% to 80%).

(7) Input voltage = $V_{ID} = 200$ mV, $2^{23}-1$ PRBS pattern at 1.5 Gbps, $t_r = t_f = 50$ ps (20% to 80%), measured over 200k samples.

(8) Input voltage = $V_{ID} = 200$ mV, 2^7-1 PRBS pattern at 1.5 Gbps, $t_r = t_f = 50$ ps (20% to 80%).

PARAMETER MEASUREMENT INFORMATION

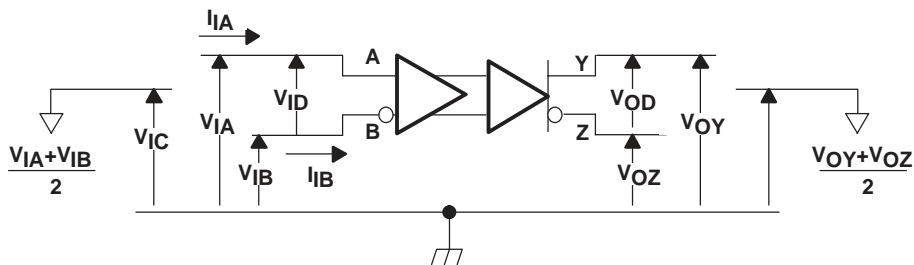


Figure 1. Voltage and Current Definitions

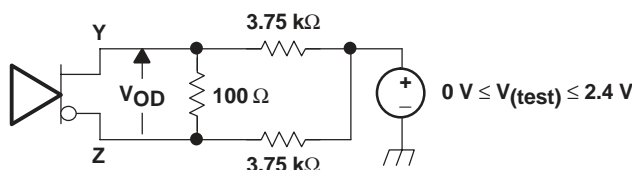
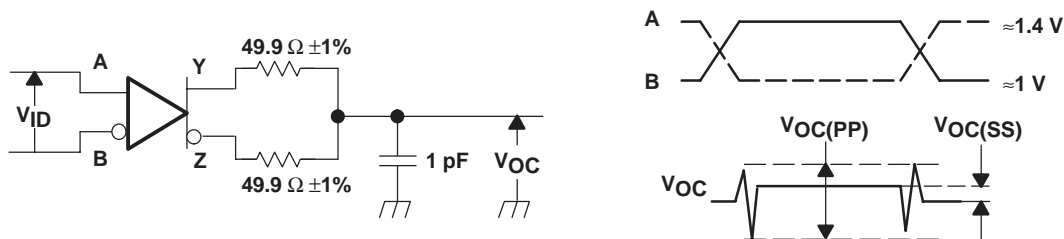
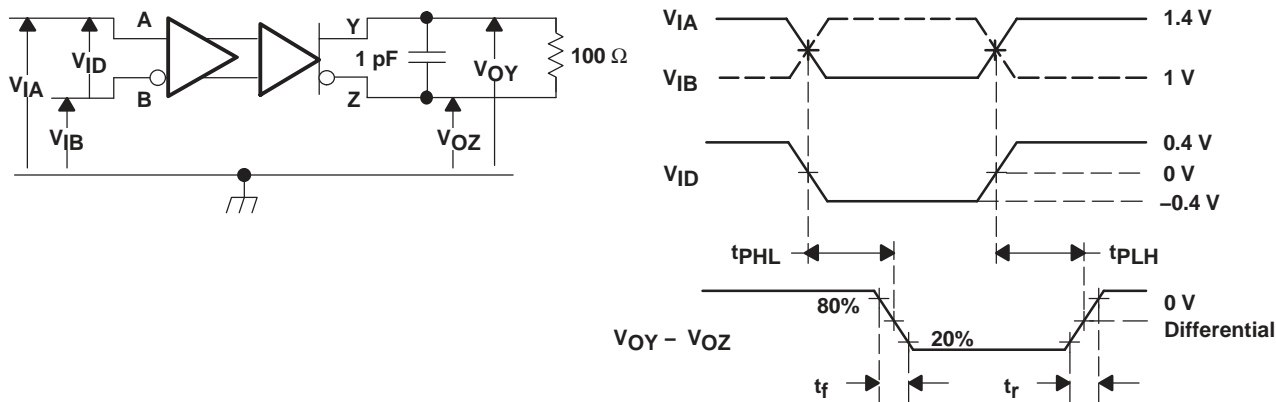


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



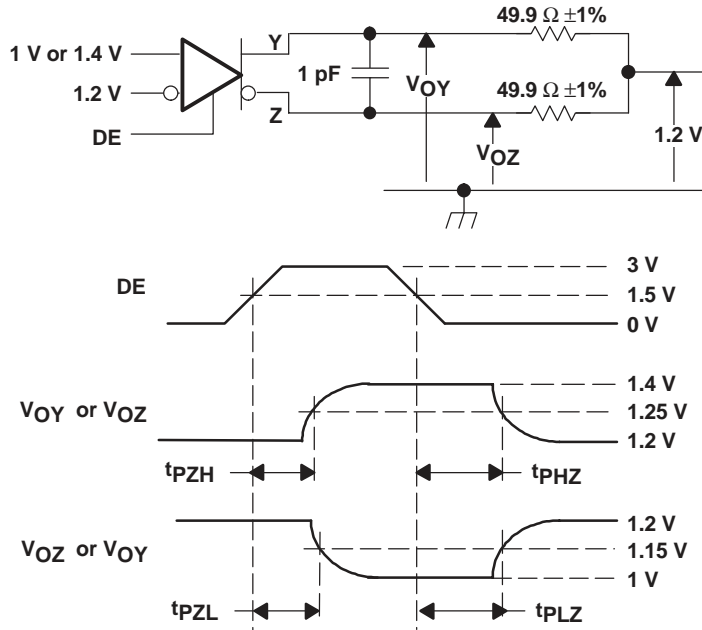
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns; $R_L = 100\Omega$; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



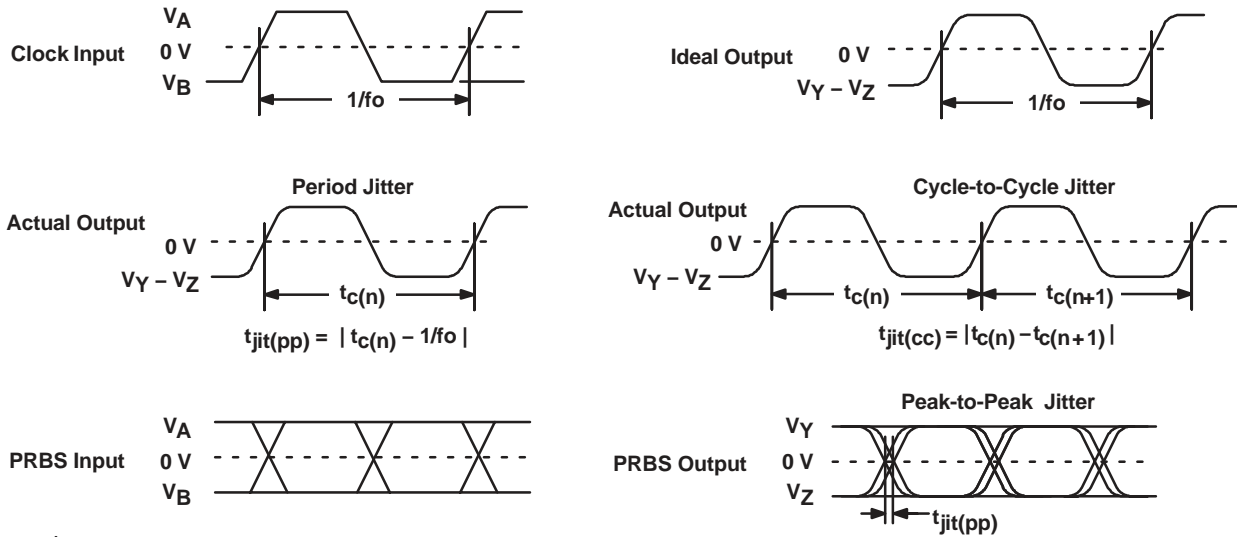
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq .25$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Timing Test Circuit and Waveforms



NOTE: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

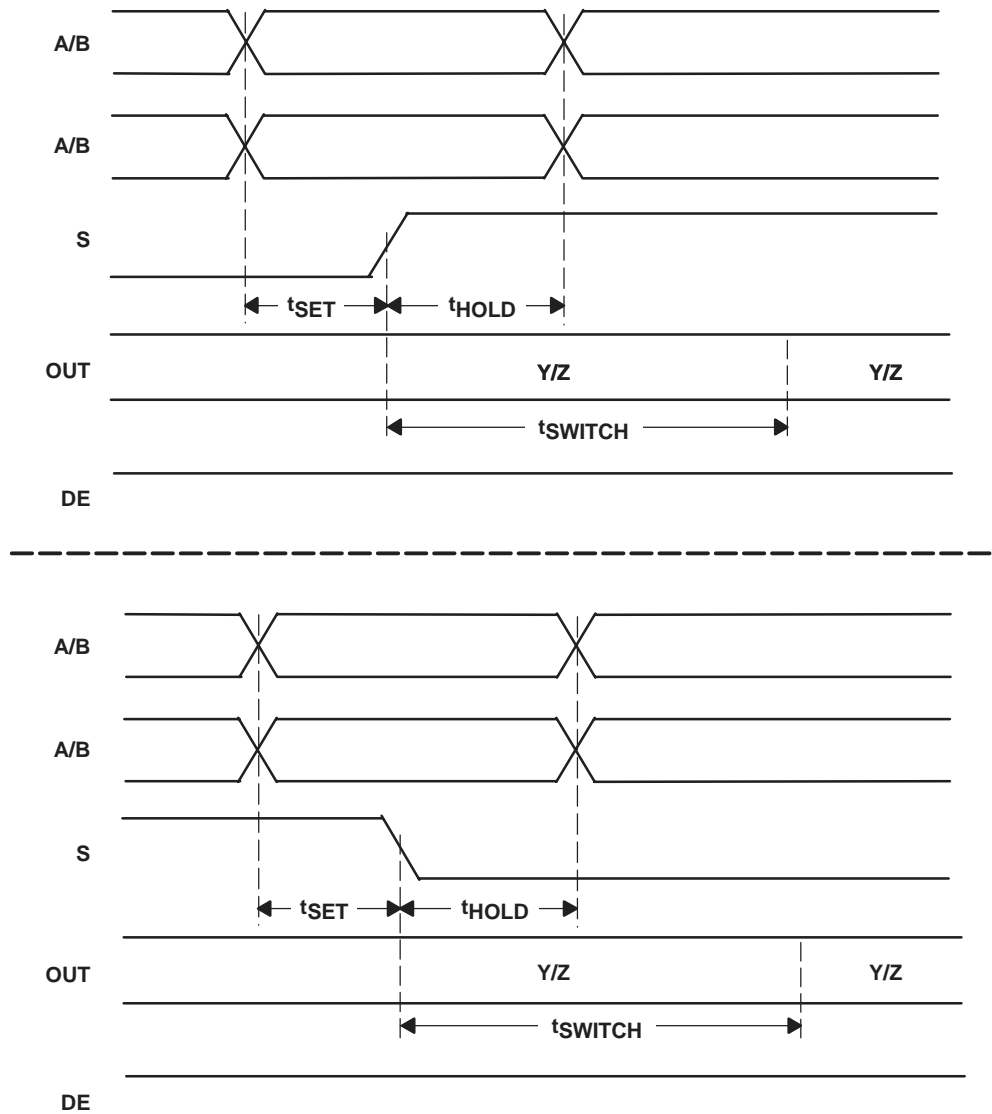
Figure 5. Enable and Disable Time Circuit and Definitions



NOTE: A. All input pulses are supplied by an Agilent 81250 Stimulus System.

NOTE: B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software.

Figure 6. Driver Jitter Measurement Waveforms



NOTE: t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 7. Input to Select for Both Rising and Falling Edge Setup and Hold Times

TYPICAL CHARACTERISTICS

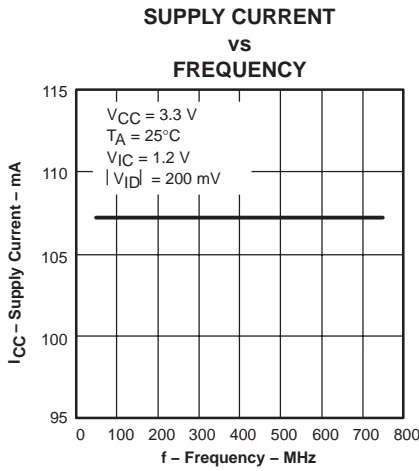


Figure 8

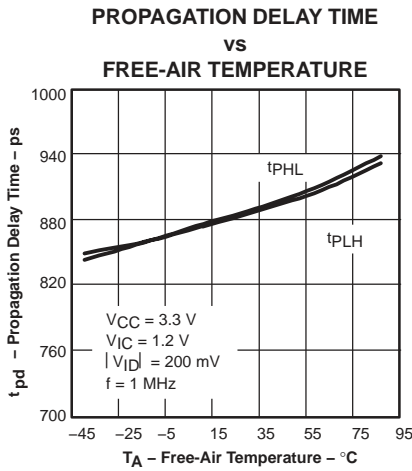


Figure 9

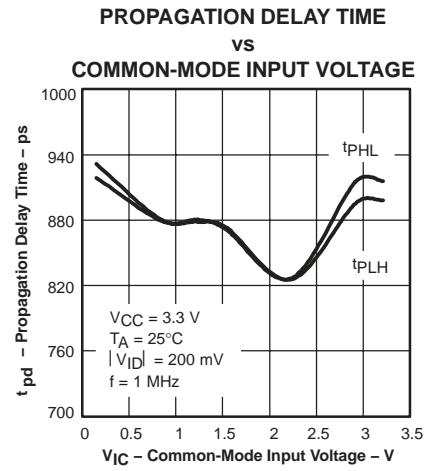


Figure 10

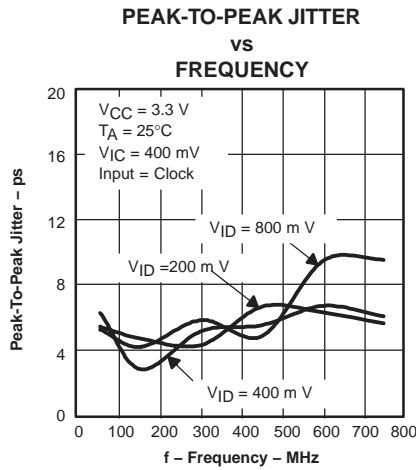


Figure 11

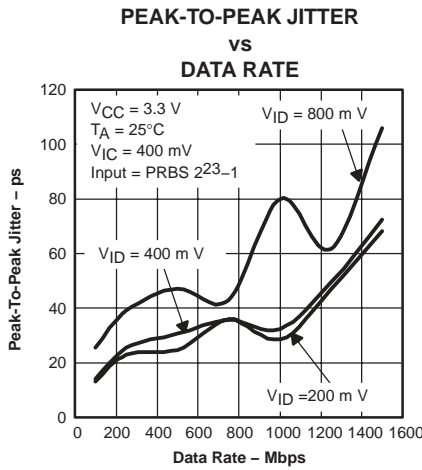


Figure 12

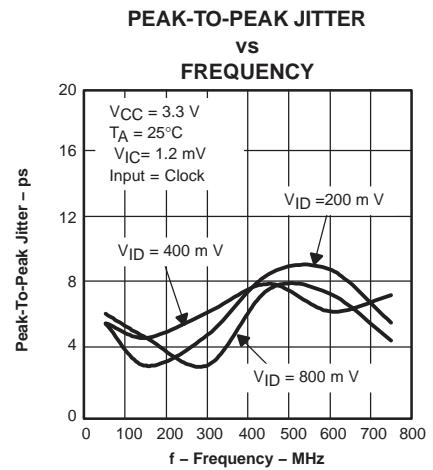


Figure 13

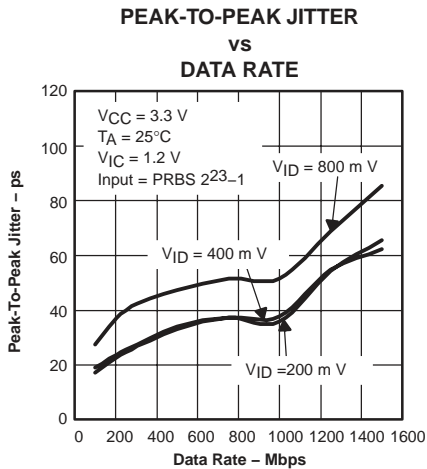


Figure 14

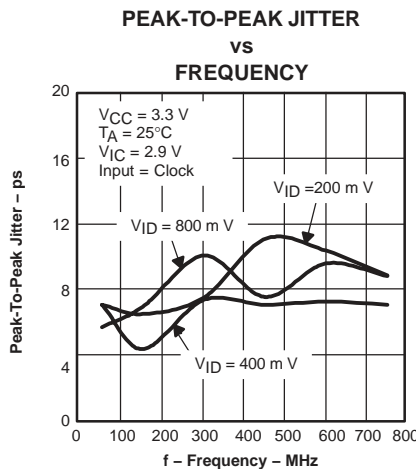


Figure 15

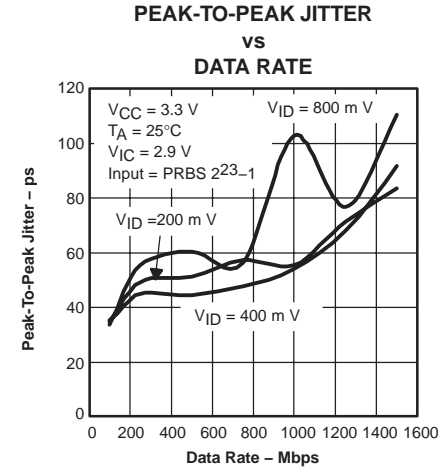


Figure 16

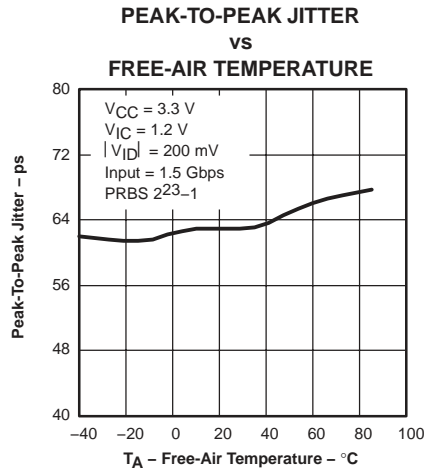


Figure 17

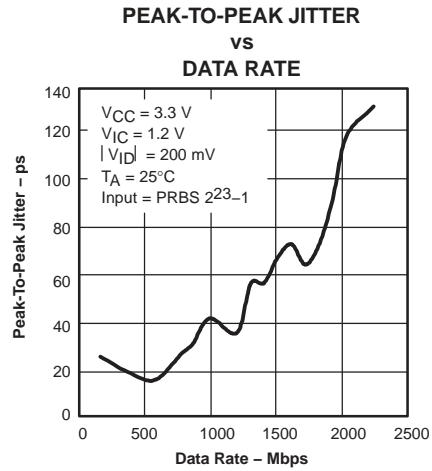


Figure 18

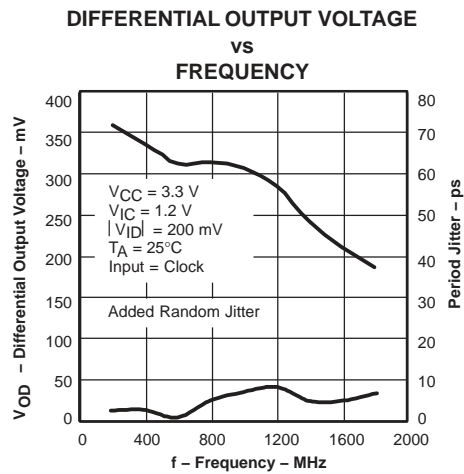
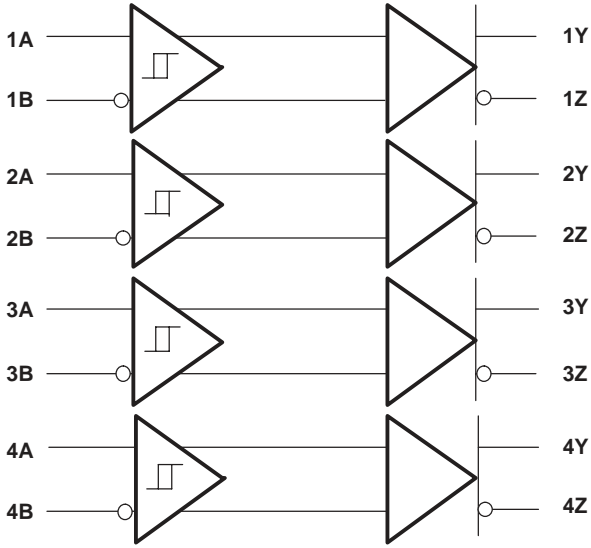


Figure 19

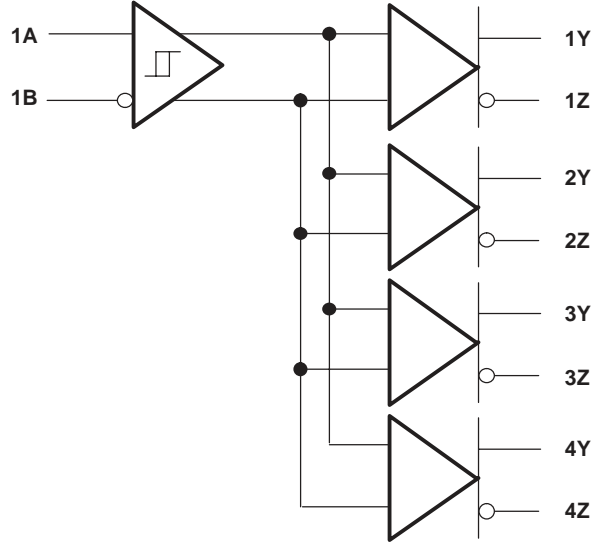
APPLICATION INFORMATION

CONFIGURATION EXAMPLES

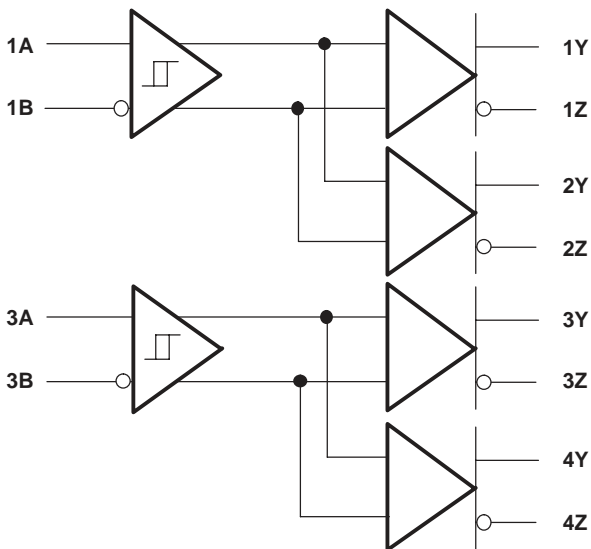
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1



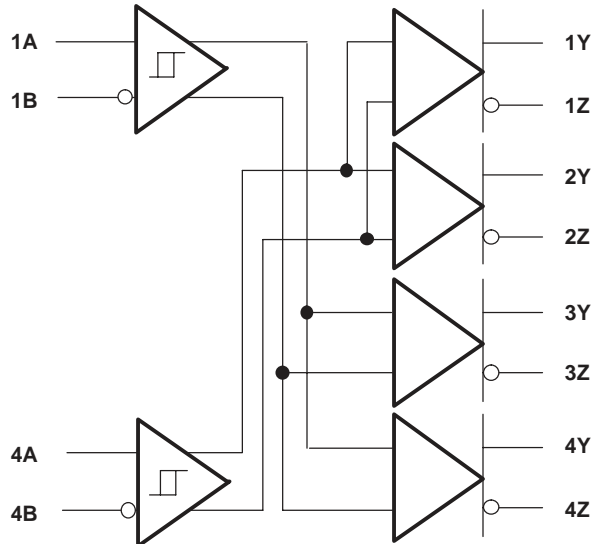
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0



S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0



APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, ETC.)

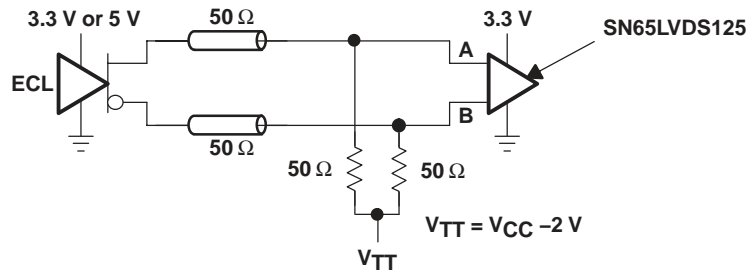


Figure 20. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

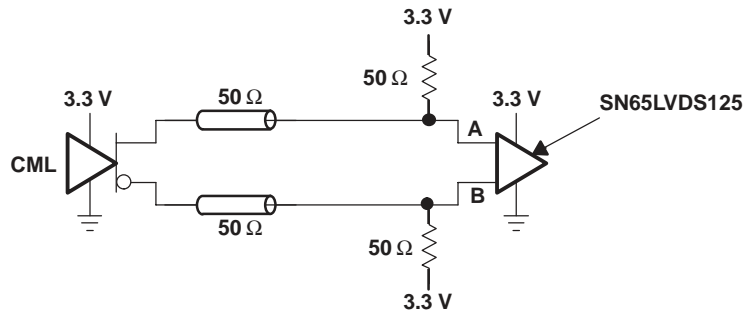


Figure 21. Current-Mode Logic (CML)

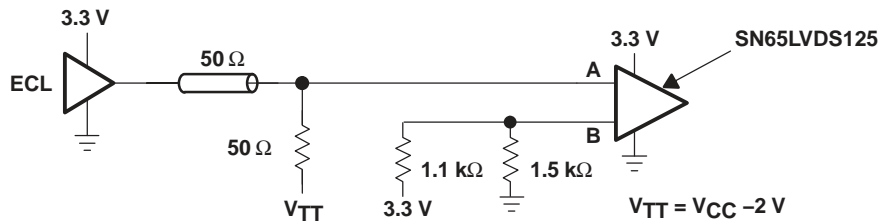


Figure 22. Single-Ended (LVPECL)

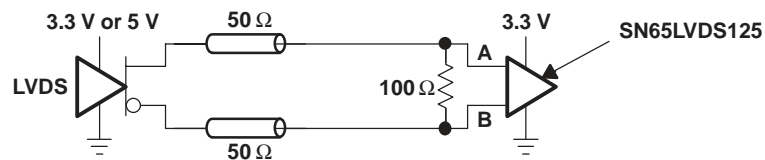
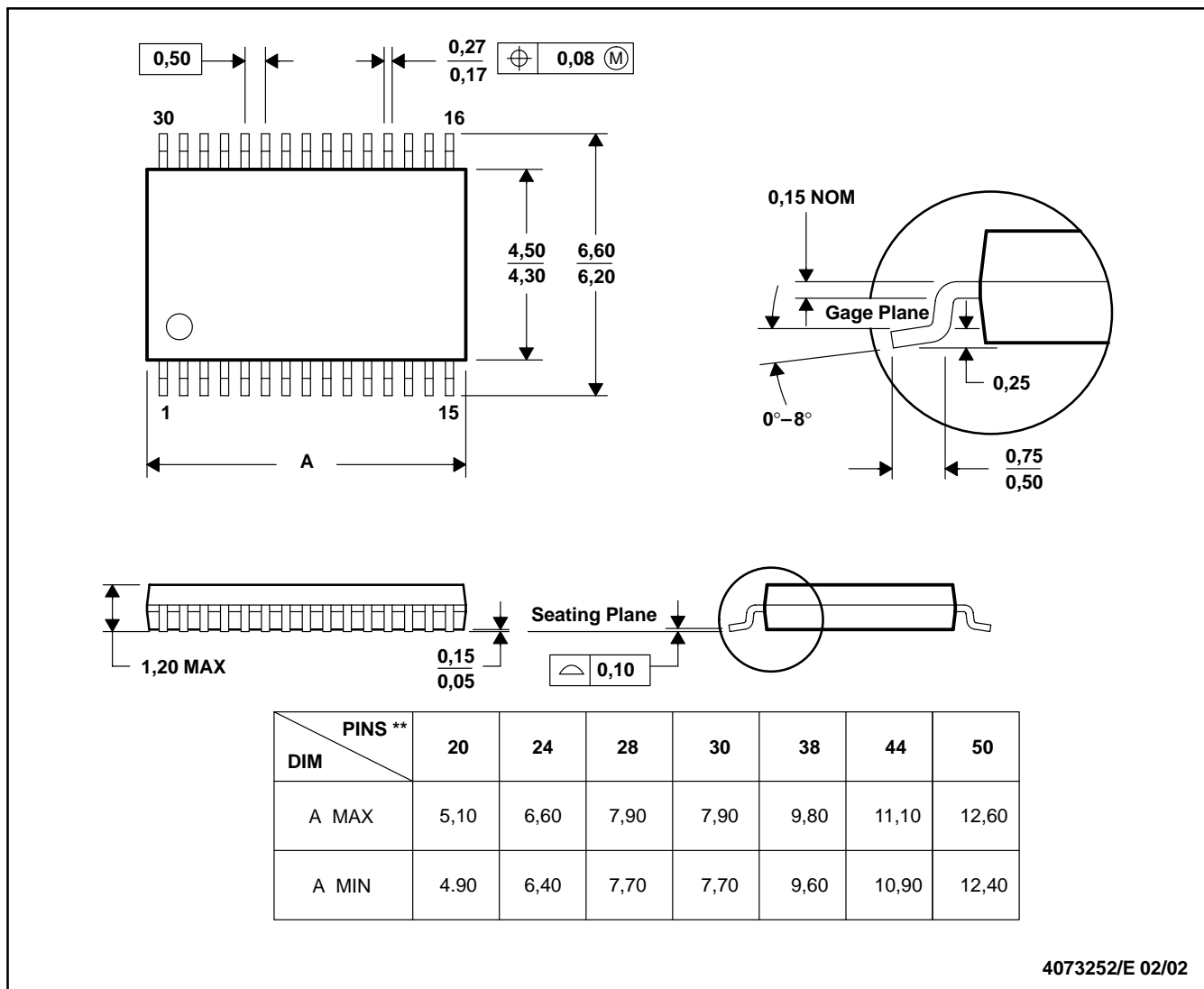


Figure 23. Low-Voltage Differential Signaling (LVDS)

DBT (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

30 PINS SHOWN



4073252/E 02/02

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-153

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